IMPLEMENTATION OF RECONFIGURABLE VITERBI DECODERS IN HARDWARE

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ABSTRACT

Channel coders are widely used in digital transmissions where data can be corrupted due to interference. They are used in a large proportion of digital transmission and digital recording systems, including digital mobile telephony and digital television broadcast, compact disc, and magnetic disk reading. Viterbi decoder is one of the most widely used channel decoders that are used for decoding data that are encoded using convolutional forward error correction codes. This research investigates an adaptive channel coder that is able to switch between few configurations depending on the channel conditions. Channel codes consist of encoders and decoders, and since encoders are rather simple, the main focus of the research is towards the decoders. The research explores into an optimized shared hardware structure between various Viterbi decoders especially of those being used in current technologies such as General Packet Radio Service (GPRS), Enhanced Data rates for GSM Evolution (EDGE), and Worldwide Interoperability for Microwave Access (Wimax). The research looks into optimized methods of memory management and is also aimed for high throughput to be used for high speed applications that are a trend for new and upcoming technologies. Initially the performance of various configuration of Viterbi decoder with respect to different channel conditions was looked into to select few suitable Viterbi decoders to be implemented on Field Programmable Gate Array (FPGA). The final implementation on FPGA combines three Viterbi decoders into a single core. The gain in area of the three Viterbi existing separately when compared to the joint hardware is about 15 %, with no loss in processing speed and throughput. The latency is measured to be a minimum amount with respect to the data size. For a packet size of 100 information bits and code rate r=1/2 the latency would be 162 cycles. The main idea in having a shared hardware structure was to basically map the trellis structure of the smaller Viterbi configuration over the larger one, thereby not taking any extra hardware of its own. The significance would be a reduced complexity of various Viterbi decoders existing on a single shared hardware.

ABSTRAK

Kod saluran digunakan dengan meluas di dalam transmisi digital di mana kerosakan maklumat boleh terjadi disebabkan gangguan bisingan. Teknik ini digunakan dengan banyaknya di dalam transmisi digital dan sistem rakaman digital, termasuk telefon bimbit dan siaran televisyen digital, cakera padat dan rakaman cakera bermagnet. Penyahkod Viterbi adalah salah satu penyahkod saluran yang digunakan dengan meluas untuk menyahkod maklumat yang telah dikod menggunakan kod pembetulan kesalahan ke hadapan konvolusi. Penyelidikan ini menyiasat kod saluran ubahsuai yang boleh bertukar konfigurasi bergantung kepada keadaan saluran isyarat. Kod saluran terdiri daripada pengekod dan penyahkod, dan sememangnya pengekod adalah mudah, maka fokus utama penyelidikan ini adalah ke arah penyahkod. Kajian ini juga menyelidik struktur perkakasan perkongsian optimum antara pelbagai penyahkod Viterbi terutamanya yang digunakan di dalam teknologi terkini seperti General Packet Radio Service (GPRS), Enhanced Data rates for GSM Evolution (EDGE), dan Worldwide Interoperability for Microwave Access (Wimax). Penyelidikan ini mengkaji kaedah optimum pengurusan memori dan juga untuk pemprosesan yang pantas untuk aplikasi kelajuan tinggi yang merupakan suatu bentuk teknologi baru akan datang. Pada mulanya prestasi pelbagai konfigurasi penyahkod Viterbi berdasarkan perbezaan keadaan saluran dikenalpasti untuk digunakan ke Field Programmable Gate Array (FPGA). Pelaksanaan terakhir adalah menggabungkan tiga penyahkod Viterbi ke dalam satu teras. Perolehan kawasan bagi tiga Viterbi yang wujud berasingan dibandingkan dengan perkakasan gabungan adalah kira-kira 15%, dengan tiada kekurangan kelajuan dan daya pemprosesan. Tempoh pendaman dikira sebagai jumlah minimum berdasarkan saiz data. Tujuan utama untuk menghasilkan struktur perkakasan perkongsian ialah pada dasarnya memetakan struktur trellis Viterbi yang mudah kepada struktur yang lebih kompleks; di mana kaedah ini tidak akan mengambil mana-mana lebihan perkakasan yang ada. Yang penting dan ternyata sekali di dalam kajian ini adalah pengurangan kompleksiti untuk pelbagai penyahkod Viterbi yang sedia ada dalam satu perkakasan perkongsian.

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GPRS	-	General Packet Radio Service
EDGE	-	Enhanced Data Rates for GSM Evolution
3G	-	Third Generation
WiMAX	-	Worldwide Interoperability for Microwave Access
MIPS	-	Millions of Instructions per Second
DSP	-	Digital Signal Processor
FPGA	-	Field Programmable Gate Array
BPSK	-	Binary Phase Shift Keying
TX	-	Transmitter
RX	-	Receiver
FEC	-	Forward Error Control
BER	-	Bit-Error Rate

Eb/No	-	Energy per Bit over Spectral Noise Density
SNR	-	Signal to Noise Ratio
CRC	-	Cyclic Redundancy Check
WLAN	-	Wireless Local Area Network
GSM	-	Global System for Mobile communication
EGPRS	-	Enhanced GPRS
TB-CC	-	Tail Biting Convolutional Codes
BTC	-	Block Turbo Codes
CTC	-	Convolutional Turbo Codes
LDPCC	-	Low Density Parity Check Codes
ZT-CC	-	Zero Tail Convolutional Code
OFDM	-	Orthogonal Frequency Division Multiplexing
OFDM A	-	Orthogonal Frequency Division Multiplexing Access
RS	-	Reed Solomon
CS	-	Coding Scheme
MCS	-	Modulation Coding Scheme
BCH codes	-	Bose-Chauduri-Hocquenghem codes
GF	-	Galois Field
XOR	-	Exclusive OR
CPLD	-	Complex Programming Logic Device
JTAG	-	Joint Test-Action Group
ROM	-	Read Only Memory
RAM	-	Random Access Memory
PSK	-	Phase Shift Keying
GMSK	-	Gaussian Minimum Shift keying
TDD	-	Time Division Muliplexing
FDD	-	Frequency Division Muliplexing
BPS	-	bits per second
MFDA	-	Modified Feed back Decoding Algorithm
FDA	-	Feed Back Decoding
BSC	-	Binary Symmetric Channel
TB	-	Trace Back

CHAPTER 1

INTRODUCTION

1.1 Background

Wireless digital communications is one of the most advanced technologies at present. In order to transmit multimedia information, which includes not only voice information but also various kinds of data such as pictures and moving images, communication systems must support very low bit error rate (BER) digital transmission. The communication channel introduces noise and interference to corrupt the transmitted signal. At the receiver, the corrupted transmitted signal is mapped back to binary bits. The received binary information is an estimate of the

transmitted binary information. Bit errors may result due to the transmission and the number of bit errors depends on the amount of noise and interference in the communication channel.

Channel coding is often used in digital communication systems to protect the digital information from noise and interference and reduce the number of bit errors. If channel coding was not used, data would have to be sent at much higher power, and sometimes due to certain design constraints/system requirement, transmission power is a limiting factor. To overcome power issues and at the same time be able to withstand harsh channel conditions, the data is given some protection, where on the receiver side; the data can be recovered even if some portion of the data stream was corrupted with noise/fading. Channel coding is mostly accomplished by selectively introducing redundant bits into the transmitted information stream. These additional bits will allow detection and correction of bit errors in the received data stream and provide more reliable information transmission. The cost of using channel coding to protect the information is a reduction in data rate or an expansion in bandwidth.

There are two main types of error correcting codes, namely block codes and convolutional codes. There are many differences between block codes and convolutional codes. Block codes are based rigorously on finite field arithmetic and abstract algebra. They can be used to either detect or correct errors. Some of the commonly used block codes are Hamming codes, Golay codes, BCH codes, and Reed Solomon codes (uses non-binary symbols).

Convolutional codes are one of the most widely used channel codes in practical communication systems. These codes are developed with a separate strong mathematical structure and are primarily used for real time error correction. Convolutional codes convert the entire data stream into one single codeword. The encoded bits depend not only on the current k input bits but also on past input bits, so basically every encoded bit has some memory of its neighboring bits. The main decoding strategy for convolutional codes is based on the widely used Viterbi algorithm.

1.2 Problem Description

High data rate communication such as GPRS, EDGE, 3G, Wimax are susceptible to multipath fading effects and therefore reliable error control is essential in such wireless communications. Usually, systems have to meet certain BER requirements that will satisfy the worst case channel conditions. For an error correction encoder, to meet worst case scenarios, it usually requires high level of redundancy bits added to the information bits. Adding too many redundancy bits will again reduce the high data rate that we are trying to achieve in the first place. The channel will not be in the worst case all the time, and therefore it is possible to transmit at higher data rates for most of the time. To overcome the effect of noise under very bad channel, and also not burden the throughput with too much protection under good channel condition, the error control schemes have to be able to adapt to the channel that the device is working on. Under harsh channel conditions, the data will have heavy protection against interference to meet the required BER, and under good conditions, the data will have minimal or no protection, and increase the data throughput.

Implementation wise, channel decoders have a high latency in decoding the received data and consumes many clock cycles or MIPS if it is implemented on DSP. With the demand for high data rate applications, latency is no longer a compromise in design. Parallel processing of the decoding blocks has become a must and its impact to the size of the decoder in terms of gate count has to be

compromised. Too high of a gate count or logic cells in FPGA is also not desired. DSP processors with no power in parallel processing have become too slow and usually require a hardware acceleration block to do such high speed processing in a separate core.

1.3 Project Objectives

The most widely used decoding algorithm as mentioned above is the Viterbi decoder which is used with different parameters for different standards requirements. This thesis analyses the different Viterbi decoders and implements a reconfigurable adaptive Viterbi decoder with shared hardware structure for GSM, GPRS, EDGE and Wimax technologies. The adaptability nature of the implemented Viterbi decoder helps to combat different channel conditions and can be used in a configurable manner to improve the received BER. The shared hardware structure would help in limiting the number of logic cells used compared to if the implementation were to be done separately. The high performance generic soft input hard output Viterbi decoder is prototyped on a FPGA.

1.4 Scope of Project

The scope of this study would be focused towards the channel coding blocks, such as convolution coding/Viterbi decoding and studying the effect of various channel models to obtain the best suitable coding rate and constraint length. The study does not include the effect of modulation, as the modulation scheme is fixed to BPSK.

The parameters of the various Viterbi decoders used in the study are of coding rates $r = 1/2$, and $r = 1/3$, and constraint length $k = 5$ and $k = 7$, which are the ones used in GSM, GPRS, EDGE and WiMax.

The fading model is a non-frequency selective Rayleigh fading with characteristics such as fast and slow fading. Fast fading is assumed such that the coherence bandwidth is larger that a symbol period, and the fading is uncorrelated, making the symbols independent to each other. Slow fading is limited to affect around 20 consecutive symbols, to avoid enhanced methods of interleaving. The interleaving mechanism to overcome the slow fading will be the standard block rectangular interleaver. It is assumed to be independent to the encoder/decoder design as it is placed after the channel coding process. The channel estimate and synchronization is assumed to be perfect. Figure 1.1 highlights the area of research.

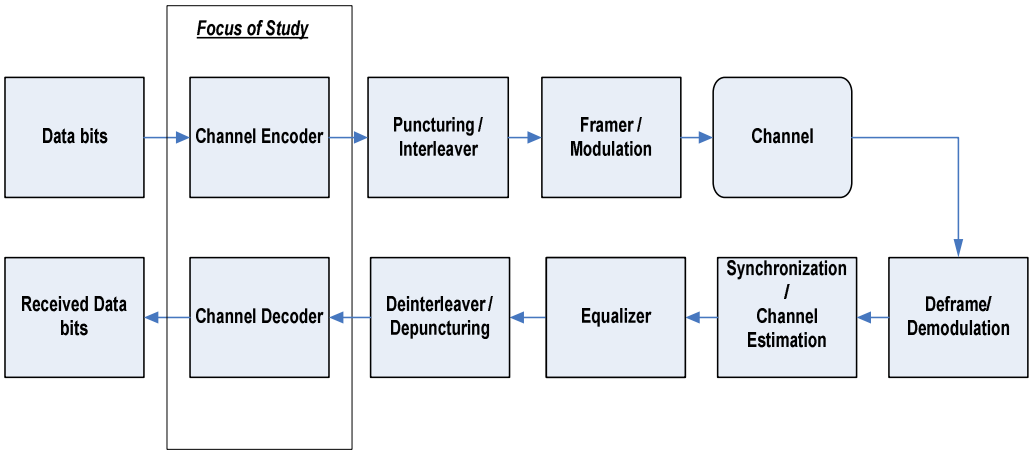

Figure 1.1: Tx – Rx modules

The channel encoder system can achieve various coding rates with the use of puncturing. Puncturing removes certain bit streams from the encoded data stream. Puncturing is used to achieve coding rates of $r = 2/3$, $r = 3/4$, $r = 5/6$ and $r = 7/8$.

The focus of the project basically is on the channel encoder (convolutional encoders) and decoder (Viterbi decoders) blocks with various CRC types. The CRC

is added to detect if the channel decoder was able to reconstruct the frame correctly or if there was a frame error.

1.5 Proposed Methodology

The designed adaptive encoder/decoder could be adopted to any wireless communication systems that requires robust error correction and also support high data rate. The hardware implementation combines the Viterbi decoder of constraint length K = 7 and K = 5. This combination allows the use of shared Viterbi decoder to be used on the GPRS, EDGE (Enhanced Data rates for Global Evolution) and 802.11(WLAN)/ 802.16 (Wimax) systems.

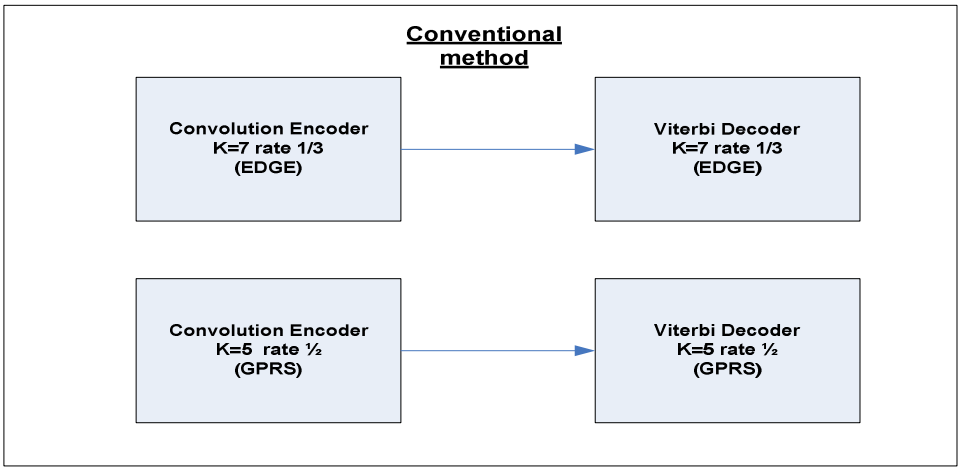

Figure 1.2: Conventional method for GPRS and EDGE

Figure 1.2 depicts the traditional method in having two different constraint lengths Viterbi decoder. For a mobile device that supports EDGE, it has to be backward compatible to the GPRS network. Since both these systems use different types of encoding methods, the conventional method of design is described in Figure 1.2. Below in Figure 1.3, a combined approach to share relevant blocks in doing the computation for the Viterbi decoder is described.

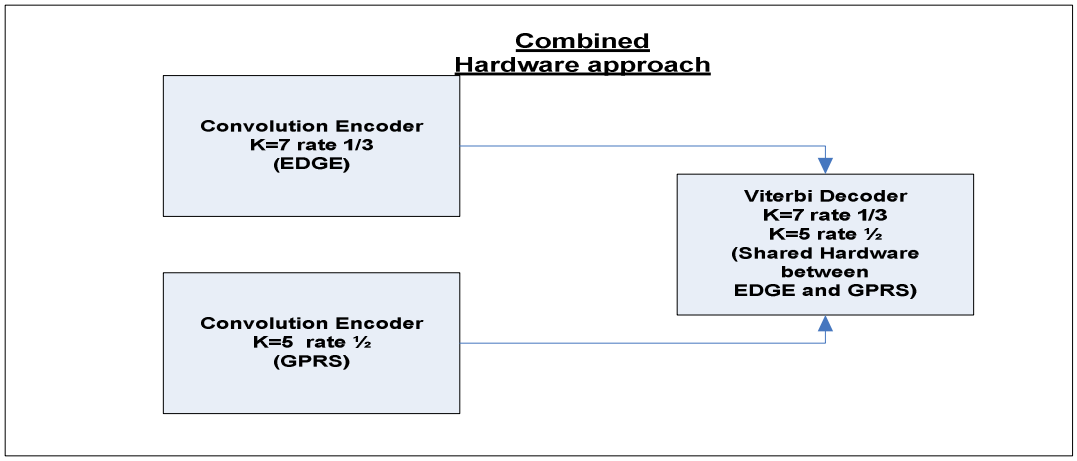

Figure 1.3: Shared Hardware approach GPRS and EDGE

Figure 1.4 shows the internal block diagram of a Viterbi decoder. Since all Viterbi decoders consist of these basic blocks, combining two different Viterbi decoder structure will be possible with the addition of configurable blocks.

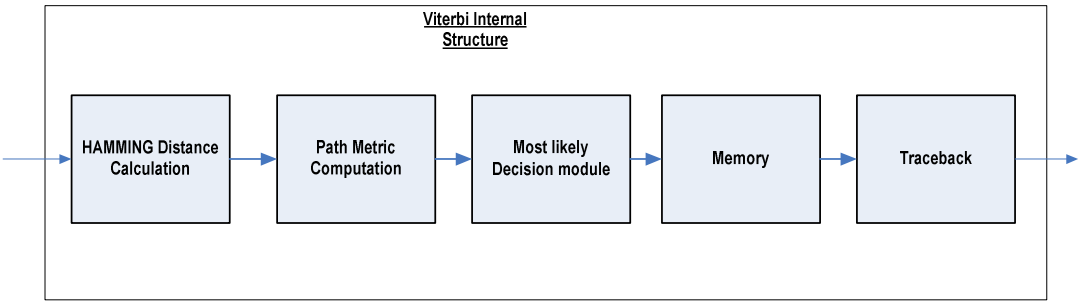

Figure 1.4: Internal Viterbi blocks

1.6 Outline of the Thesis

The thesis is outlined into 6 chapters. Chapter 2 will discuss the work done by other researchers in the related field. Chapter 3 describes the theory of background knowledge on some encoding/decoding processes is described to some detail. Further on in Chapter 4, the design methodology is described, followed by the results obtained from the experiment in Chapter 5. The results will cover both the results on the algorithm which includes performance curves and also on the RTL implementation. Chapter 6 summarizes the important findings regarding the shared structure and the thesis conclusion.