QUALITY IMPROVEMENT OF SHUNT ACTIVE POWER FILTER WITH DUAL PARALLEL TOPOLOGY

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To my beloved mother, father, family and friends

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Alhamdulillah, thanks to Allah S.W.T the most merciful and the most compassionate for the guidance and knowledge bestowed upon me, for without it I would not have been able to come this far. Peace is upon him, Muhammad the messenger of God.

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ABSTRACT

The potential of a shunt active power filter (APF) with dual parallel (DP) topology as proposed by Lucian Asiminoaei, Cristian Lascu, Frede Blaabjerg and Ion Boldea in mitigating the harmonics current in a three-phase power system feeding a nonlinear load has been verified by conducting a simulation study using Matlab/Simulink. In the control system of this shunt APF, the harmonic currents and the currents between feedback and feedforward APF from the three-phase line are used as a reference input. The error is the comparison of the reference current and the actual compensating harmonic currents from the power devices. The error produced is used as an input to a PI controller for hysteresis current controller (HCC) to generate the switching signals for the APF. The compensated currents produced from the feedback shunt APF will mitigate the 5^{th} and 7^{th} harmonics while the feedforward shunt APF will mitigate the rest of the harmonics until the 31^{st} order. This project proposed by implementing Fuzzy PI controller as a control strategy, APF generate better compensated harmonic currents to the line when more fuzzy rules are created. The APF with DP topology starts to compensate the harmonic currents at t = 0.4s and the load is change from R in series with L to R in parallel with C or vice versa at t = 0.7s. The Fuzzy PI controller response for the increase or reduce of load is faster besides PI controller to mitigate the harmonic currents. Fuzzy PI controller takes less than 0.1s to isolate the harmonics currents, but PI controller take more than 0.1s to isolate the harmonic currents. The total harmonic distortion (THD) when used Fuzzy PI controller is lower compared to PI controller.

ABSTRAK

Potensi penapis kuasa aktif (APF) pirau dengan topologi dwi selari (DP) yang dicadangkan oleh Lucian Asiminoaei, Cristian Lascu, Frede Blaabjerg dan Ion Boldea dalam mengasingkan arus harmonik dalam sistem kuasa tiga fasa bersama beban tidak linear disahkan dengan melaksanakan pembelajaran secara simulasi menggunakan Matlab/Simulink. Dalam sistem kawalan APF pirau ini, arus harmonik dan arus diantara suap balik dan suap kehadapan APF daripada talian tiga fasa digunakan sebagai masukan rujukan. Ralat adalah perbandingan antara arus rujukan dengan arus harmonik terpampas sebenar daripada peranti kuasa. Ralat yang terhasil digunakan sebagai masukan kepada pengawal PI untuk pengawal arus histerisis (HCC) menghasilkan isyarat pensuisan APF. Arus terpampas yang terhasil dari suap balik APF pirau akan menghasilkan harmoni ke-5 dan ke-7 manakala suap balik kehadapan APF pirau akan mengasingkan yang selebihnya sehingga harmonik ke-31. Projek ini dicadangkan dengan melaksanakan pengawal Fuzzy PI sebagai strategi pengawalan, APF menghasilkan arus harmonik terpampas yang baik kepada talian apabila banyak arahan fuzzy digunakan. APF dengan topology DP mula untuk memampas arus harmonik pada t = 0.4s dan beban akan bertukar dari R sesiri dengan L kepada R selari dengan C atau sebaliknya pada t = 0.7s. Respon pengawal Fuzzy PI kepada penambahan atau pengurangan beban adalah lebih pantas berbanding pengawal PI untuk mengasingkan arus harmonik. Pengawal Fuzzy PI mengambil masa kurang dari 0.1s untuk mengasingkan arus harmonik tetapi pengawal PI mengambil masa lebih daripada 0.1s untuk mengasingkan arus harmonik. Penjumlahan herotan harmonik (THD) apabila menggunakan pengawal Fuzzy PI adalah rendah berbanding menggunakan pengawal PI.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF APPENDIX

CHAPTER 1

INTRODUCTION

Malaysia grid transmission lines typically supply a large amount of harmonics produced by customers in heavy industry and factory. The harmonics produce by nonlinear loads like heavy machine and furnace will disturb other appliances like television, laptop and all electronic devices. The usage of the nonlinear load will increase the harmonics distortion and reduce the power quality. To overcome this problem, active power filter (APF) can be used as a device to eliminate the harmonics in the grid system.

1.1 Project Background and Review

Harmonics issue is very popular nowadays. This is because harmonics not only damage the customer devices, but it can also lead to system failure. As an example, in a radio communication system for marine organization, the signal is sent from the headquarters, but if the filtering device fails the signal will crash. The data received from the headquarters is not full and always missing. This problem occurs because the harmonics distort the communication system at the sending and receiving ends. In certain cases, harmonic can be very useful for controlling a system. In engineering, harmonics are used as part of a control system, such as in light rail transit system (LRT). This is the easiest controlling technique to avoid accidents between trains.

The power quality problems are not new in power distribution, but only recently the effects of these problems have gained public awareness. Advances in semiconductor device technology have fuelled a revolution in power electronics, and there are indications that this trend will continue [1]. However these power equipments which include adjustable-speed motor drives (ASDs), electronic power supplies, direct current motor drives, battery chargers and electronic ballasts are responsible for the rise in related power quality problems [2] - [4]. These nonlinear loads are constructed by nonlinear devices, in which the current is not proportional to the applied voltage. A simple circuit as shown in Figure 1.1 illustrates the concept of current distortion. In this case, a sinusoidal voltage is applied to a simple nonlinear resistor in which the voltage and current vary according to the curve shown. While the voltage is perfectly sinusoidal, the resulting current is distorted.

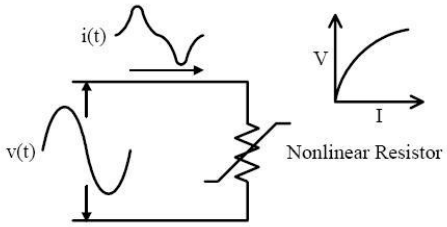


Figure 1.1 Current distortion caused by nonlinear resistance

Nonlinear loads appear to be prime sources of harmonic distortion in a power distribution system. Harmonic currents produced by nonlinear loads are injected back into power distribution systems through the point of common coupling (PCC). These harmonic currents can interact adversely with a wide range of power system equipment, most notably capacitors, transformers, and motors, causing additional losses, overheating, and overloading [2] - [4].

There are set of conventional solutions to the harmonic distortion problems which have existed for a long time. The passive filtering is the simplest conventional solution to mitigate the harmonic distortion [1], [8]. Although simple, these

conventional solutions that use passive elements do not always respond correctly to the dynamics of the power distribution systems [8]. Over the years, these passive filters have developed to high level of sophistication. Some even tuned to bypass specific harmonic frequencies. However, the use of passive elements at high power level makes the filter heavy and bulky. Moreover, the passive filters are known to cause resonance, thus affecting the stability of the power distribution systems [9]. As the regulatory requirements become more stringent, the passive filters might not be able to meet future revisions of a particular Standard.

1.2 Objective

The objectives of this project are:

- To study the characteristics of a three-phase power system that is connected to a nonlinear load.
- To study the effect of using proportional integral (PI) controller and a Fuzzy PI controller on a shunt active power filter (APF) with dual parallel (DP) topology.

1.3 Scope of project

The scope of this project is based on the objectives as stated in Section 1.2. A shunt APF with dual parallel (DP) topology [7] is studied and analyzed when used to mitigate the harmonics in a three-phase power system that is feeding a nonlinear load. The nonlinear load is represented by a three-phase rectifier that is connected to a load of either a resistor (R) in series with an inductor (L) or R that is parallel to a capacitor (C). To improve the performance of the shunt APF with DP topology, a Fuzzy PI instead of a PI controller is proposed as part of its control system.

1.4 Project Overview

The overall APF system proposed for this project is shown in Figure 1.2. In the simulation design of the shunt APF with DP topology, a 100 V, 50 Hz three-phase power supply has been considered. The power system is connected to a three-phase rectif

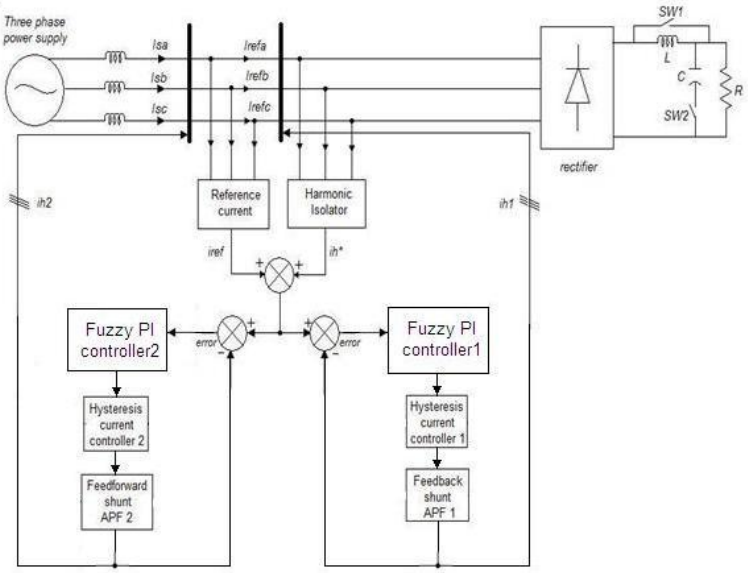


Figure 1.2 Block diagram of the proposed topology

The supply current that distorts due to the nonlinear load will be compensated by the shunt APF. From Figure 1.2, the function of the feedback and feedforward shunt APF is to compensate the harmonic currents faster than usual [7]. The feedback shunt APF will mitigate the 5^{th} and 7^{th} harmonic current while the feedforward shunt APF will mitigate the rest of the harmonics until the 31^{st} order.

Refering to Figure 1.2, the current flowing into the middle of the feedforward APF and feedback APF is used as the reference current, i_{ref} to make the DP topology isolate the harmonic currents faster than conventional APF. The distorted current is fed into the harmonics isolator to produce the inversed of the harmonic currents in the line. The harmonics isolator algorithms are based on the instantaneous active and reactive power [17], [18]. The harmonic currents coming out of the harmonic isolator, i_h^* is added with i_{ref} as the reference signals to the closed loop control system. Error is the difference between the reference signals with the actual compensated harmonic currents; i_{h1} and i_{h2} produce by the APF. The error is used as an input to a PI or a Fuzzy PI controller to control the Hysteresis current controller (HCC).

1.5 Organization of Thesis

The thesis is organized into six chapters as follows:

Chapter I discusses the objective, scope and general concepts of the proposed project.

Chapter II gives the literature review of the work carried out which includes the principles of the control strategy used in the shunt APF with DP topology.

Chapter III provides the details of the shunt APF with DP topology including the relevant equations and operation of the system.

Chapter IV shows the simulation design and the results of each stage. The system is constructed using Matlab/Simulink blocks. Results of the simulation study conducted are described in this chapter.

Chapter V consists of some discussion on the results of the simulation study and some suggestions for future work.

Chapter VI gives the conclusion of the project.

CHAPTER 2

LITERATURE REVIEW

This chapter presents the conventional filter, active power filter (APF) and the basic control technique. The passive filter and the conventional APF such as series, parallel and hybrid APFs are reviewed to study the operation to compensate the harmonic currents. The control method such as bipolar, unipolar, and hysteresis band current controller modes are reviewed to design the controlling system.

2.1 Fundamental of Harmonic Distortion

Due to the proliferation of nonlinear loads from power electronics converters, one of the electric power quality (PQ) issues that received much attention is the harmonic distortion. These nonlinear loads control the flow of power by drawing currents only during certain intervals of the 50/60 Hz period. Figure 2.1 [12] illustrates that any periodic, distorted waveform can be expressed as a sum of pure sinusoids. The sum of sinusoids is referred as a Fourier series. The Fourier analysis permits a periodic distorted waveform to be decomposed into an infinite series containing DC component, fundamental component (50/60 Hz for power systems) and its integer multiples called harmonic components. The harmonic number (h) usually specifies a harmonic component, which is the ratio of its frequency to the fundamental frequency [4].

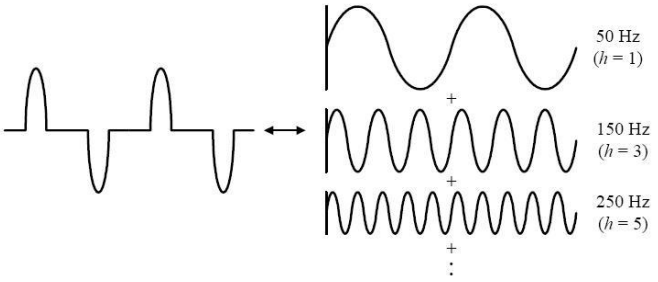


Figure 2.1 Fourier series representation of a distorted waveform

The total harmonic distortion (THD) is the most common measurement indices of harmonic distortion [3], [4]. THD applies to both current and voltage and is defined as the root-mean-square (*rms*) value of harmonics that is divided by the *rms* value of the fundamental, and then multiplied by 100% as shown as the following equation:

$$THD = \frac{\sqrt{\sum_{h>1}^{h_{max}} M_h^{\,2}}}{M_1} \times 100\%, \tag{2.1}$$

where M_h is the *rms* value of the harmonic component *h* of the quantity M.

THD of current varies from a few percent to more than 100%. THD of voltage is usually less than 5%. Voltage THDs below 5% are widely considered to be acceptable, while values above 10% are definitely unacceptable and will cause problems for sensitive equipment and loads [4].

2.2 Harmonic Distortion Impacts on Electric Power Quality

Figure 2.2 [13] shows the result of distorted currents passing through the linear, series impedance of a power distribution system, but the source currents is a pure sinusoidal. There is a nonlinear load that draws the distorted current. The harmonic currents pass through the impedance of the system hence causing a voltage drop for each harmonic. This prompts the appearance of harmonic voltages at the point of common coupling (PCC). The amount of voltage distortion depends on the source impedance and the current supplied out. Harmonics have a number of undesirable effects on electric PQ and fall into two basic categories, short-term and long-term. Short-term effects are usually the most noticeable and are related to excessive voltage distortion. On the other hand, long-term effects are regularly concealed and are usually associated with either increased resistive losses or voltage stresses [13]. In addition, the harmonic currents produced by nonlinear loads can interact adversely with a wide range of power system equipment, most notably recognized capacitors, transformers, and motors, causing additional losses, overheating, and overloading. These harmonic currents could also instigate interferences with telecommunication lines and errors in metering devices [2], [3], [4], [13].

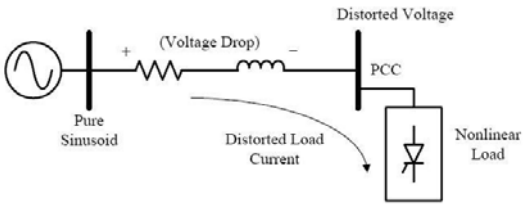


Figure 2.2 Harmonic currents flowing through the system impedance result in harmonic voltages at PCC

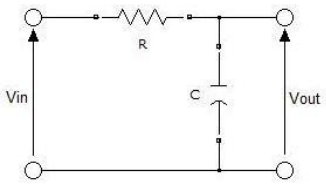
Because of the adverse effects that harmonics engage on electric PQ, certain standards have been utilized to define a reasonable framework for harmonic control [13]. The objective of such Standard is to propose steady-state harmonic limits that are acceptable by both electric utilities and their customers.

2.3 Harmonic Mitigation Approaches

Harmonic distortion in power distribution systems could be eradicated with three main approaches mainly passive filtering, active filtering and hybrid power filtering. These sections discuss the general properties of the various approaches for harmonic distortion mitigation. The advantages, disadvantages, and limitations of these approaches are also discussed in this section.

2.3.1 Passive Power Filter

Harmonic distortion problems exist because of the growth of industry. To overcome this problem, passive filter is used as a conventional solution to isolate the harmonic currents. Passive filter is a harmonic filter that does not have any active components such as transistor. There are five types of basic passive filter such as low pass, high-pass, all-pass, band-pass and notch-pass as shown in Figure 2.3 [1].



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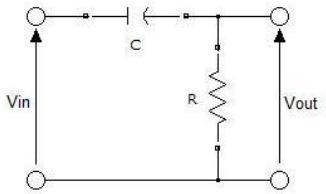

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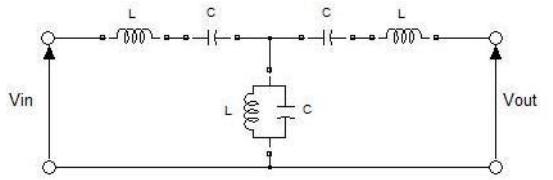

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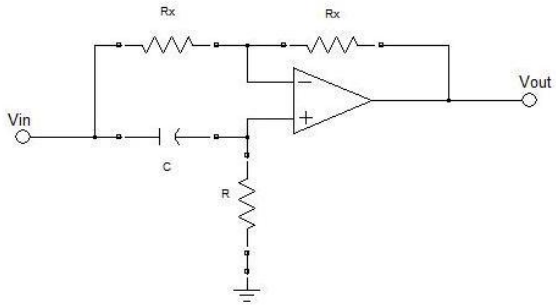

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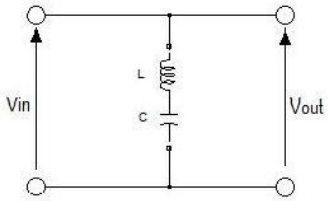


(e)

Figure 2.3 Types of passive filters (a) Low-pass filter (b) High-pass filter (c) Band-pass filter (d) All-pass filter (e) Notch-pass filter

Low-pass filter is a filter that only passes low frequency and rejects the signal above cut off frequency [1] as shown in Figure 2.3 (a). High-pass filter is the opposite of that low-pass filter as shown in Figure 2.3 (b). High-pass filter is a filter that only passes high frequency and reject the signal below cut off frequency [1]. Figure 2.3 (c) illustrates a band-pass filter. Band-pass filter is a filter that only passes the frequency within the setting range and eliminates the signal of outer range. In addition, this filter

could be exploited by merging the low and high - pass filter [1]. All-pass filter is a type of filter that allows passes of all amplitude by shifting modifying the signal to other phases. Besides, all-pass filter is recognized as a phase-shift filter as shown in Figure 2.3 (d) [1]. Notch-pass filter is the opposite of that band-pass filter as shown in Figure 2.3 (e) [1]. A notch-pass filter or band-stop filter is a filter that only passes the frequency not altered but rejects the selected signal.

Passive filter is used to overcome harmonic problems however could not work properly because of the frequency in the three-phase line is variable. The effect of the harmonic suppression is inspired by impedance and other parameter, whereby resonance will occur between the power impedance and passive filter [2].

2.3.2 Active Power Filter

APF is a filter that uses power electronic switching to generate the compensated currents that isolate the harmonic currents when injected to the three-phase line. APF has a good harmonic suppression, but the problem is APF could not be used in high power situation because of cost a hefty price [4] and APF performance depends on the power device topology and the control method. There are three types of APF such as series, shunt and hybrid APF.

Figure 2.4 represents the series APF. Series APF signifies that APF is connected in series with the utility through a transformer. Series APF is suitable for harmonic currents compensation of a voltage harmonic source such as diode rectifier and DC link capacitor [6].

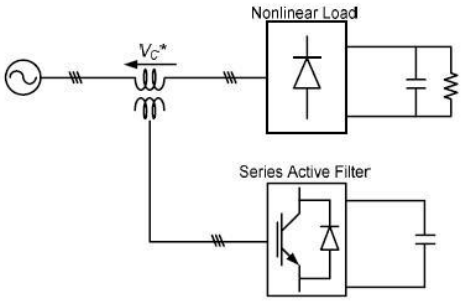


Figure 2.4 Series APF

The main advantage of series APF is to sustain the output of three-phase voltage waveform to be sinusoidal compared to shunt APF.

Shunt APF is connected in parallel with nonlinear loads shown in Figure 2.5. Shunt APF is used to mitigate the harmonic currents by injecting the compensating current i_c^* to the point of common coupling (PCC) [7]. Shunt APF does not only mitigate the harmonic currents, but also can compensate the reactive power and balance the three-phase currents [6].

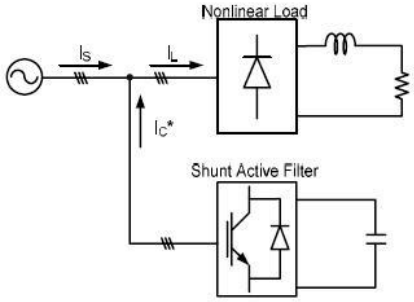
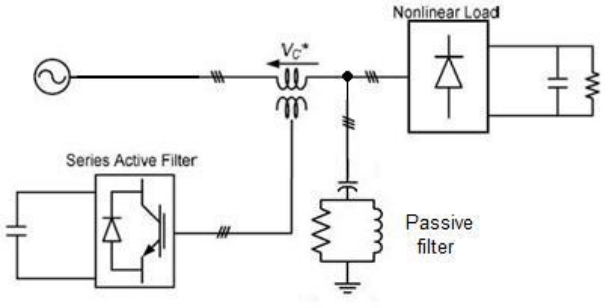


Figure 2.5 Shunt APF

The drawback of the shunt APF is difficult to implement in a large scale and the cost is too high.

Combination of APF and passive filter would enhance better result in harmonic mitigation, hence improving the APF performance. This combination is termed as hybrid APF [6] - [11]. The hybrid APF configuration is shown in Figure 2.6. From this figure, passive filter will mitigate the harmonic currents and the APF will shelter the passive filter from power resonance.



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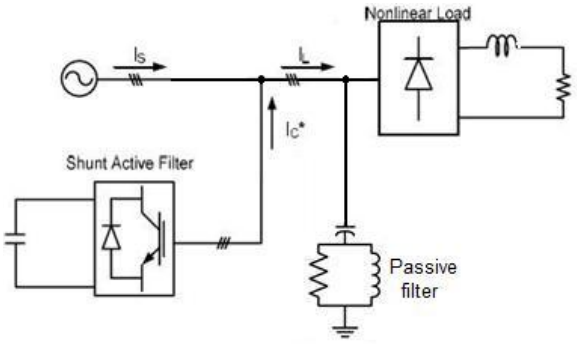


(b)

Figure 2.6 Hybrid APFs: (a) Combination of shunt APF and shunt passive filter
(b) Combination of series APF and shunt passive filter

Hybrid APF is suitable to high power application compared to passive filter, series and shunt APF.

2.4 Control Technique

For the APF to operate properly, various switching methods can be used to control the inverter output such as bipolar mode, unipolar mode and hysteresis current control mode. Figure 2.7 [12] shows the bipolar switching mode control. In this control technique, only one signal is used to compare with a saw tooth signal to produce the switching signals of the APF.

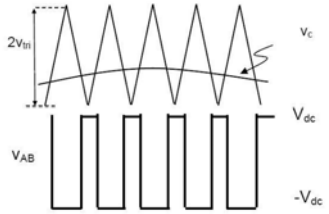


Figure 2.7 Bipolar mode control

Figure 2.8 [12] shows the unipolar switching mode control. In this control technique, two signals are used to compare with saw tooth signal to produce the switching signals.

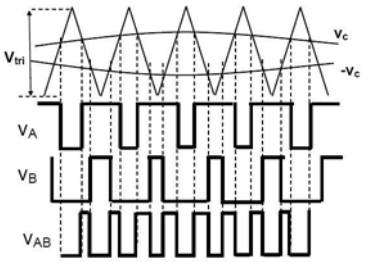


Figure 2.8 Unipolar mode control

Figure 2.9 [12] shows the hysteresis band current control mode. In this control technique, the upper and lower band is set up to build up the expected sinusoidal output.

In this control technique, the actual currents that produced are compared with the reference current to produce the hysteresis switching signal.

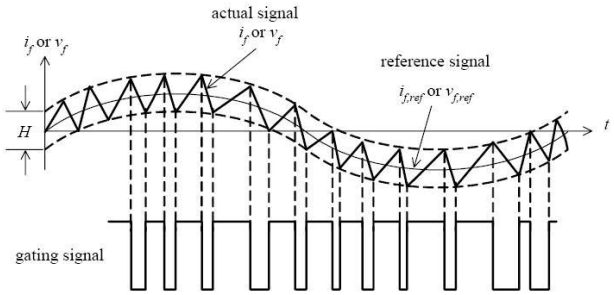


Figure 2.9 Hysteresis band current control mode

CHAPTER 3

SHUNT APF WITH DUAL PARALLEL (DP) TOPOLOGY

This chapter presents the basics of the shunt APF with DP topology as proposed by [7] and the control method employed to produce the switching signals for the APF. The development of Fuzzy PI instead of the conventional PI controller as part of the Hysteresis current controller (HCC) for the control of the APF in producing the compensated current that eliminates the harmonics current is also elaborated in this chapter.

3.1 Research Methodology

Figure 3.1 shows the flow chart of the work carried out for the project. The system simulation is conducted using Matlab/Simulink. The Simulink blocks are used to simulate the operation of the three-phase power system that is connected to a nonlinear load represented by a rectifier. This project starts with a literature review on various APF topologies, which later reveals the potential of the shunt APF with DP topology.

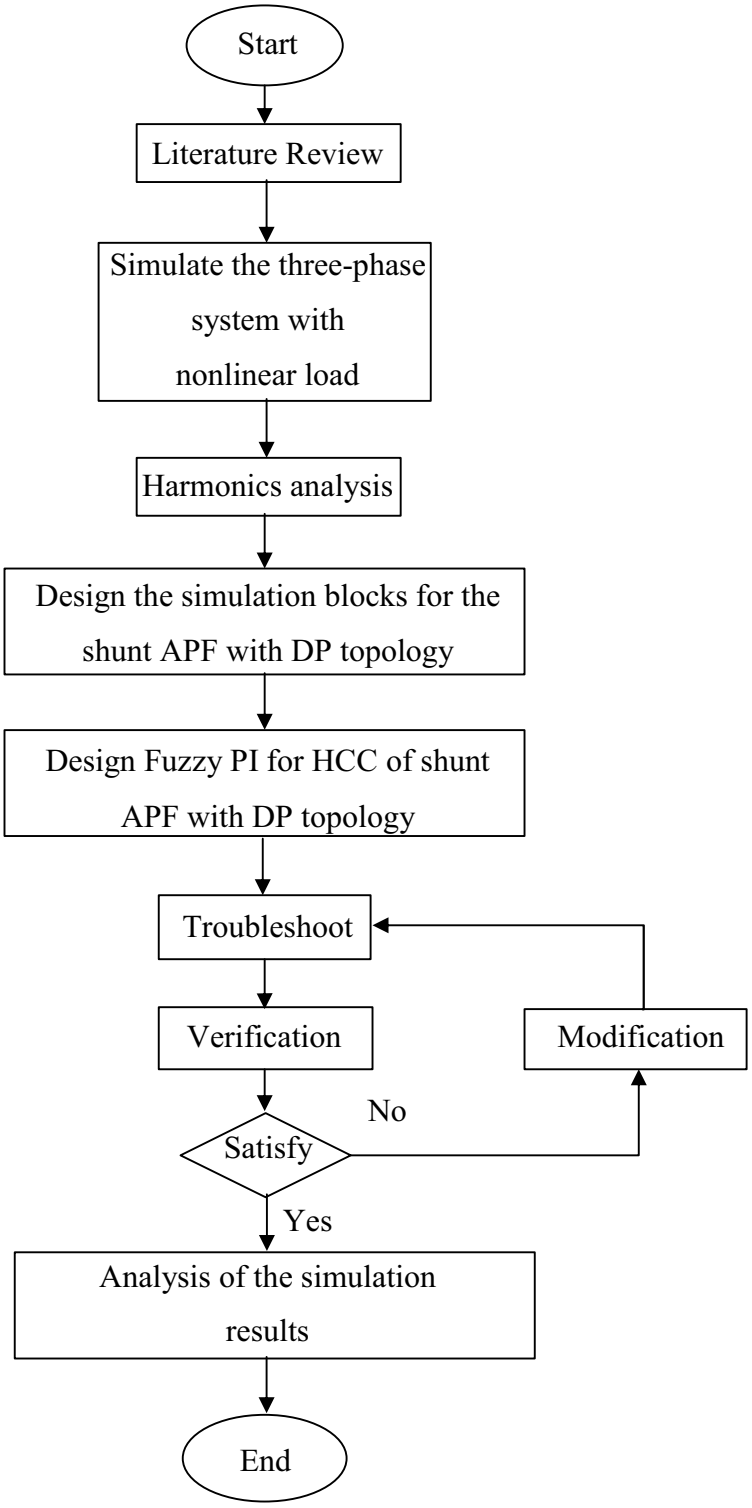


Figure 3.1 Flow chart of work carried out

The operation of the shunt APF with DP topology is then simulated by connecting it to the three-phase power system. In this case a PI controller is applied to the HCC in generating the switching signals, as proposed by [20]. A Fuzzy PI

controller is then designed and simulated to replace the conventional PI controller for the HCC of the shunt APF. The Fuzzy PI controller is proposed to isolate the harmonic currents faster than using the PI controller. The fuzzy rules are modified to reach the best performance in the same time frame. Lastly, the simulation results are analyzed to compare the harmonic currents isolation and performance of the shunt APF with DP topology when using PI and Fuzzy PI controller.

3.2 Shunt APF with DP Topology

Figure 3.2 shows the simulation design of the three-phase shunt APF with DP topology. The three-phase system with different nonlinear load is used to test the closed loop current controller and the APF performance in eliminating the harmonic currents.

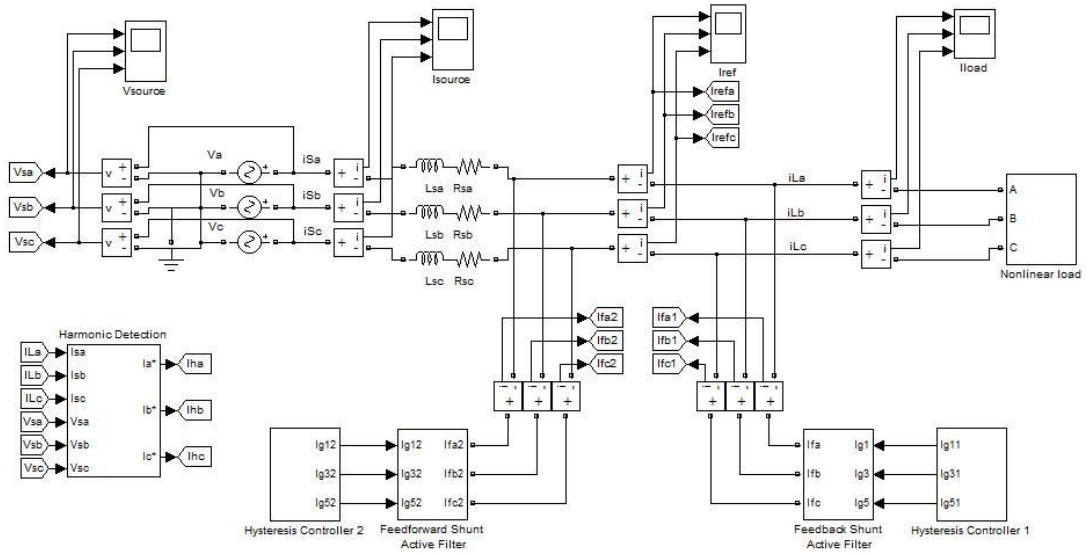


Figure 3.2 Simulation design of the three-phase shunt APF with DP topology

In the simulation block set, the harmonics are detected by developing the harmonic extraction block to generate the harmonic current i_h to isolate the desired compensated harmonic currents with the fundamental signal. The harmonic currents

generated by each phase, i_{ha}, i_{hb} and i_{hc} are used as reference in the hysteresis current controller. In this system, the DP topology makes the elimination of the harmonic currents better than using only feedforward APF. The feedback shunt APF will improve the steady state performance of the harmonic mitigation while the feedforward shunt APF will improve the dynamic response.

3.3 RL and RC Nonlinear Load Modeling

To test the system performance, a nonlinear load with an uncontrolled diode rectifier is used. Figure 3.3 shows the simulation blocks of the nonlinear load. The ideal switch is used to design the load to be R in series with L and R in parallel with C.

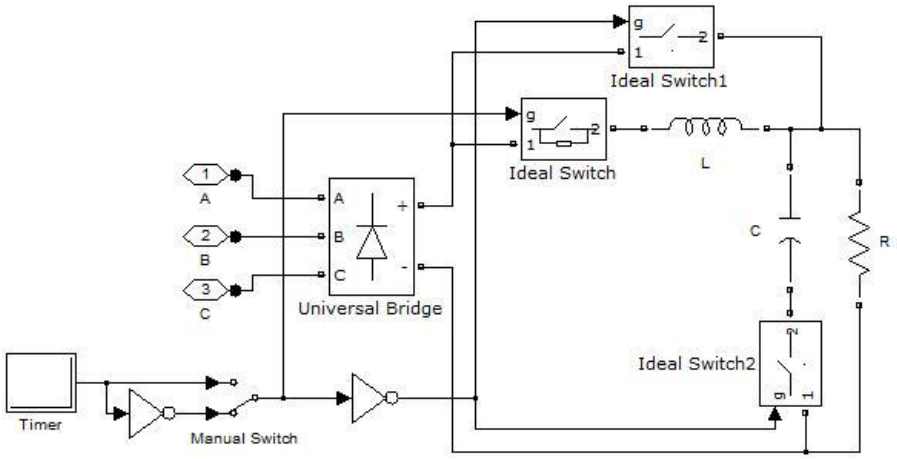


Figure 3.3 Three-phase rectifiers with RL/RC nonlinear load

Timer and manual switch is used to change the load from RL to RC or vice versa at t = 0.7s. The changing of the nonlinear load is done automatically while the simulation is running. The universal bridge or three-phase rectifier will produce the harmonic currents because of the conductivity and the voltage loss of each diode inside the universal bridge.

3.4 Harmonic Detection

The harmonics current is used in the HCC to generate the switching signals of the power device of the inverter. Figure 3.4 shows the simulation blocks developed based on [7] for harmonic detection. The three phase source current and voltage are used to define the active and reactive powers that occur in the system. The reactive power is extracted by transforming the three phase system to α□, and then the harmonic currents, $I_{h\alpha}$ and $I_{h\square}$ are transposed to get the harmonic current for each phase.

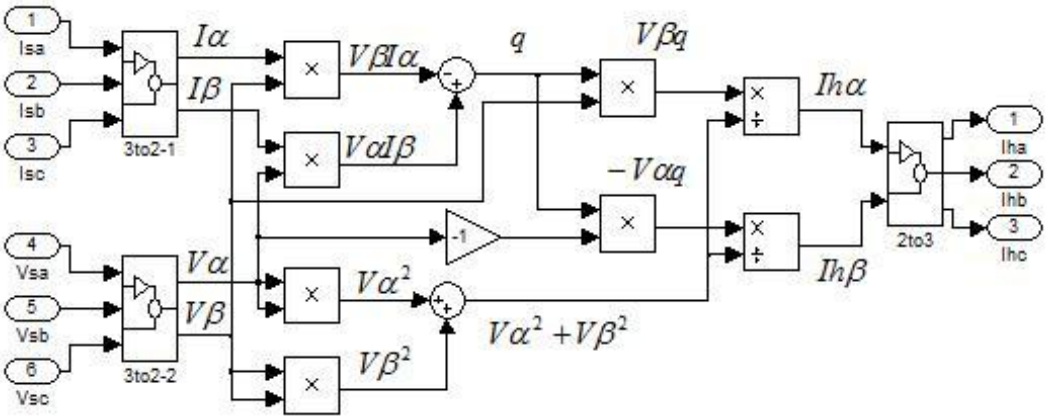


Figure 3.4 Simulation blocks for harmonic detection

The subsystem blocks (3to2-1 and 3to2-2) in Figure 3.4 are used to transform the three-phase system to α□ and the subsystem block (2to3) is used to transpose α□ to the three-phase harmonic currents. From [24] and [25], in $\alpha - \square$ coordinates, I and V as current and voltage are considered in phase α as,

$$I_{\alpha} = 0.8164Isa - 0.4082Isb - 0.4082Isc \tag{3.1}$$

$$V_{\alpha} = 0.8164Vsa - 0.4082Vsb - 0.4082Vsc \tag{3.2}$$

the values in phase □ is lagging I and V for 90^0,

$$I_{\square} = 0.7071Isb - 0.7071Isc \tag{3.3}$$

$$V_{\square} = 0.7071Vsb - 0.7071Vsc \tag{3.4}$$

$$q = V_{\alpha} I_{\square} - V_{\square} I_{\alpha} \tag{3.5}$$

the harmonic current, I_h in α and $\square$,

$$I_{h\alpha} = \frac{V_{\square} q}{V_{\alpha}^2 + V_{\square}^2} \tag{3.6}$$

$$I_{h\square} = \frac{-V_{\alpha} q}{V_{\alpha}^2 + V_{\square}^2} \tag{3.7}$$

harmonic current, I_h for every phase,

$$I_{ha} = 0.8164 I_{h\alpha} \tag{3.8}$$

$$I_{hb} = -0.4082 I_{h\alpha} + 0.7071 I_{h\square} \tag{3.9}$$

$$I_{hc} = -0.4082 I_{h\alpha} - 0.7071 I_{h\square} \tag{3.10}$$

Figure 3.5 shows the phase harmonic currents I_{ha}, I_{hb} *and* I_{hc} that are extracted from the three-phase system. The harmonic currents from the harmonic detection block will be used in the hysteresis current controller.

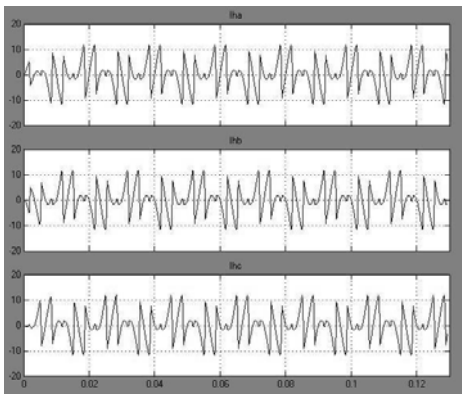


Figure 3.5 Harmonic current for each phase

3.5 Feedback and Feedforward APF

For the shunt APF with DP topology, the same APF is used for feedback and feedforward compensation, but the value of the inductance is different for each case. For feedback shunt APF, the inductance value is 5.6 mH to mitigate the 5th and 7th harmonic current. For feedforward APF, the inductance value is 3.0 mH to mitigate the rest of the harmonic currents until the 31st order. Figure 3.6 shows the APF that is used in the DP topology. From this figure, the timer and ideal switch is used to set the system start to isolate the harmonic current at t = 0.4s. The IGBT/Diode pair is used as a power switch in the APF.

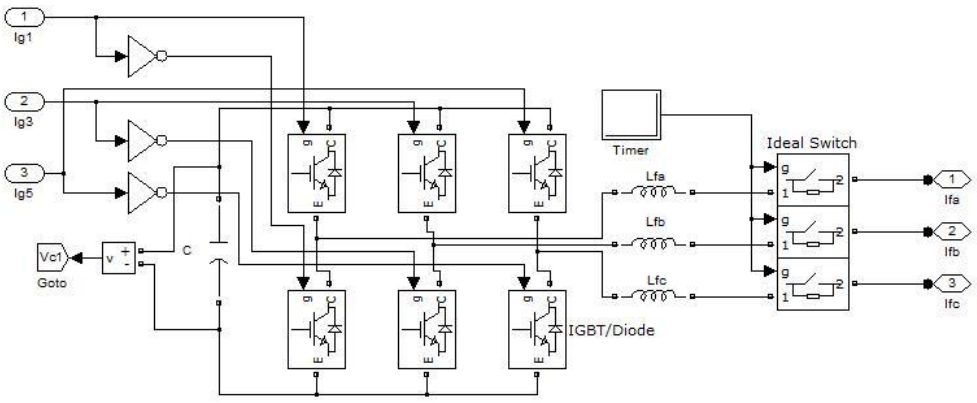


Figure 3.6 Simulation block of shunt APF

A capacitor C of 2.2 mF is used to produce the compensated current. The capacitor voltage is measured and will go through charging and discharging to be used in the control part to generate the error. From Figure 3.6, the inverter output voltage, V_x is,

$$Vx = Lx\frac{difx}{dt} + ex \tag{3.11}$$

where L_x is the inductor and e_x is the line voltage. In discrete form,

$$Vx^*(n+1) = Lx\frac{i^*fx(n+1) - ifx(n)}{Ts} + ex(n) \tag{3.12}$$

Kirchhoff current law at PCC,

$$ifx(n) = iLx(n) - iSx(n) \tag{3.13}$$

where $if_x(n)$ is the compensated current, $iL_x(n)$ is the load current and $iS_x(n)$ is the source current. The error becoming less significant when the sampling frequency increases,

$$if^*x(n) = iLx(n) - iS^*x(n) \tag{3.14}$$

and the active filter current can be expressed as

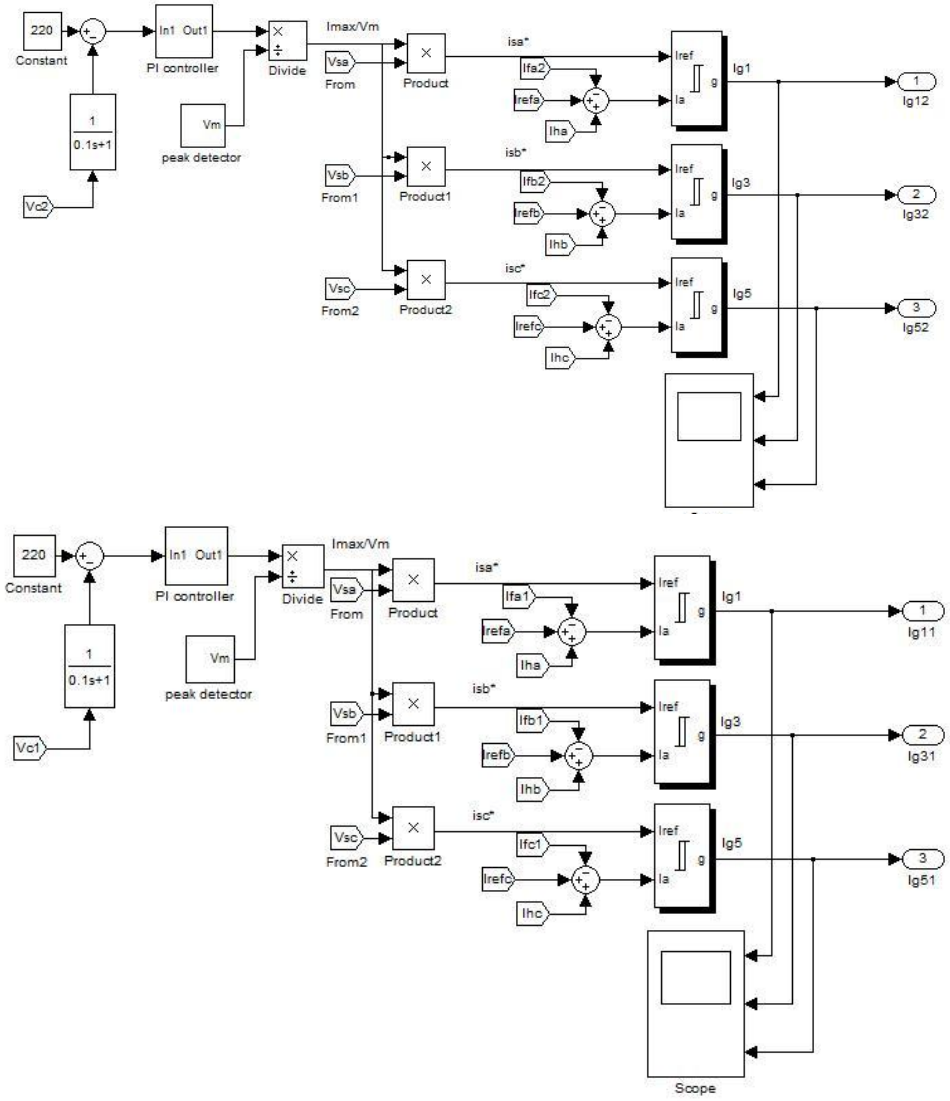
$$\frac{difx}{dt} = \frac{Vxn(t) - ex}{Lx} \tag{3.15}$$

3.6 Hysteresis Current Controller (HCC)

Hysteresis current controller is used to generate the switching signals for the shunt APF for both the feedback and feedforward sides. Two types of controllers are considered for the HCC, in this case the PI and Fuzzy PI controller in generating the switching signals.

3.6.1 PI Controller

PI controller is one of the methods used to monitor the control system. Figure 3.7 shows the PI controller of the HCC for feedback and feedforward shunt APF. The stability of the control system is determined by referring to the bode plot when the proportional gain, *Kp* and integral gain, *Ki* are changed. For this DP topology, *Kp* and *Ki* have been set as 0.75 and 9.15 respectively.



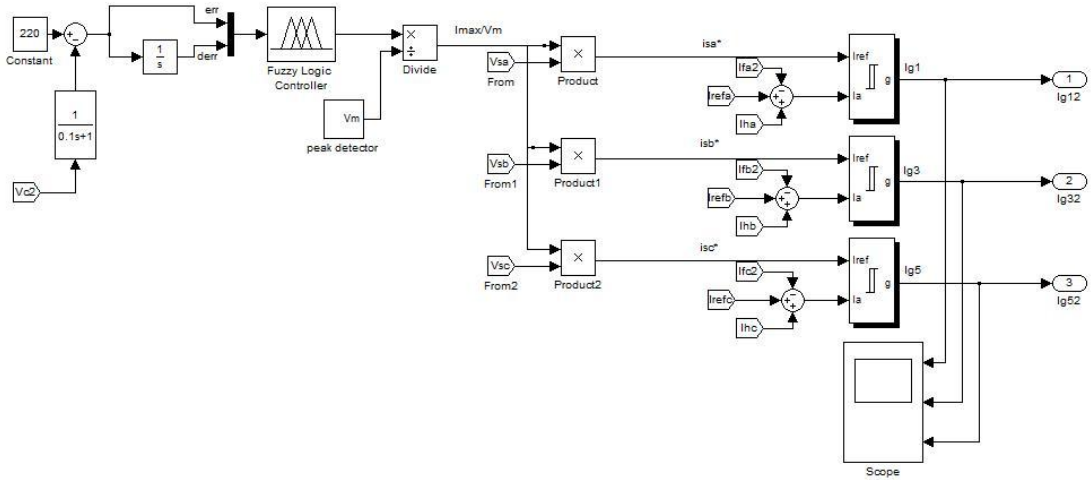
(b)

Figure 3.7 PI controller of the HCC for the shunt APF (a) Feedforward (b) Feedback

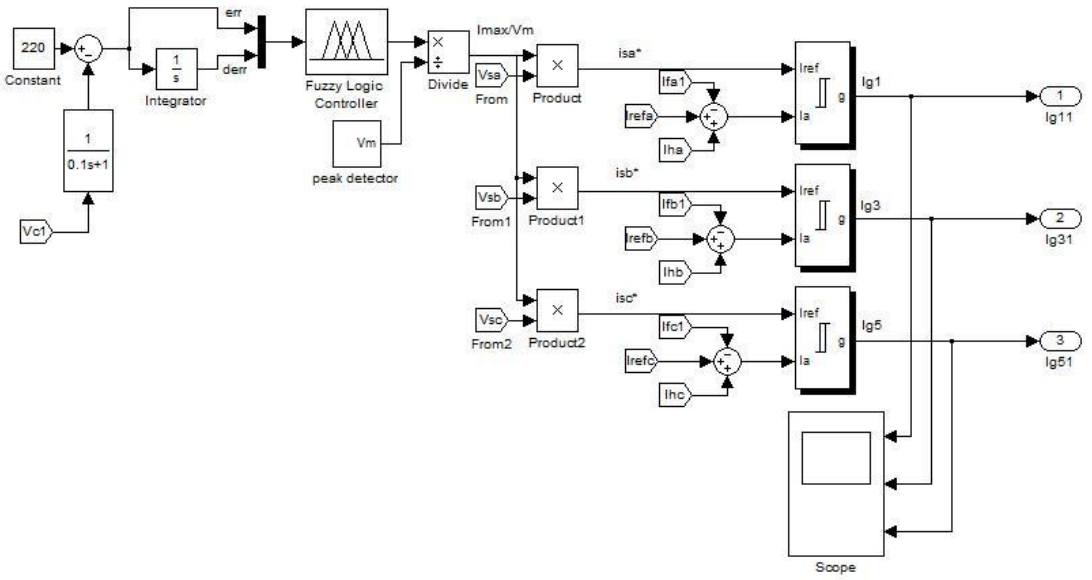
In this case, the error is constructed from a constant value that is compared to the capacitor voltage as the PI controller input signal while the output of the PI controller is the maximum current I_{max}. This maximum current is then divided by the three-phase peak value V_m, and then multiplied with every phase voltage, V_{sa},V_{sb} and V_{sc} to get the reference current for every phase. The sum of the reference current with harmonic current is subtracted from the compensated current that is produced for every phase and compared with the reference current, I_{sa}^*, I_{sb}^* *and* I_{sc}^* at the hysteresis band controller. Then, the hysteresis pulse signal is generated to trigger the IGBT gate I_{g1}, I_{g3} and I_{g5} with its complement.

3.6.2 Fuzzy PI Controller

A Fuzzy PI controller is proposed to monitor the hysteresis current controller as shown in Figure 3.8 for both feedback and feedforward shunt APF. In general, a Fuzzy logic controller must have two inputs, error (*err*) and change of error (*derr*) to create the fuzzy rule. The stability of this control system depends on the number of rules that are created.



(a)



(b)

Figure 3.8 Fuzzy PI controller of the HCC for the shunt APF (a) Feedforward (b) Feedback

Three types of fuzzy rules have been considered as shown in Table 3.1.

Table 3.1 Fuzzy rules (a) 9 (b) 25 (c) 81

derr \ err	N	Z	P
N	NM	NS	PS
Z	NS	Z	PS
P	NS	PS	PM

(a)

derr \ err	NM	NS	Z	PS	PM
NM	NB	NL	NM	NS	Z
NS	NL	NM	NS	Z	PS
Z	NM	NS	Z	PS	PM
PS	NS	Z	PS	PM	PL
PM	Z	PS	PM	PL	PB

(b)

derr \ err	NB	NL	NM	NS	Z	PS	PM	PL	PB
NB	NB	NB	NB	NB	NB	NL	NM	NS	Z
NL	NB	NB	NB	NB	NL	NM	NS	Z	PS
NM	NB	NB	NB	NL	NM	NS	Z	PS	PM
NS	NB	NB	NL	NM	NS	Z	PS	PM	PL
Z	NB	NL	NM	NS	Z	PS	PM	PL	PB
PS	NL	NM	NS	Z	PS	PM	PL	PB	PB
PM	NM	NS	Z	PS	PM	PL	PB	PB	PB
PL	NS	Z	PS	PM	PL	PB	PB	PB	PB
PB	Z	PS	PM	PL	PB	PB	PB	PB	PB

(c)

CHAPTER 4

SIMULATION RESULTS AND ANALYSIS

This chapter presents the simulation results and the related analysis. The simulation of the three-phase system with nonlinear load is run for 1 second. The shunt APF with DP topology is set to mitigate the harmonic currents at t = 0.4s and the load is changed from R in series with L to R in parallel with C or vice versa at t = 0.7s. The simulation is run twice considering increasing and decreasing load as described in the following sections.

4.1 Three-phase Nonlinear Load

The three -phase nonlinear load simulation blocks are as shown in Figure 4.1.

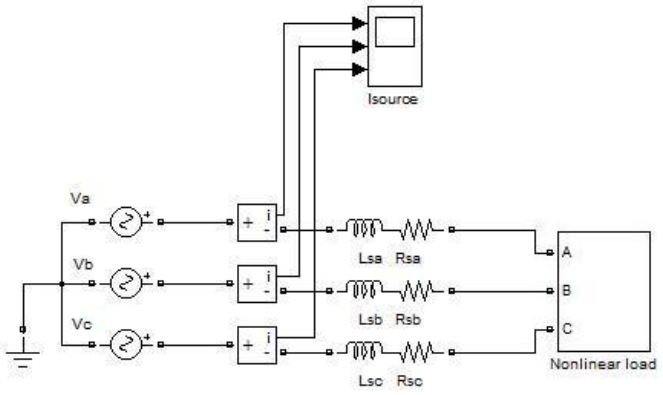
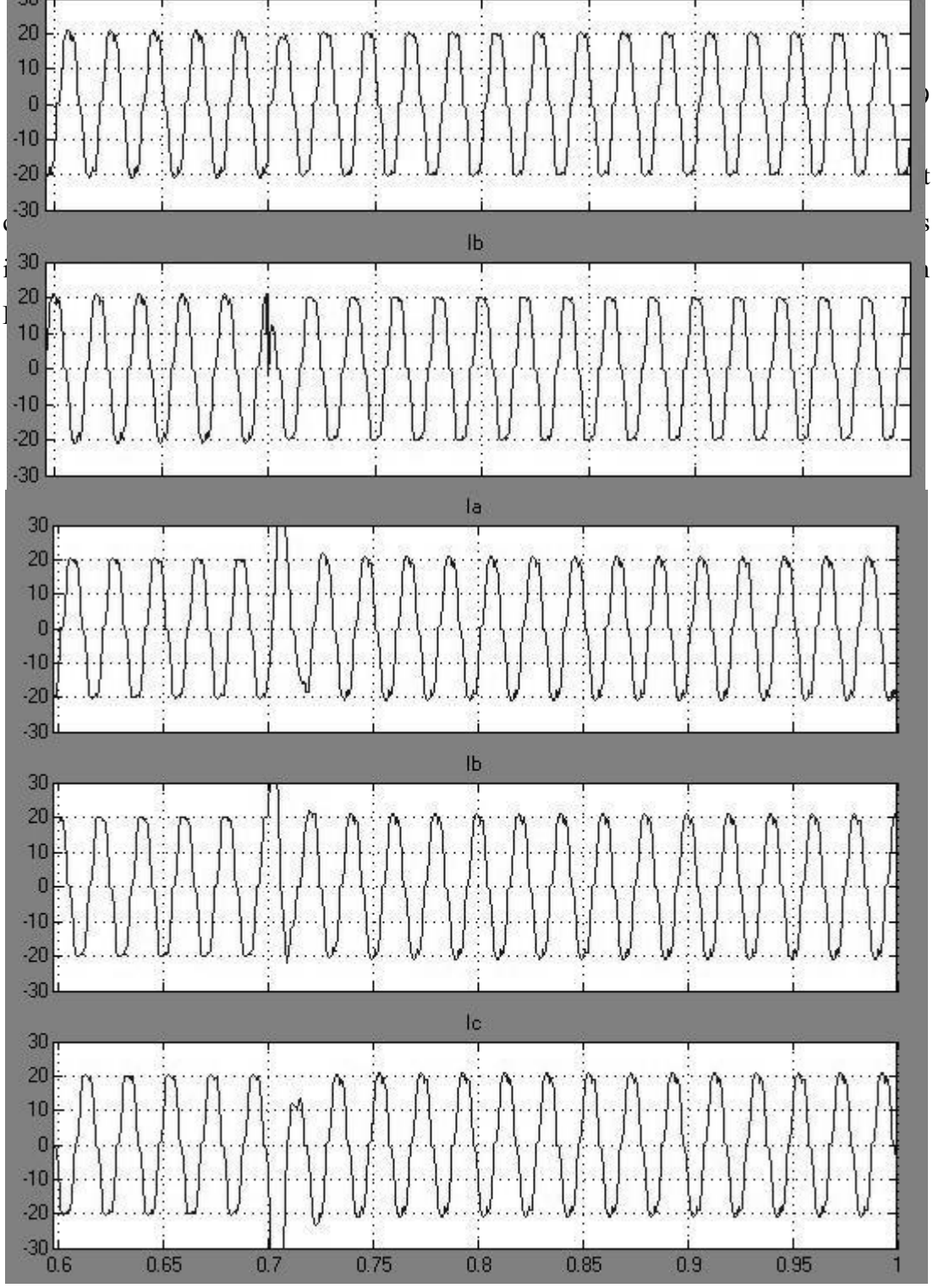


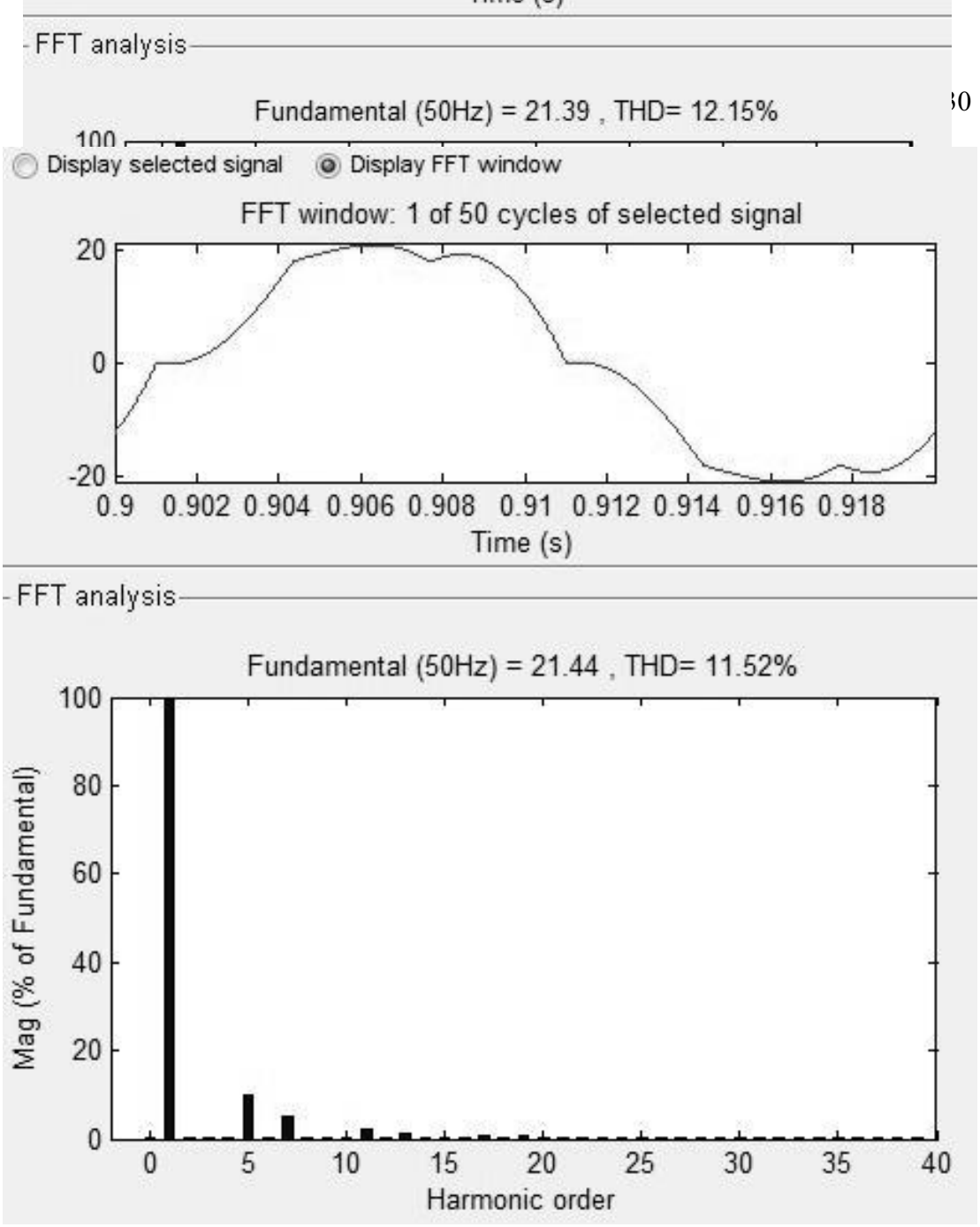
Figure 4.1 Three-phase nonlinear load



(b)

Figure 4.2 Distorted source current, (a) increasing load (b) decreasing load

Figure 4.3 shows the total harmonic distortion (THD) in one cycle starting at t = 0.9s after the load is changed at t = 0.7s. When the load is increased, the THD is 12.15% as shown in Figure 4.3 (a) and when the load is decreased, the THD is 11.52% as shown in Figure 4.3 (b).



(b)

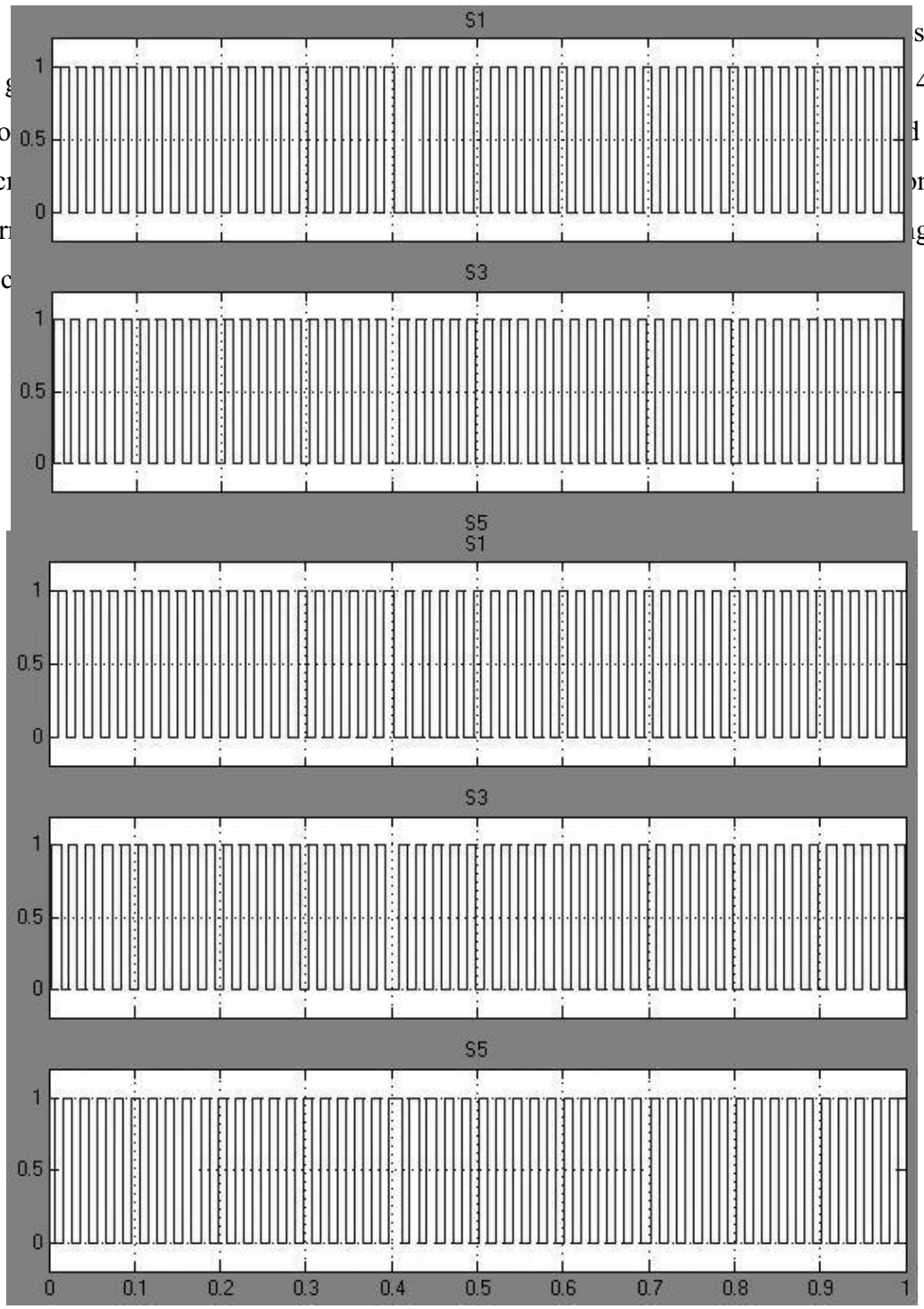
Figure 4.3 Percent THD when (a) load is increased (b) load is decreased

4.2 Three-phase Nonlinear Load with Compensation

When the shunt APF with DP topology is connected to the three-phase power system feeding the nonlinear load, the harmonic currents is set to mitigate at t = 0.4s. First, the PI controller is used with HCC to generate the switching signals. Then the Fuzzy PI controller is used with HCC as an improvement of the control method to generate the switching signals.

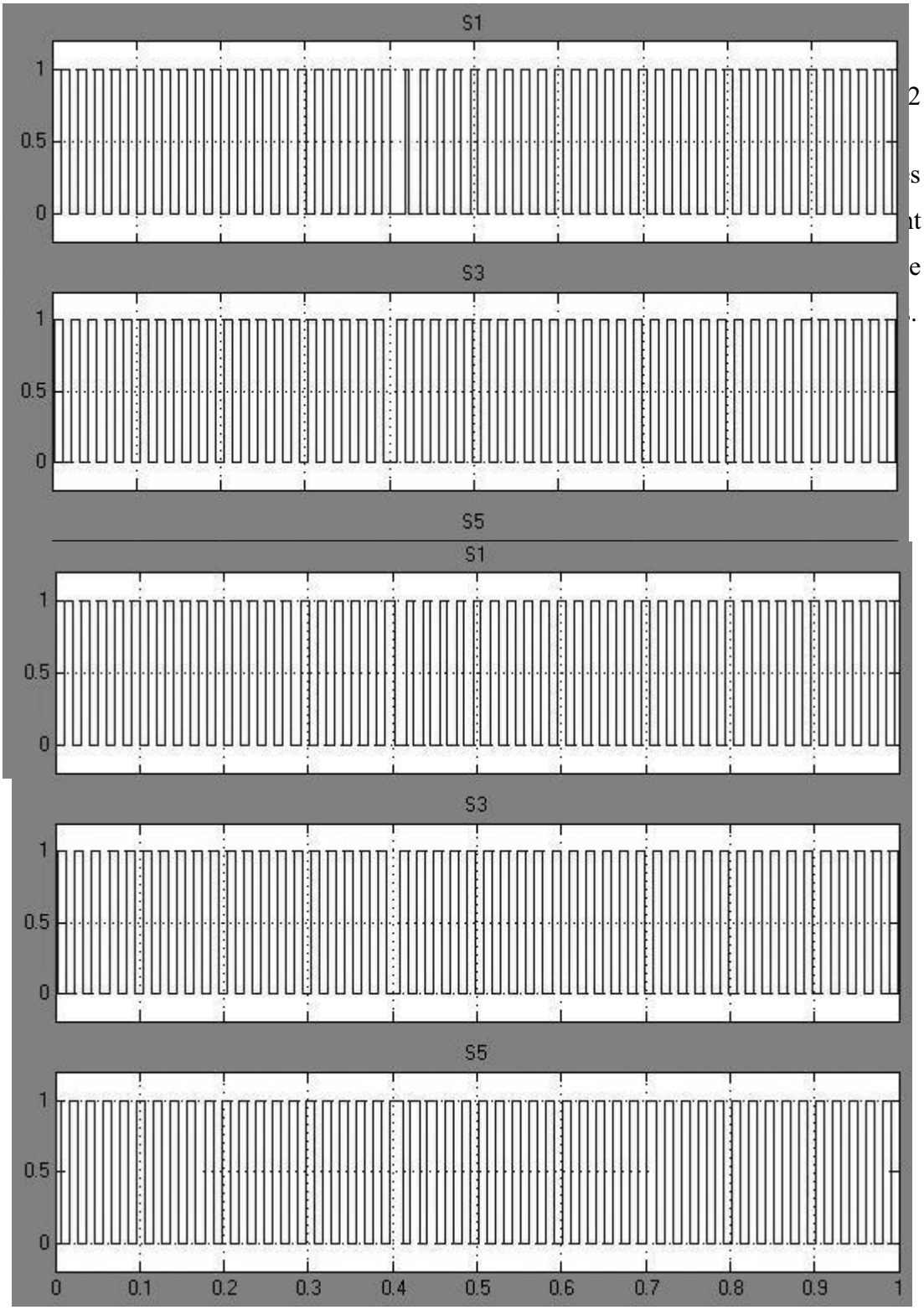
4.2.1 PI Controller

sed
to g 4.4
sho d is
incr onic
curr gly
to c



(b)

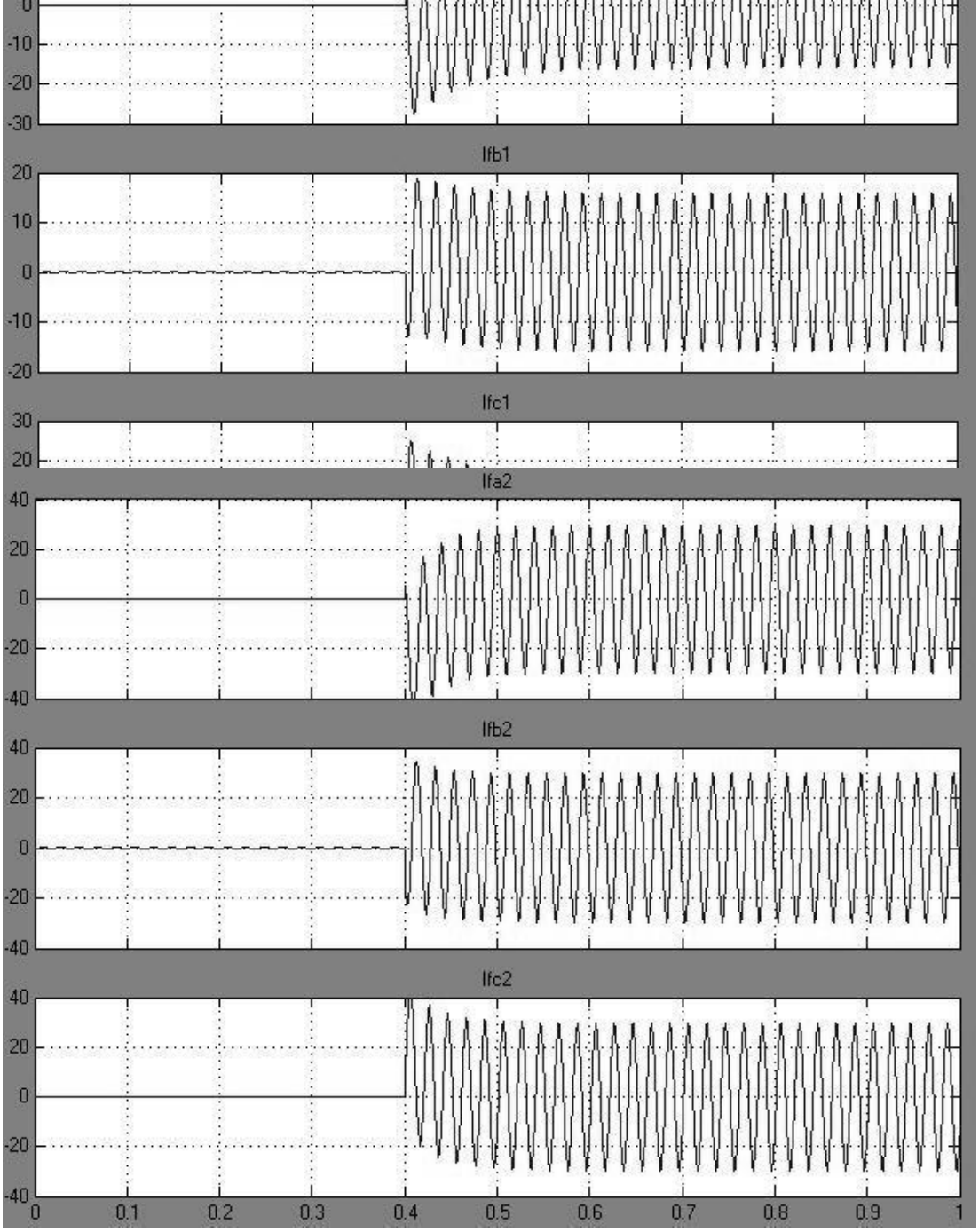
Figure 4.4 Switching signals of the shunt APF with DP topology when the load is increased (a) feedback (b) feedforward



(b)

Figure 4.5 Switching signals of the shunt APF with DP topology when the load is decreased (a) feedback (b) feedforward

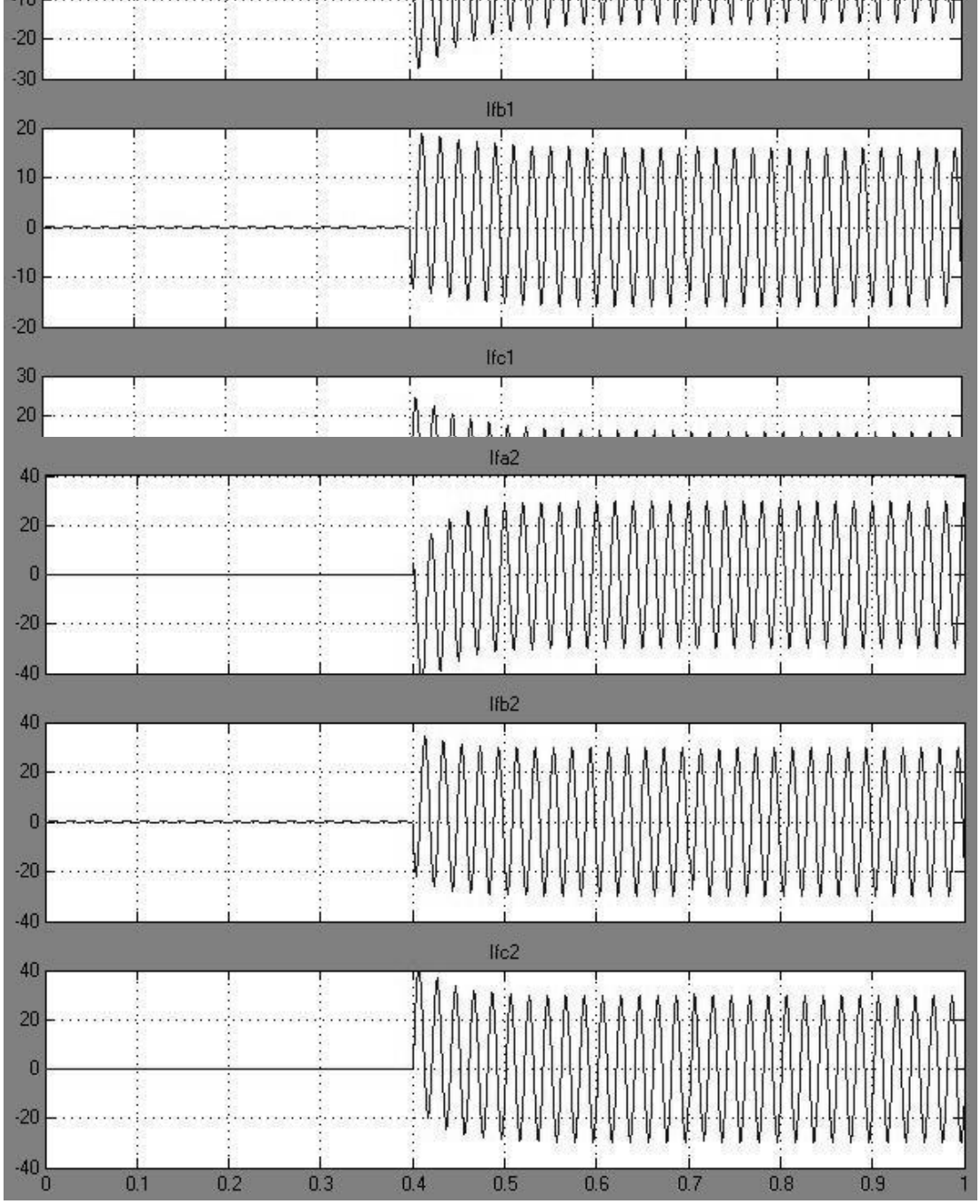
Figure 4.6 shows the compensated current when the shunt APF is connected to the power system and the load is increased. The shunt APF is set to mitigate the harmonics current at $t = 0.4$s.



(b)

Figure 4.6 Compensation current when the load is increased for the shunt APF with DP topology (a) feedback (b) feedforward

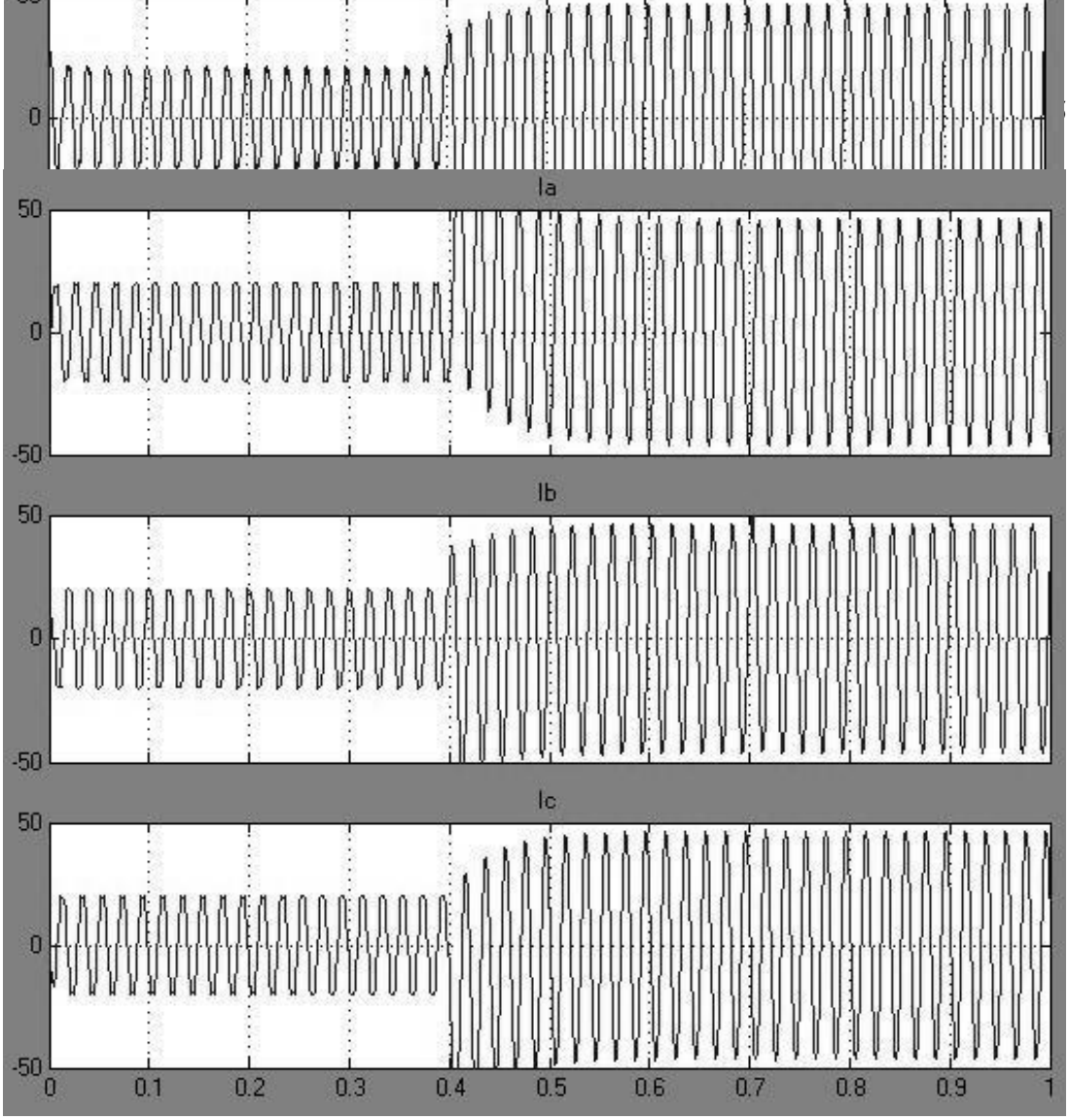
Figure 4.7 shows the compensated current when the shunt APF is connected to the power system and the load is reduced. The shunt APF is set to mitigate the harmonics current at $t = 0.4$s.



(b)

Figure 4.7 Compensation current when the load is decreased for the shunt APF with DP topology (a) feedback (b) feedforward

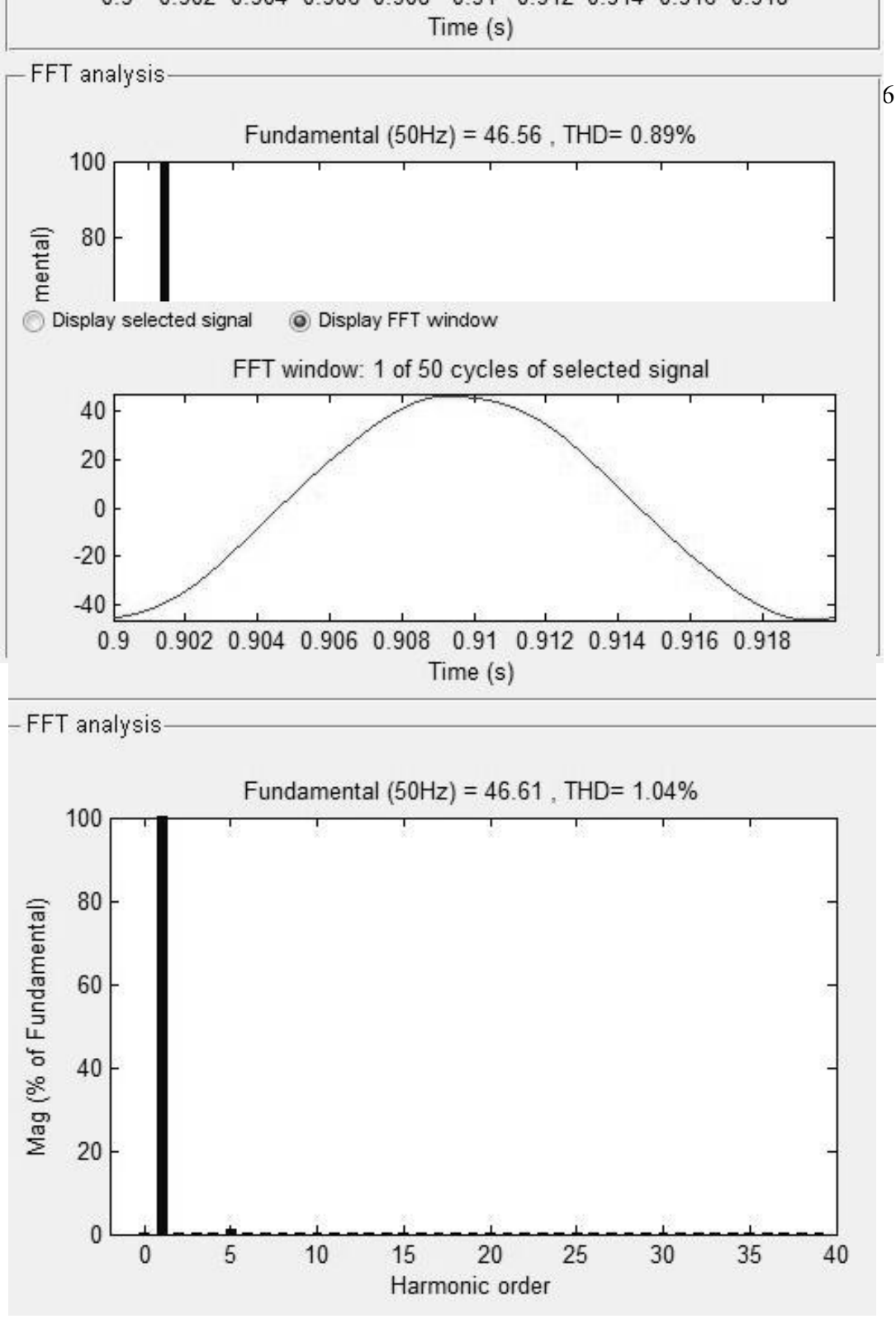
Figure 4.8 shows the source current when the compensated current is injected to the three-phase line at t = 0.4s and the load is changed at t = 0.7s.



(b)

Figure 4.8 Source current with compensation when (a) load is increased (b) load is decreased

Figure 4.9 shows the THD in one cycle starting at t = 0.9s when the load is changed at t = 0.7s. When the load is increased, the THD is 0.89% as shown in Figure 4.9 (a) and when the load is decreased the THD is 1.04% as shown in Figure 4.9 (b).



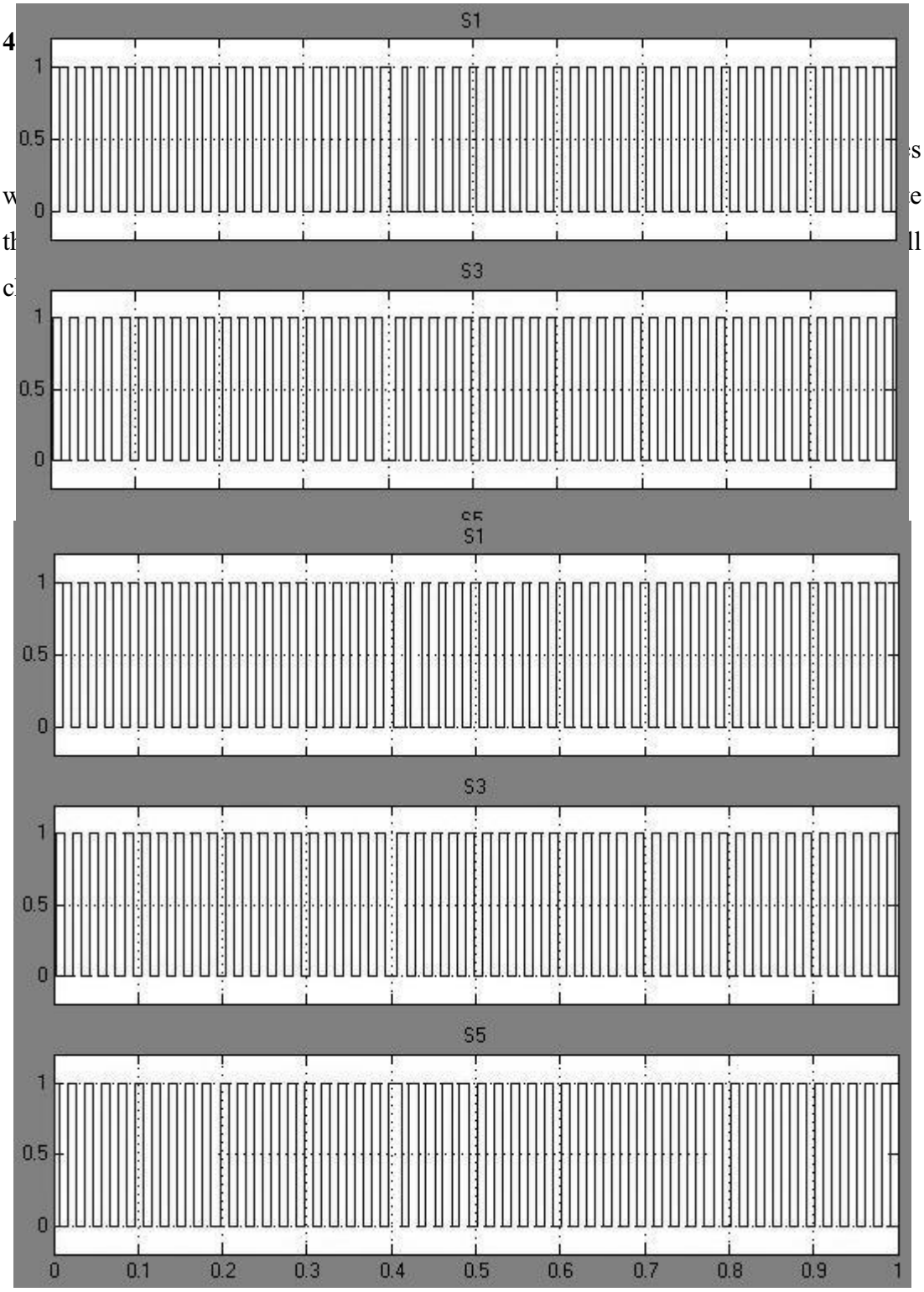
(b)

Figure 4.9 Percent THD when (a) load is increased (b) load is decreased

4.2.2 Fuzzy PI Controller

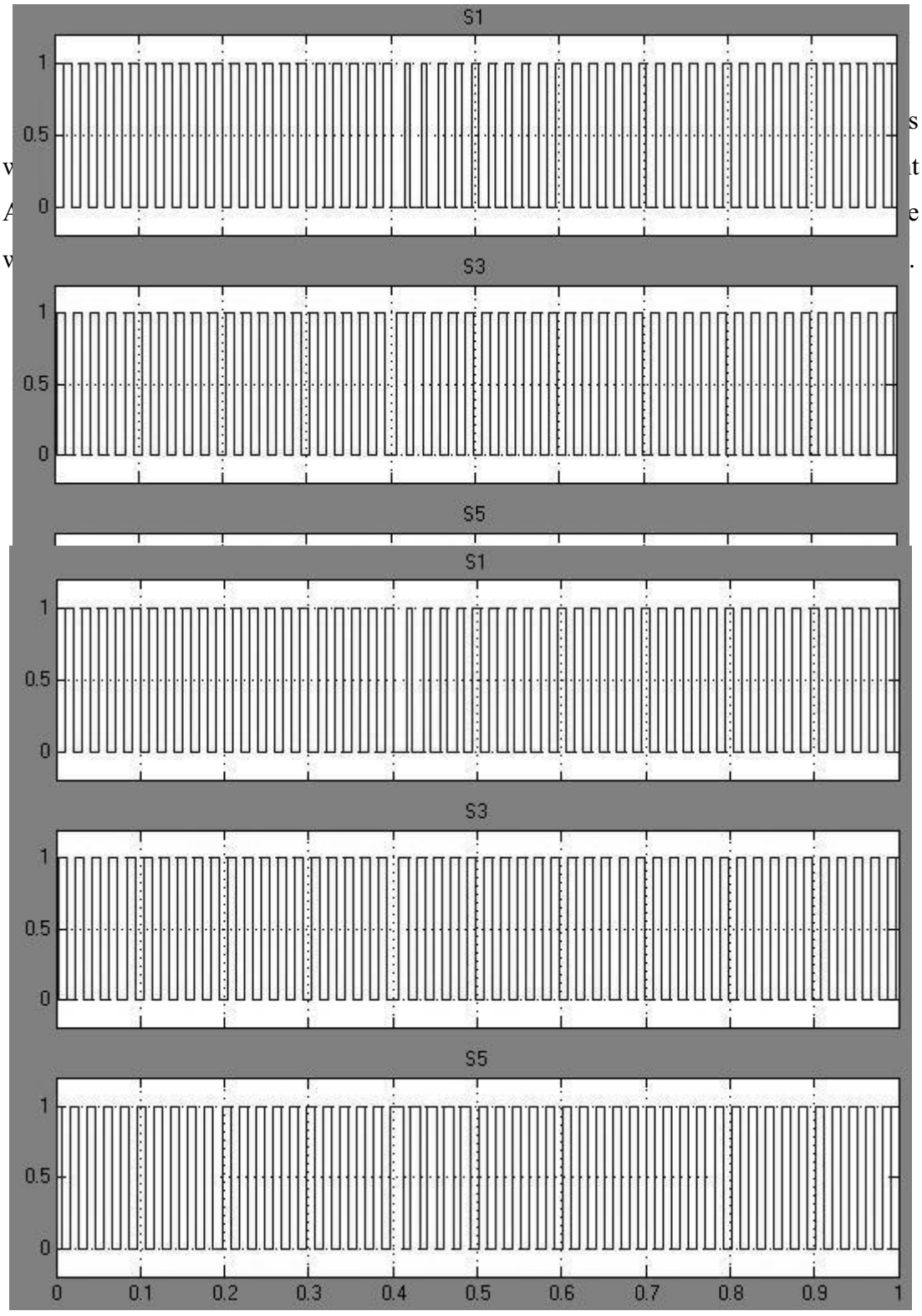
In Chapter III, the simulation design of a Fuzzy PI controller for HCC is discussed to generate the switching signals of the shunt APF with DP topology. Three different types of fuzzy rules have been considered for the Fuzzy PI controller to generate the switching signals for the power devices.

4



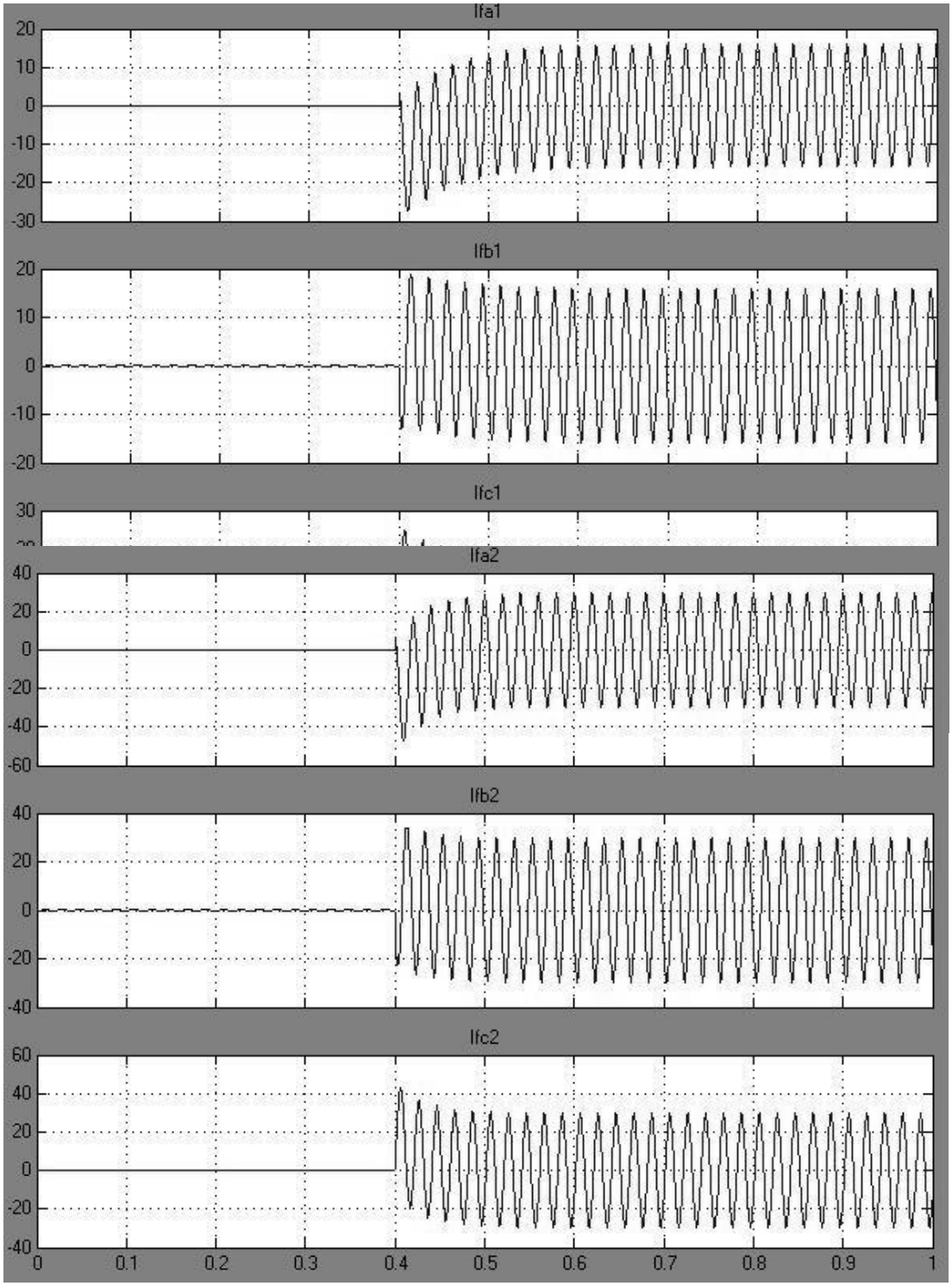
(b)

Figure 4.10 Switching signals of the shunt APF with DP topology when the load



(b)

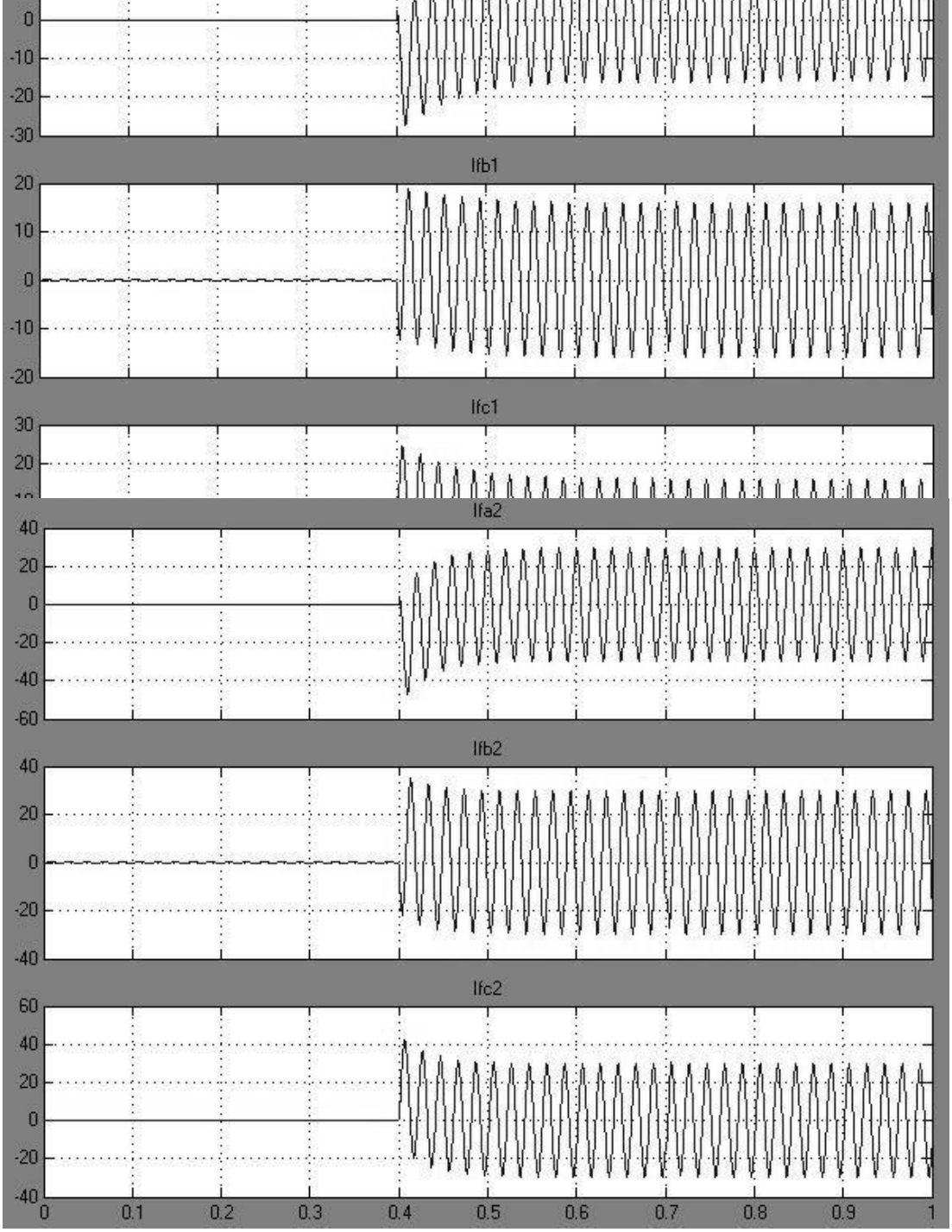
Figure 4.11 Switching signals of the shunt APF with DP topology when the load is decreased (a) feedback (b) feedforward



(b)

Figure 4.12 Compensation current when the load is increased for the shunt APF with DP topology (a) feedback (b) feedforward

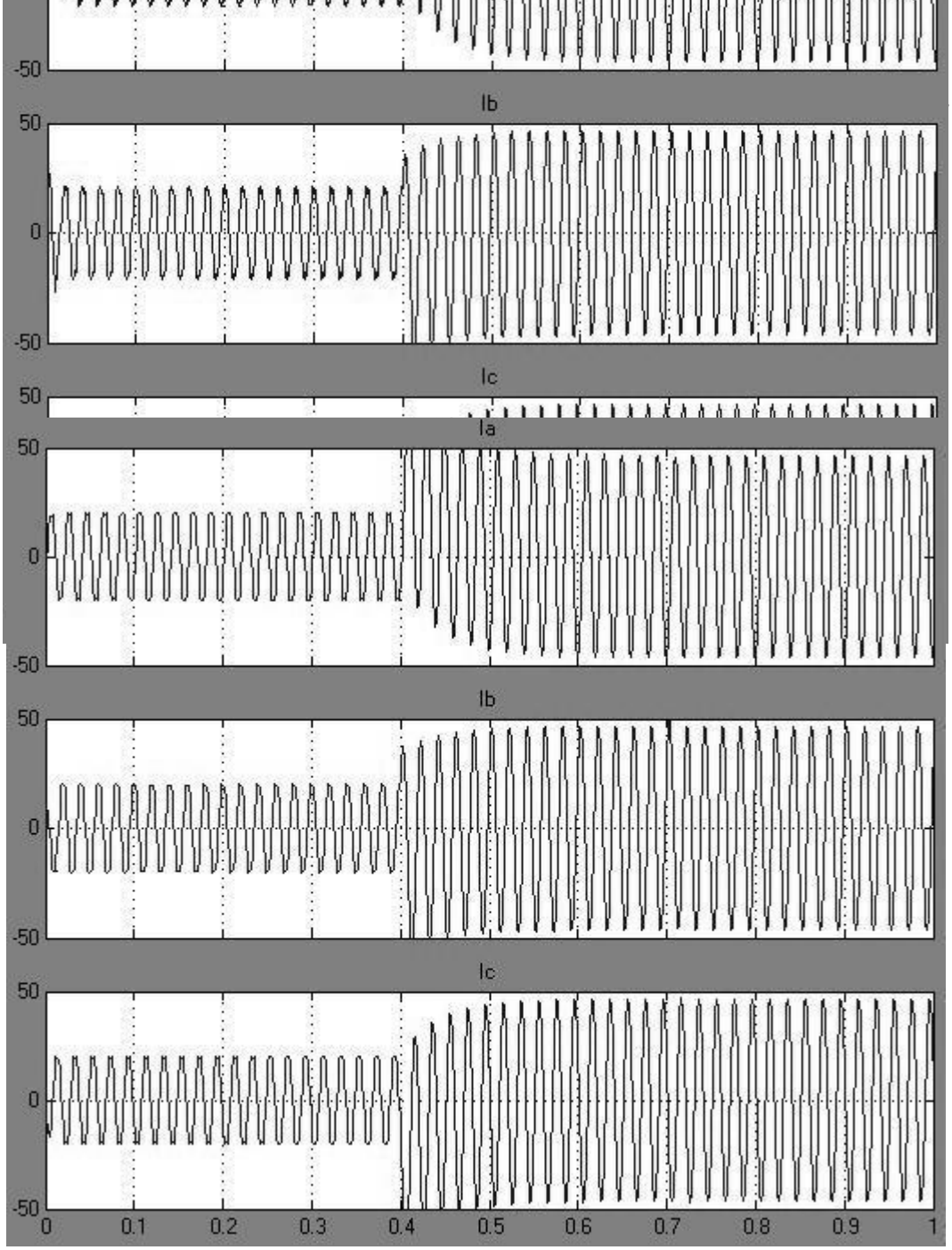
Figure 4.13 shows the compensated current when the shunt APF is connected to the power system and the load is decreased. The shunt APF is set to mitigate the harmonics current at $t = 0.4$ s.



(b)

Figure 4.13 Compensation current when the load is decreased for the shunt APF with DP topology (a) feedback (b) feedforward

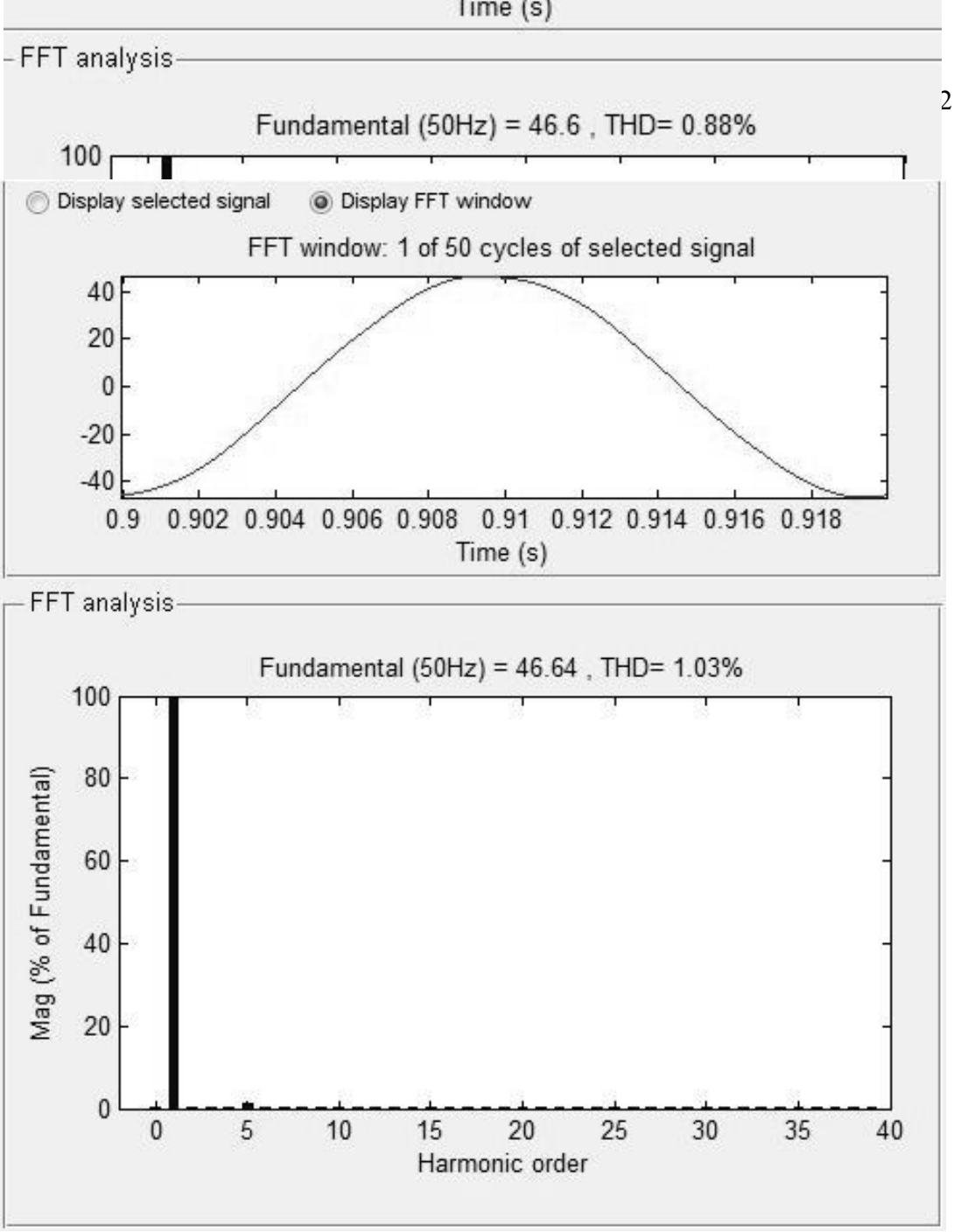
Figure 4.14 shows the source current when the compensated current is injected to the three-phase line at $t = 0.4$ s and the load is changed at $t = 0.7$ s.



(b)

Figure 4.14 Source current with compensation when
(a) load is increased (b) load is decreased

Figure 4.15 shows the THD in one cycle starting at t = 0.9 s when the load is changed at t = 0.7 s. When the load is increased, the THD is 0.88% as shown in Figure 4.9 (a) and when the load is decreased, the THD is 1.03% as shown in Figure 4.9 (b).

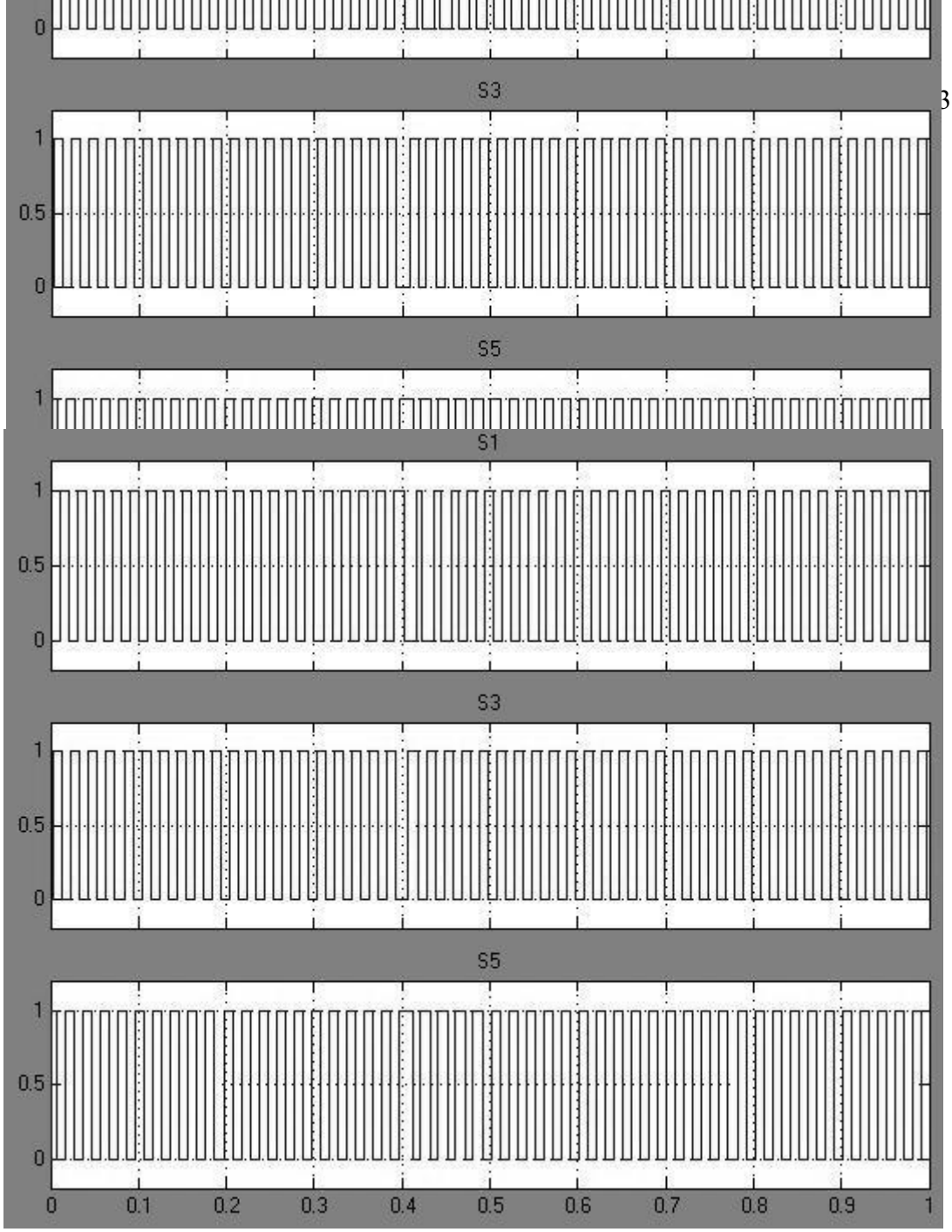


(b)

Figure 4.15 Percent THD when (a) load is increased (b) load is decreased

4.2.2.2 Fuzzy PI Controller with 25 Rules

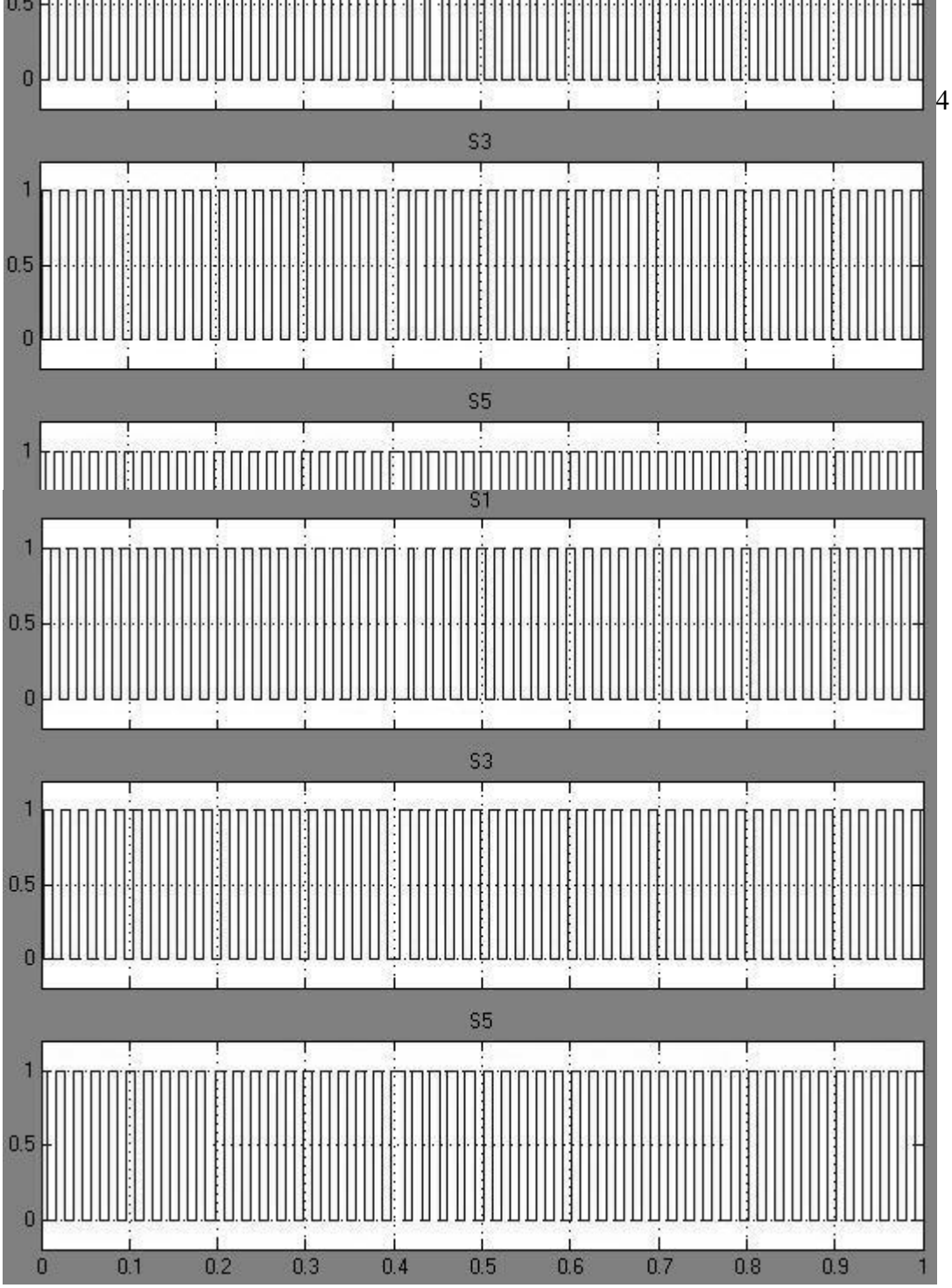
Figure 4.16 shows the switching signal of the DP topology when the load is increase. When the shunt APF with DP topology start to mitigate the harmonic currents at t = 0.4s, the switching signal will change the width to control the power device.



(b)

Figure 4.16 Switching signal when the load is increase for
(a) feedback shunt APF (b) feedforward shunt APF

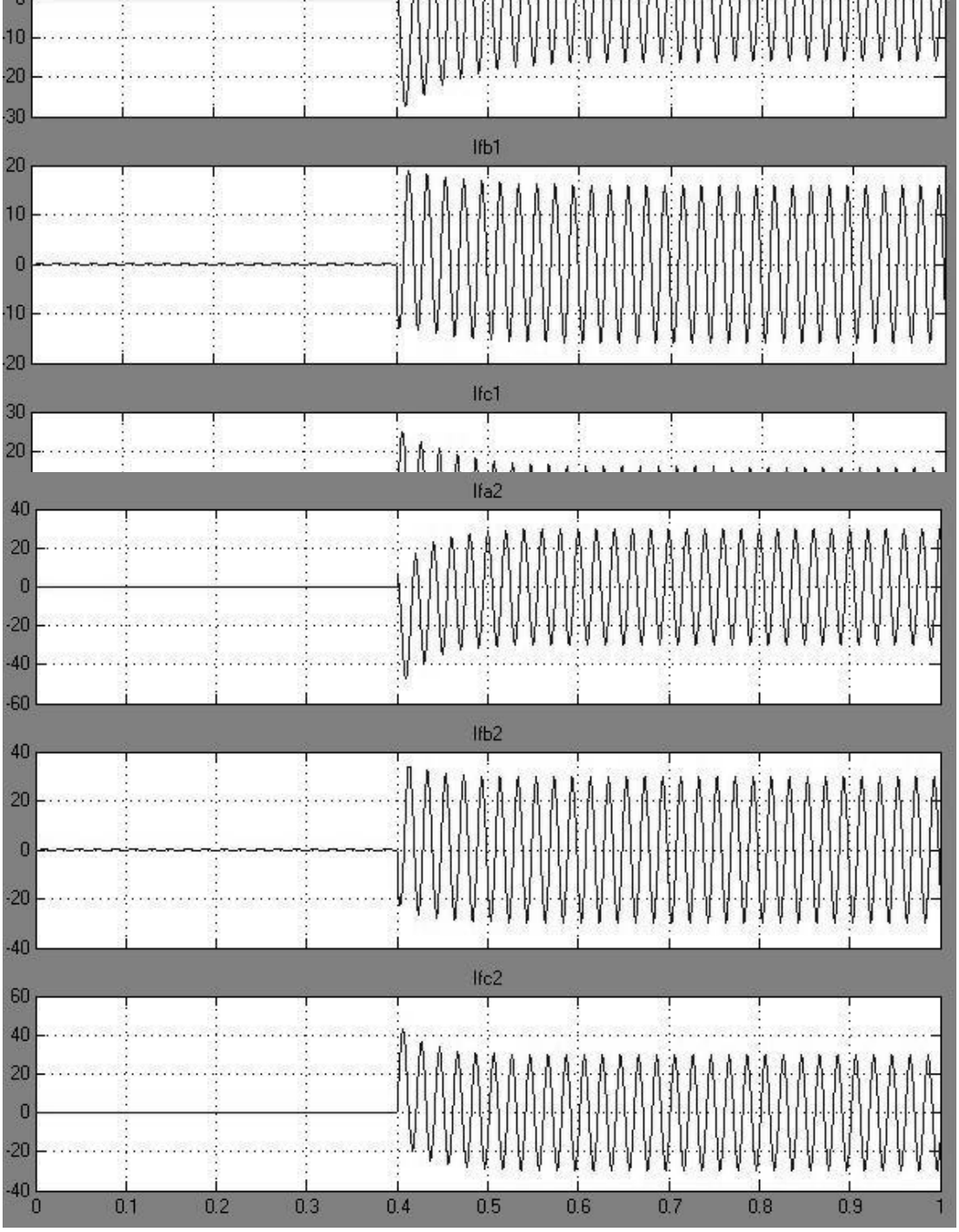
Figure 4.17 shows the switching signal of the DP topology when the load is reduced. When the shunt APF with DP topology start to mitigate the harmonic currents at t = 0.4s, the switching signal will change the width to control the power device.



(b)

Figure 4.17 Switching signal when the load is reduce for
(a) feedback shunt APF (b) feedforward shunt APF

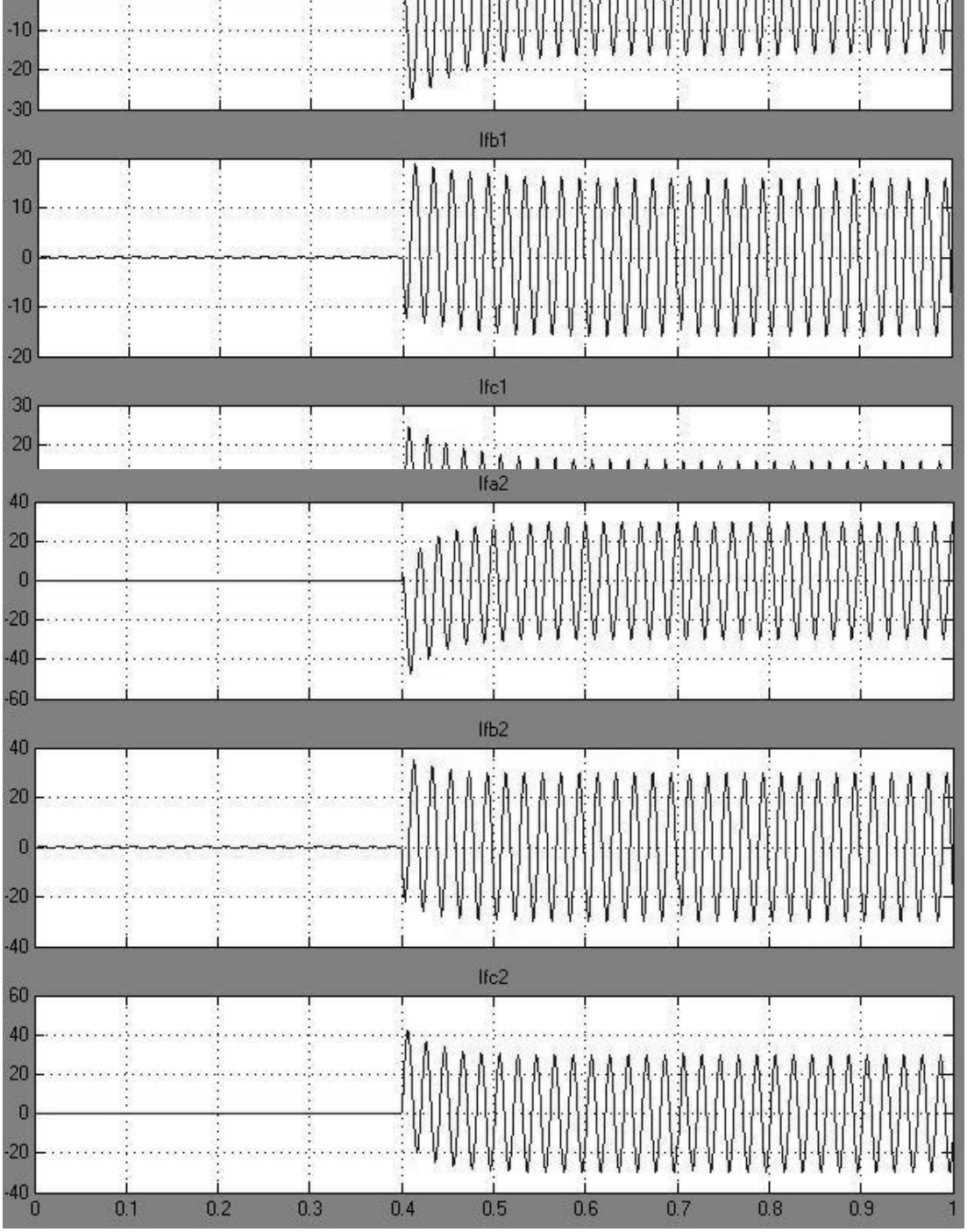
Figure 4.18 shows the compensated current when the shunt APF is connected to the network and the load is increase. Shunt APF will start to mitigate the harmonics current at $t = 0.4$s.



(b)

Figure 4.18 Compensation current when the load is increase for
(a) feedback shunt APF (b) feedforward shunt APF

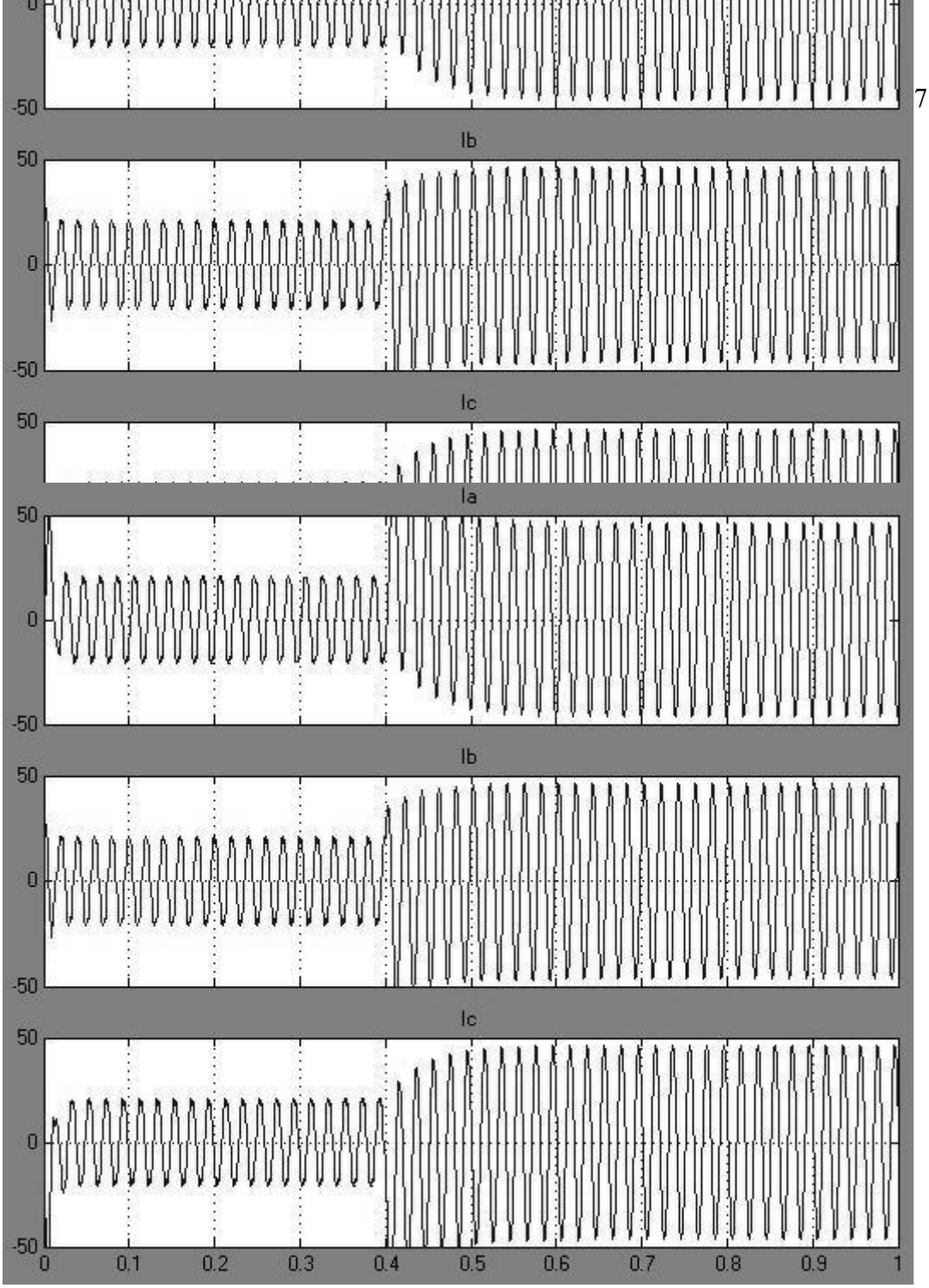
Figure 4.19 shows the compensated current when the shunt APF is connected to the network and the load is reduce. Shunt APF will start to mitigate the harmonics current at t = 0.4s.



(b)

Figure 4.19 Compensation current when the load is reducing for
(a) feedback shunt APF (b) feedforward shunt APF

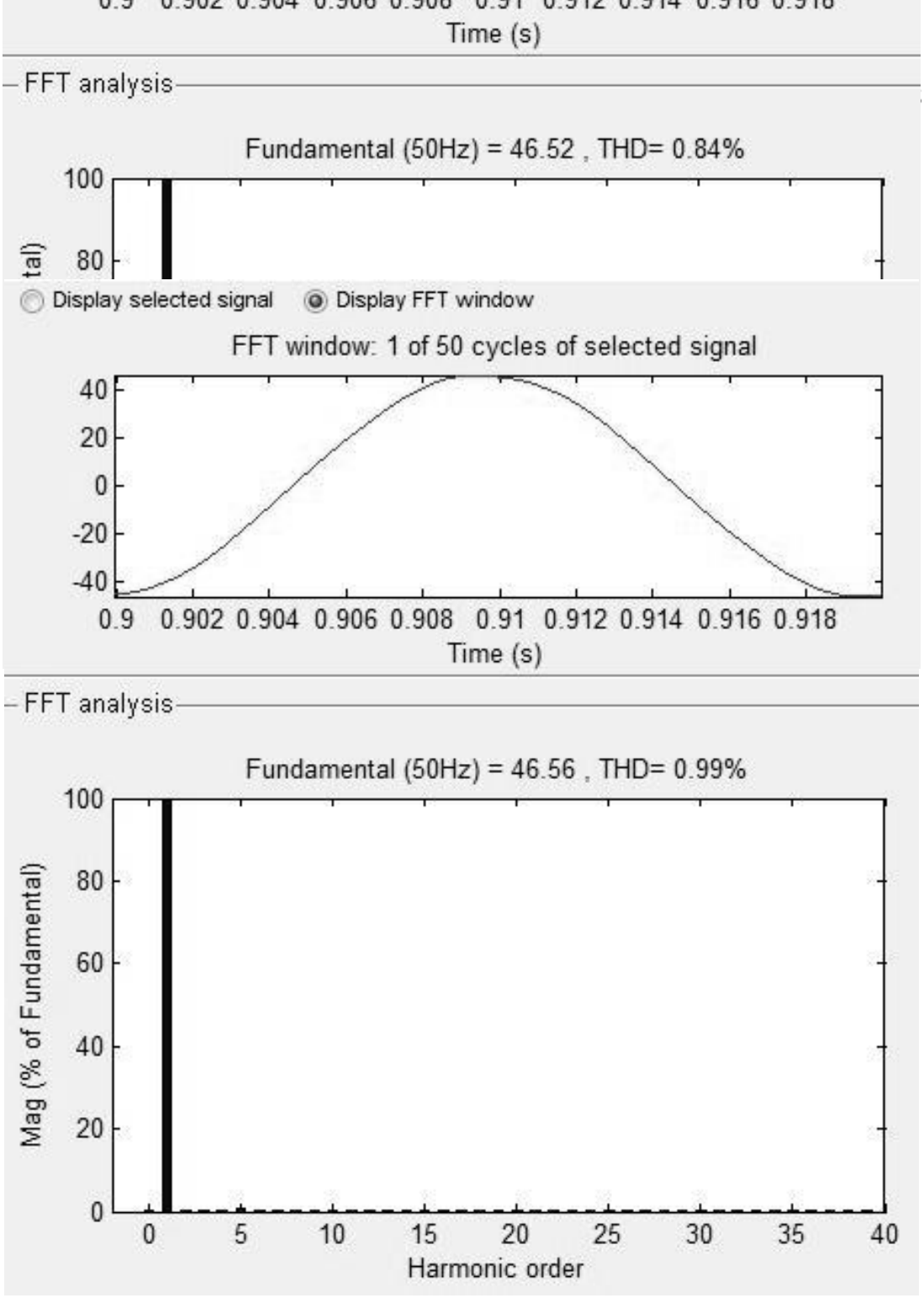
Figure 4.20 shows the source current when the compensated current is injected to the three phase line at t = 0.4s and the load is change at t = 0.7s.



(b)

Figure 4.20 Source current with compensation when
(a) load increase (b) load reduce

Figure 4.21 shows the THD in one cycle started at t = 0.9s when the load change at t = 0.7s. When the load is increase, the THD are 0.84% shown in Figure 4.21 (a) and when the load is reducing, the THD are 0.99% shown in Figure 4.21 (b).

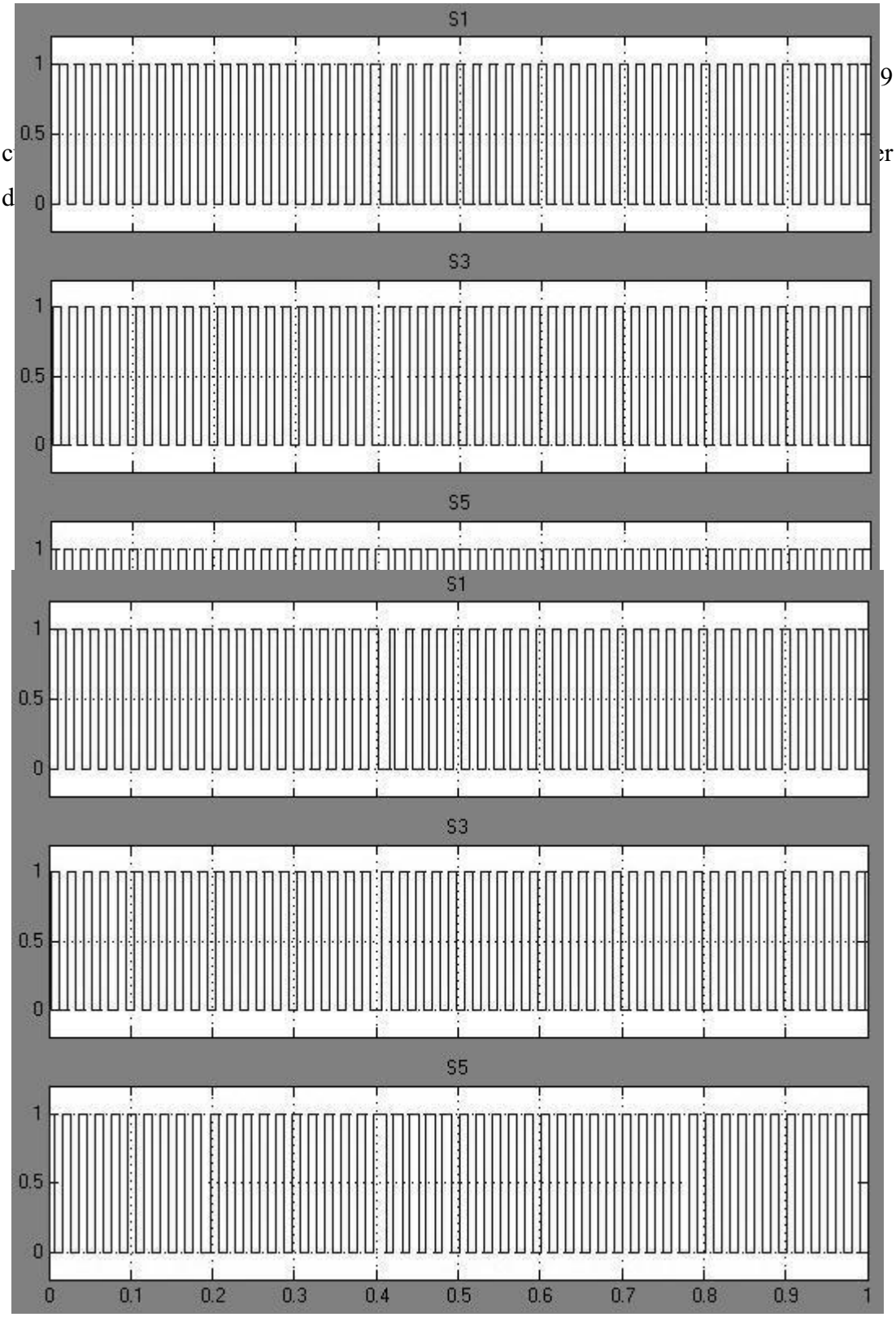


(b)

Figure 4.21 THD when (a) load increase (b) load reduce

4.2.2.3 Fuzzy PI Controller with 81 Rules

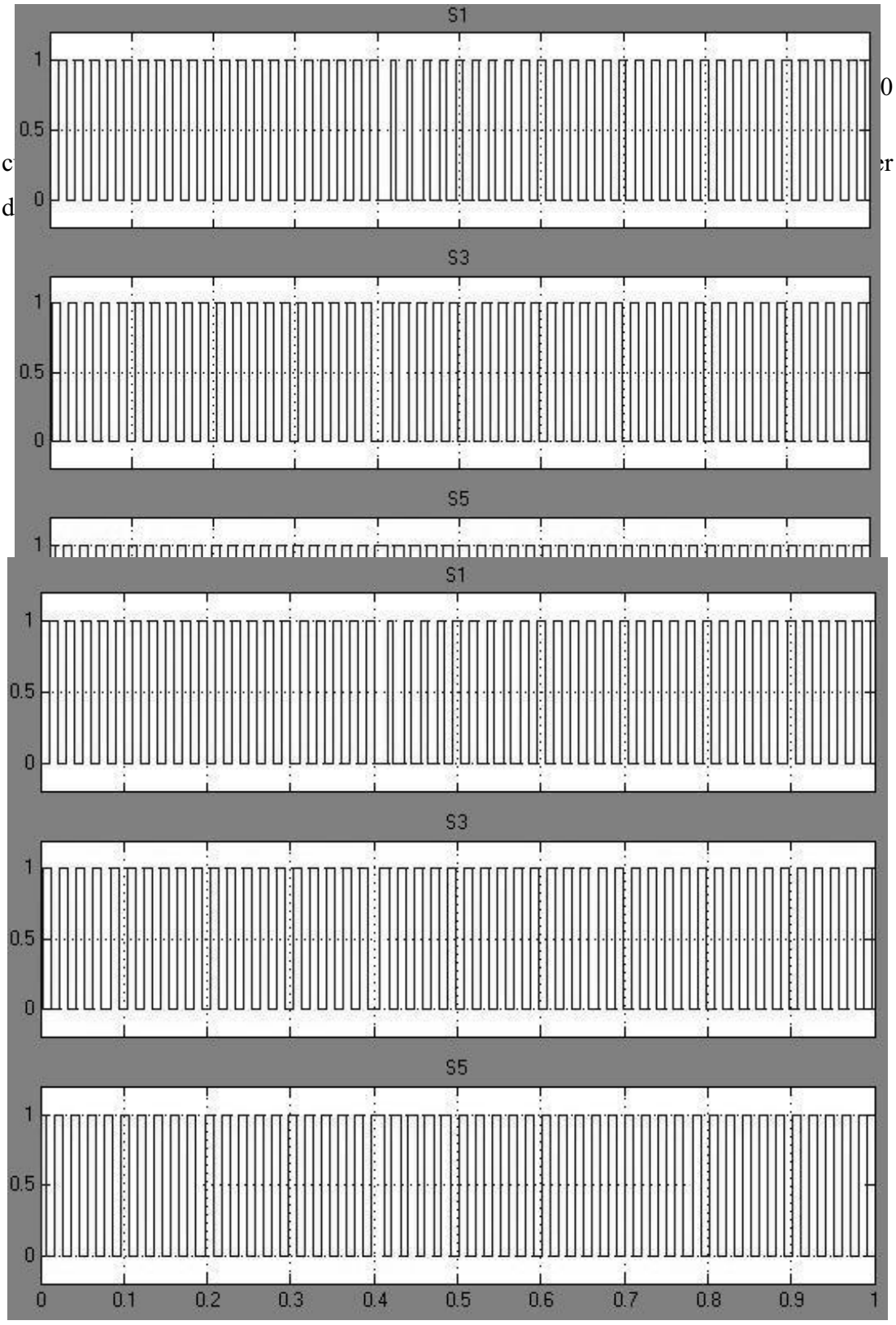
Figure 4.22 shows the switching signal of the DP topology when the load is increase. When the shunt APF with DP topology start to mitigate the harmonic



(b)

Figure 4.22 Switching signal when the load is increase for
(a) feedback shunt APF (b) feedforward shunt APF

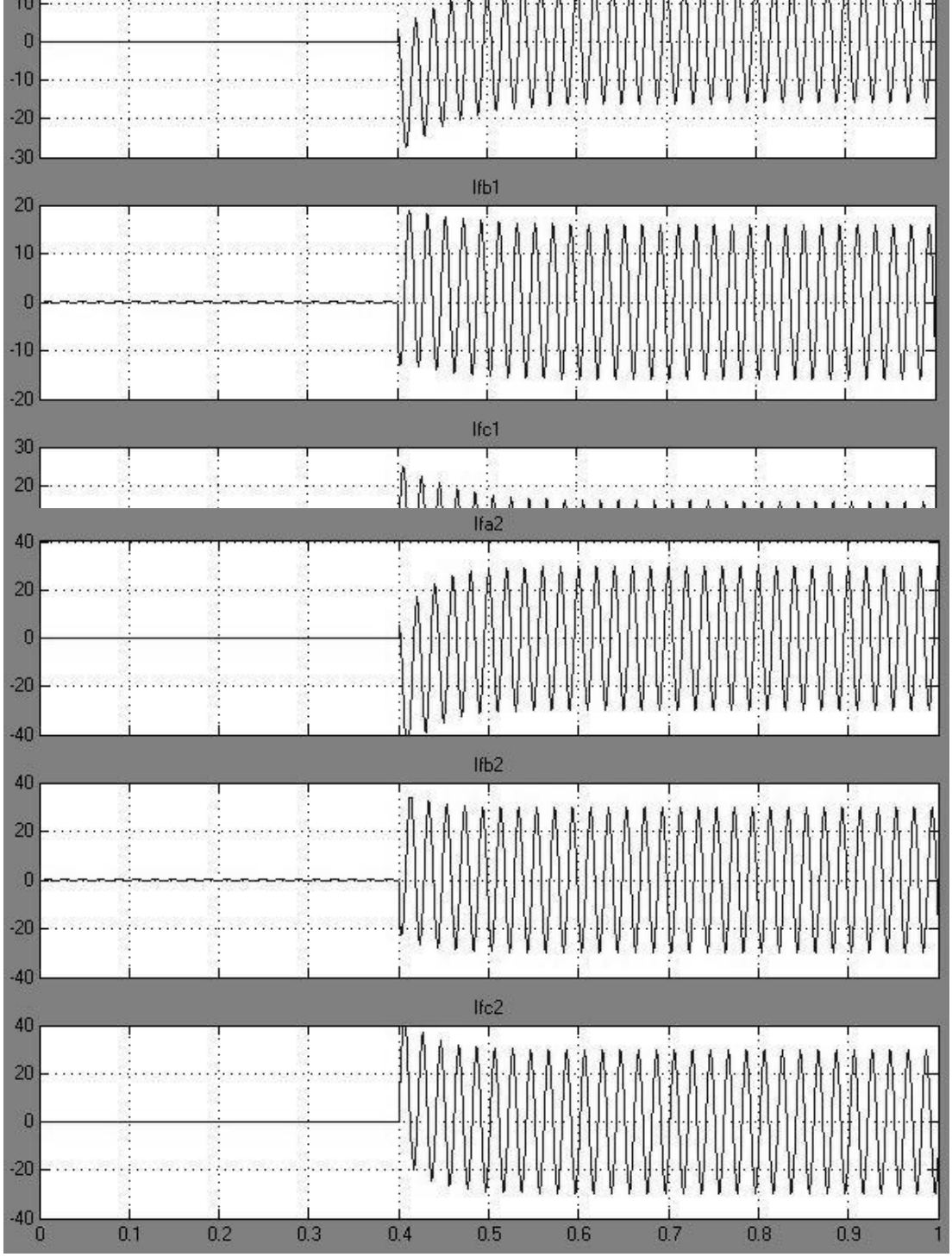
Figure 4.11 shows the switching signal of the DP topology when the load is reduced. When the shunt APF with DP topology start to mitigate the harmonic



(b)

Figure 4.23 Switching signal when the load is reduce for
(a) feedback shunt APF (b) feedforward shunt APF

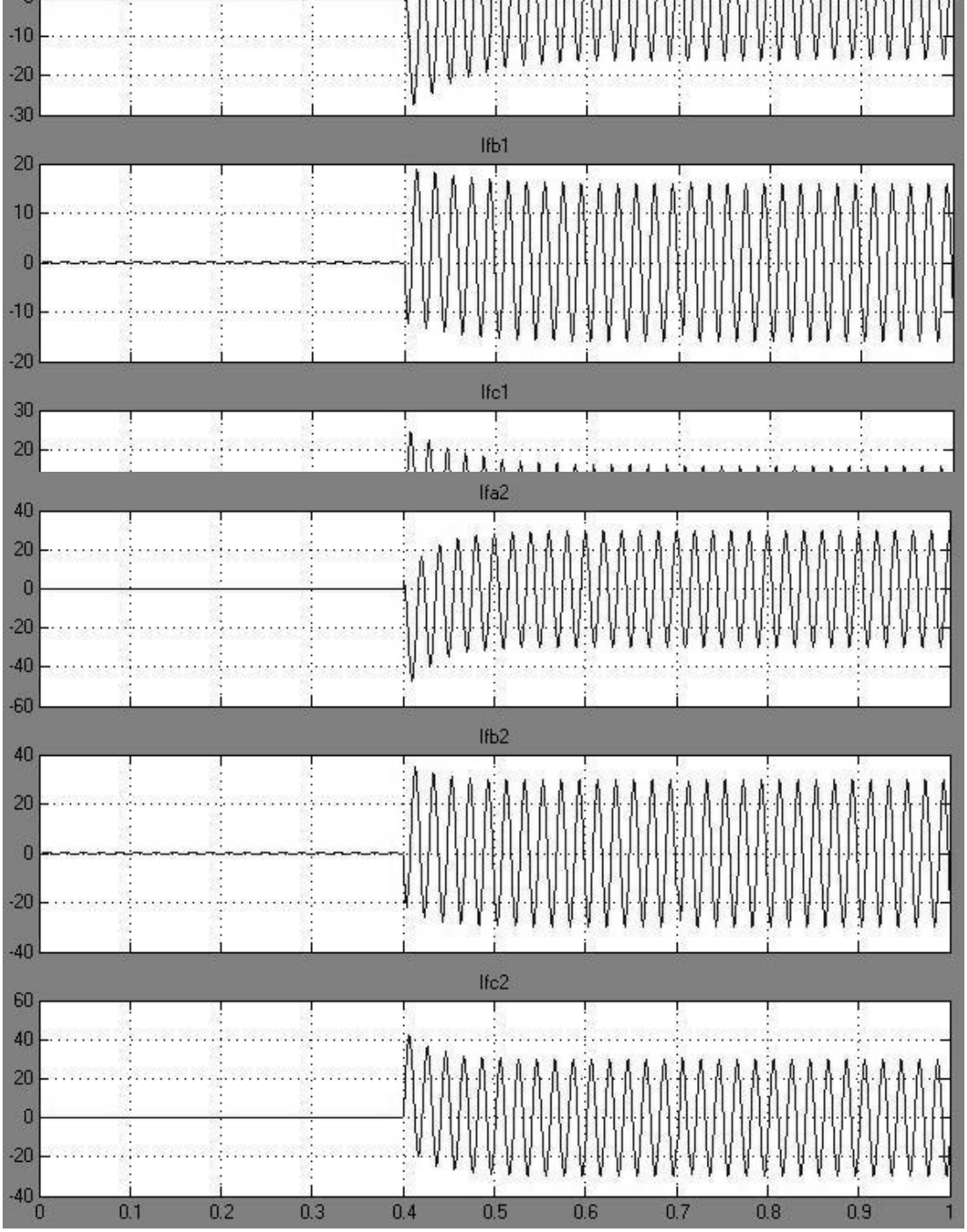
Figure 4.24 shows the compensated current when the shunt APF is connected to the network and the load is increase. Shunt APF will start to mitigate the harmonics current at $t = 0.4$s.



(b)

Figure 4.24 Compensation current when the load is increase for
(a) feedback shunt APF (b) feedforward shunt APF

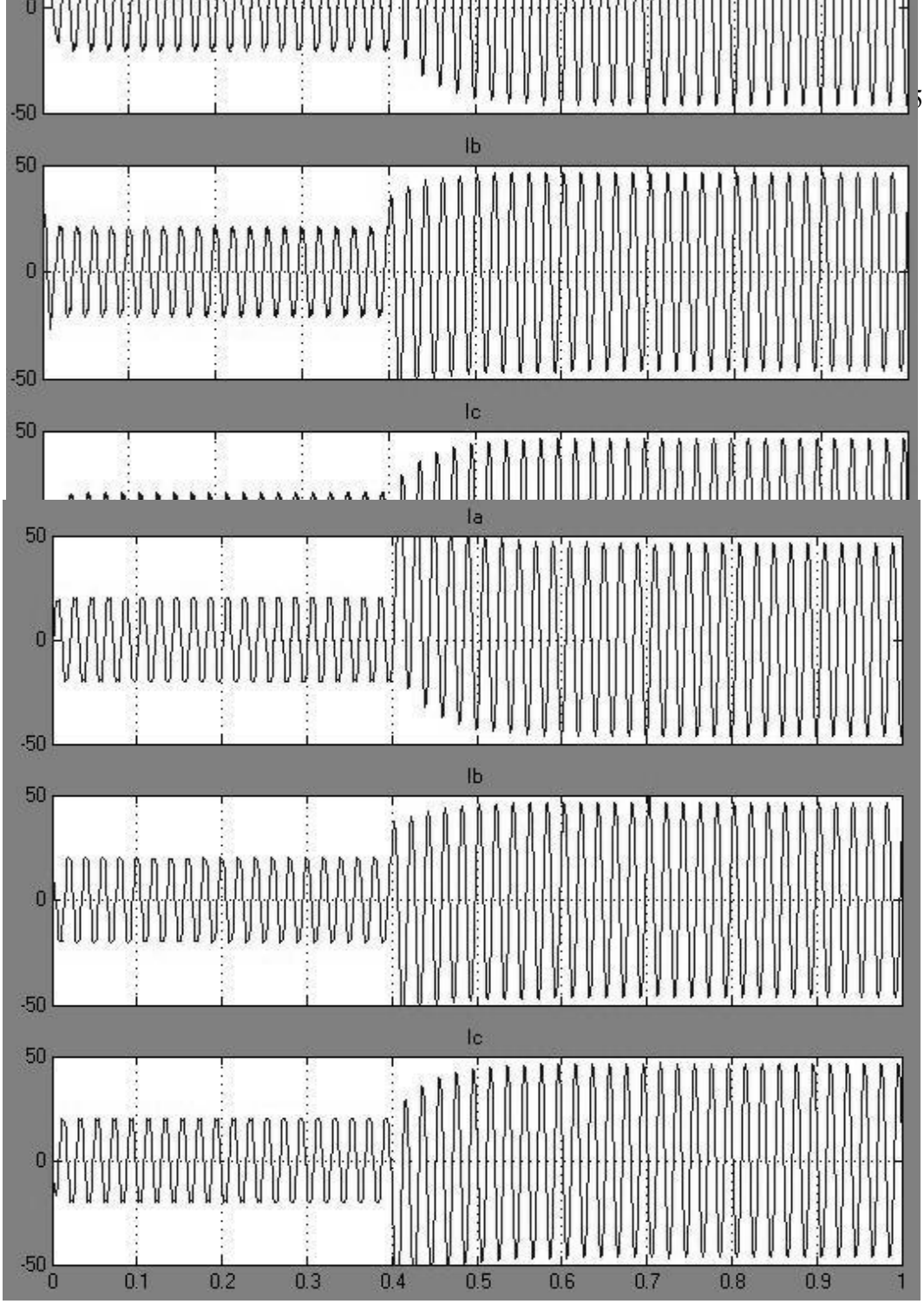
Figure 4.25 shows the compensated current when the shunt APF is connected to the network and the load is reduce. Shunt APF will start to mitigate the harmonics current at t = 0.4s.



(b)

Figure 4.25 Compensation current when the load is reducing for
(a) feedback shunt APF (b) feedforward shunt APF

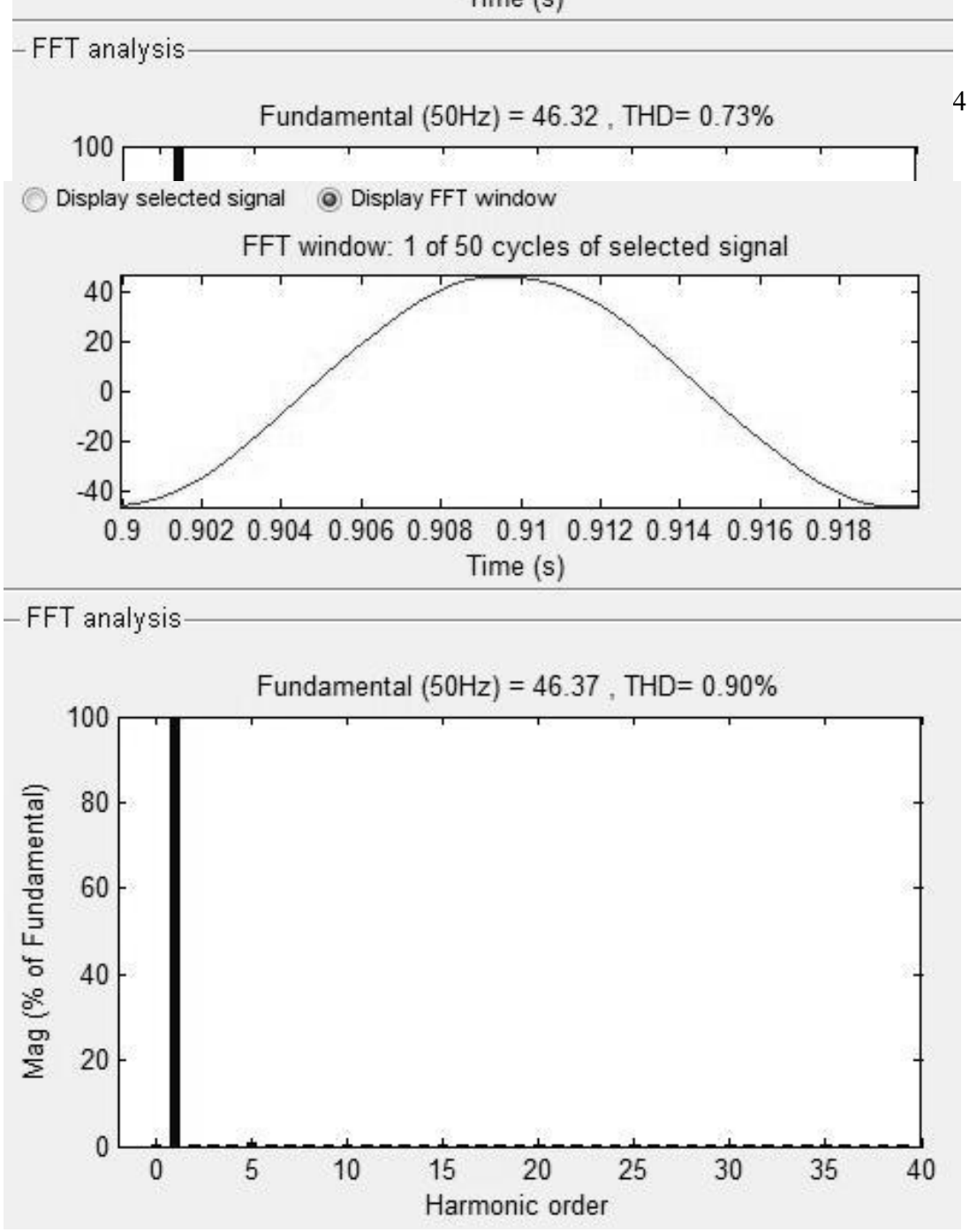
Figure 4.26 shows the source current when the compensated current is injected to the three phase line at t = 0.4s and the load is change at t = 0.7s.



(b)

Figure 4.26 Source current with compensation when
(a) load increase (b) load reduce

Figure 4.27 shows the THD in one cycle started at t = 0.9s when the load change at t = 0.7s. When the load is increase, the THD are 0.73% shown in Figure 4.27 (a) and when the load is reducing, the THD are 0.90% shown in Figure 4.27 (b).



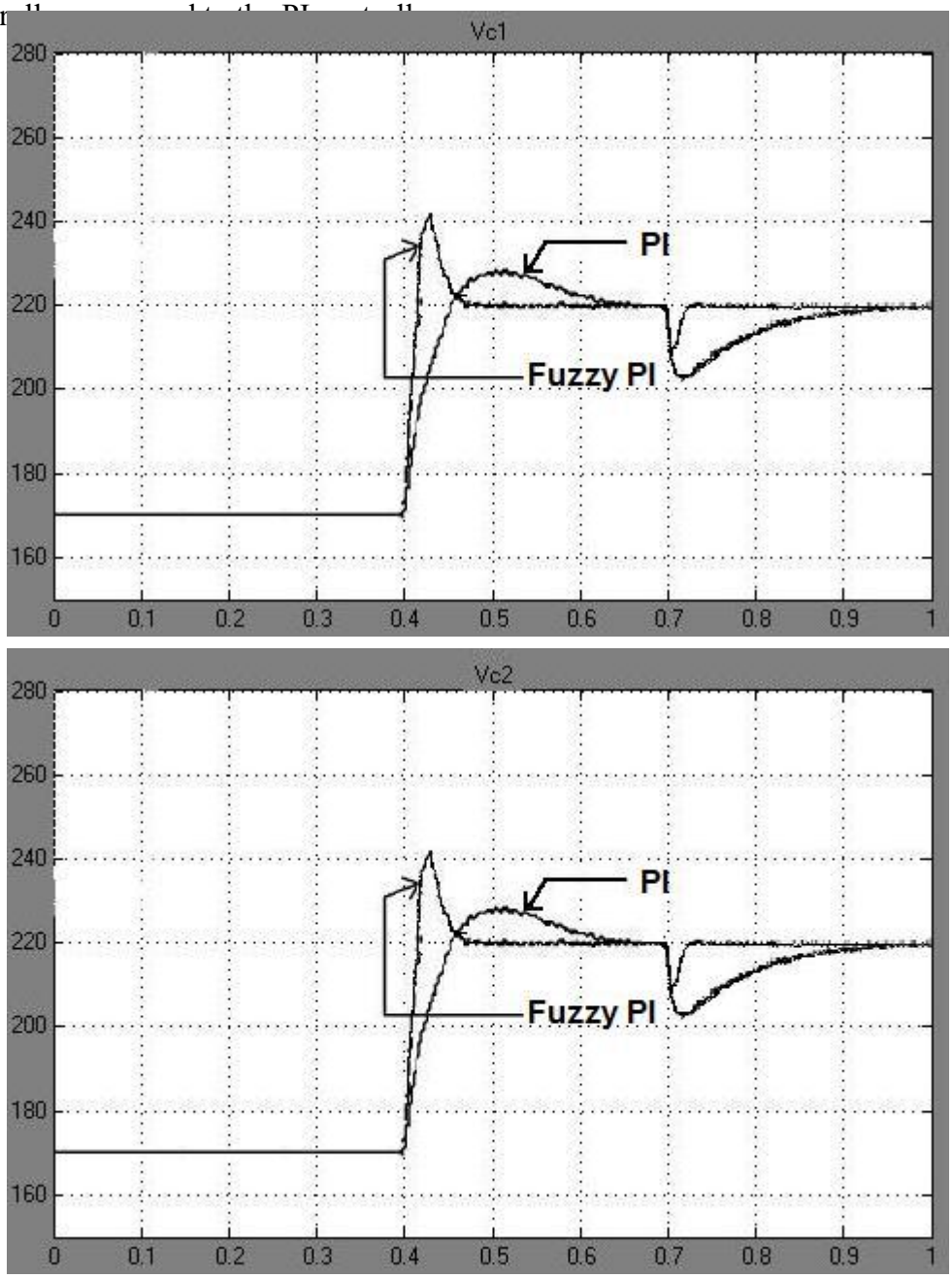
(b)

Figure 4.27 THD when (a) load increase (b) load reduce

4.3 Controller performance

The controller performance depends on the harmonic currents mitigation. The controller performance is considered better when the THD is lower and the response is faster when subjected to load change. The change of error will reduce when the capacitor voltage reaches 220 V since it is used as a reference to generate the error when compared with a constant value of 220.

Figure 4.28 shows the comparison of the capacitor voltage when PI and Fuzzy PI controller (25 rules) with HCC are used in the shunt APF with DP topology when the load is decreased. At t = 0.4 s, when the shunt APF starts to mitigate the harmonic currents, the capacitor voltage reaches 220V faster when using Fuzzy PI contr

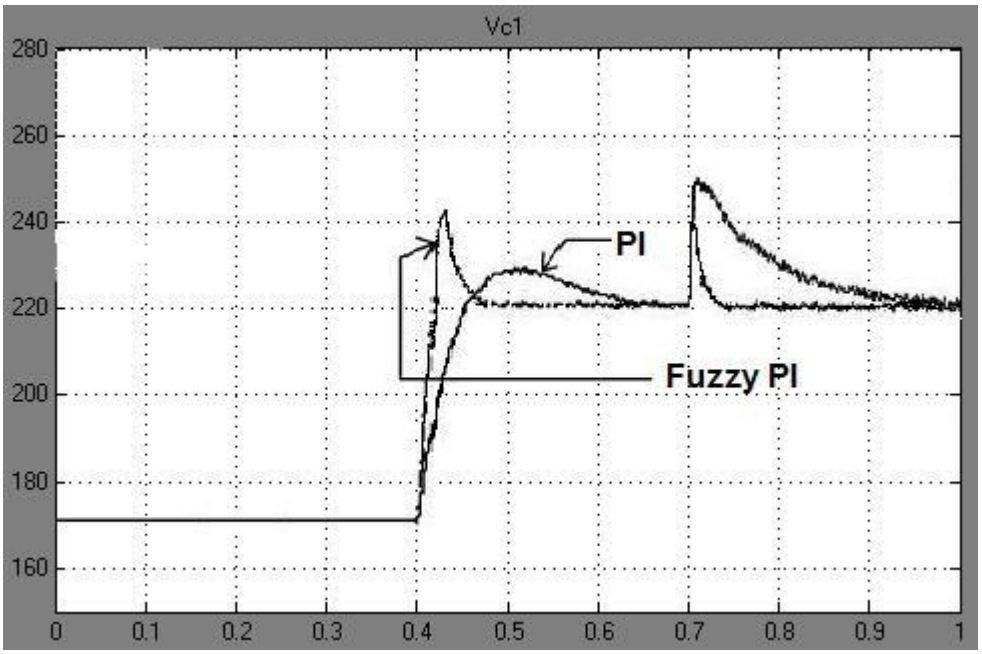


(b)

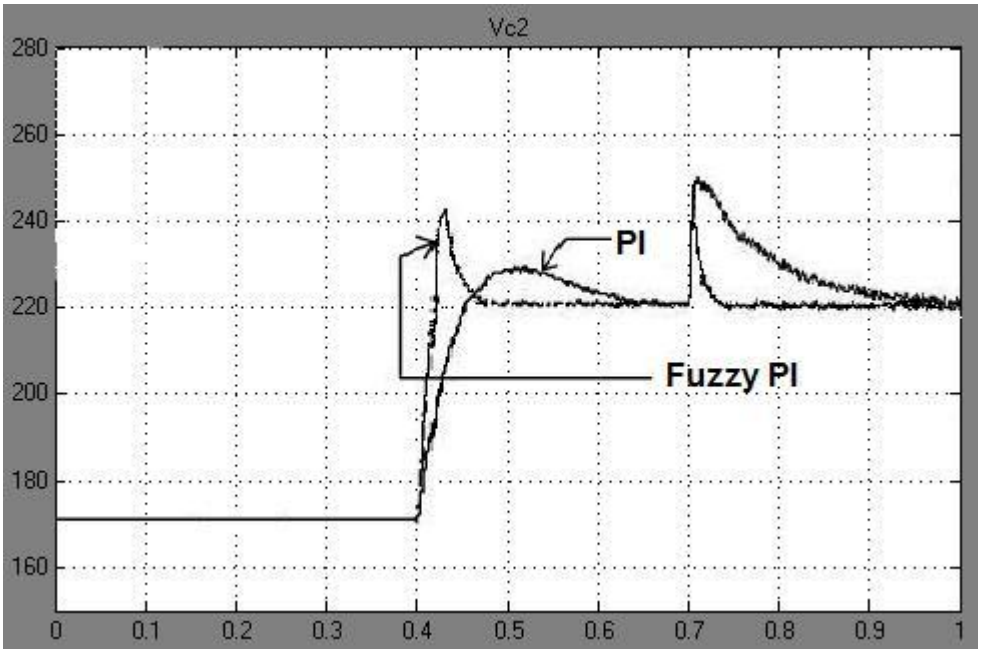
Figure 4.28 Capacitor voltages when the load is decreased for the shunt APF with DP topology (a) feedback (b) feedforward

When the load is decreased at t = 0.7 s, the capacitor voltage is discharged to compensate the harmonic currents and will be charging back to 220 V after the harmonic currents are isolated. The capacitor voltage will reach 220 V faster when using the Fuzzy PI controller compared to the PI controller.

Figure 4.29 shows the comparison of the capacitor voltage when PI and Fuzzy PI controller (25 rules) with HCC are used in the shunt APF with DP topology when the load is increased. At t = 0.4 s, when the shunt APF starts to mitigate the harmonic currents, the capacitor voltage reaches 220 V faster when using Fuzzy PI controller compared to the PI controller.



(a)



(b)

Figure 4.29 Capacitor voltages when the load is increased for the shunt APF with DP topology (a) feedback (b) feedforward

When the load is increased at t = 0.7s, the capacitor voltage is charged to compensate the harmonic currents and will discharge back to 220V after the harmonics are isolated. The capacitor voltage will reach 220V faster when using the Fuzzy PI controller compared to the PI controller.

CHAPTER 5

DISCUSSION AND FUTURE WORK

From the simulation results, the shunt APF with DP topology mitigates the harmonic currents better when using Fuzzy PI compared to the PI controller for the HCC. The feedback shunt APF mitigates the 5^{th} and 7^{th} harmonic currents while the feedforward shunt APF mitigates the high order harmonic currents until the 31^{st} order.

4.1 Discussion

Since the shunt APF with DP topology is composed of two inverters, people may argue if this is economically feasible. It is expected that two inverters will contribute to higher cost than a single one since each inverter comes with its own controlling device. The cost of the control system is in fact lower compared to the power switches. On the contrary, the most expensive components are the power switches and the passive power components such as the boost inductor L_f and the DC capacitor C.

For the shunt APF with DP topology, the harmonic currents are divided between the two inverters as mentioned above. The current in each inverter is thus lower than that of a single unit inverter, which contributes to a reduced total power of both inverters.

From the simulation results, the shunt APF isolates the harmonic current better when using a Fuzzy PI controller with more rules for the HCC. This is verified by the lower percent THD of the source current when using the Fuzzy PI controller with more rules. When the PI controller is utilized, the THD of the system is 0.98% and 1.04% for the case of increasing and decreasing load respectively. On the other hand, when the Fuzzy PI controller is employed, the THD is lower when using more rules but takes longer simulation time. This can be confirmed by referring to Table 5.1.

Table 5.1 THD when using Fuzzy PI controller

THD		Load increase	Load reduce
Fuzzy PI controller	9 rules	0.88%	1.03%
	25 rules	0.84%	0.99%
	81 rules	0.73%	0.90%

The percent THD is high when the load is changed from *R* in series with *L* to *R* in parallel with *C* due to the charging and discharging of the capacitor voltage that will produce more harmonic currents.

When the load is increased or decreased or vice versa, the Fuzzy PI controller performs better than the PI controller in terms of harmonic isolation. The former takes less than 0.1 s to make the error become zero in comparison to the latter that takes more than 0.1 s to make the error become zero.

4.2 Future Work

To improve the shunt APF with DP topology, some future works are proposed to improve the quality of harmonic isolation as well as the control system.

5.2.1 Improvement on Shunt APF

A possibility in improving the performance of the shunt APF is to consider the use of multilevel inverters instead of the conventional inverter topology. The main purpose of using the multilevel inverter is to balance the neutral point voltage in the case of disturbance or even continuous load condition [21]. Multilevel inverters can reach high voltage and reduce harmonic current without transformers. Multilevel inverters also have the ability to reduce the voltage stress on each power device due to the utilization of multiple levels on the DC bus [22]. With multilevel inverters, smaller value of the boost inductor and DC capacitor will be sufficient which will contribute to a much reduced system cost.

5.2.2 Improvement on Control System

Usually, conventional controllers such as PI controllers are used to control the switching of power devices. In recent years, Fuzzy PI controller is becoming attractive because of its fast response to the change in error and high accuracy [22].

For further improvement in the control system and harmonic mitigation capability of the shunt APF with DP topology, Artificial Neural Network (ANN) is proposed as a possible solution. By using ANN, accuracy of the control system can be better achieved as it is known as a control technique with less error [28]. The response of this control technique is also better than that based on Fuzzy logic due to the use of the back propagation algorithm to reduce the error while no rules need to be developed to get the best result [28].

5.2.3 Improvement on DC Capacitor Performance

Capacitor is one of the devices used to produce the compensated current by the charging and discharging of voltage through the IGBT/diode pair inverter. To cut the system cost, photovoltaic (PV) is proposed to replace the DC capacitor which is too expensive, particularly that with big capacity for charging purposes. By using PV as a voltage source for the shunt APF the process of charging and discharging of voltage is eliminated thus possibly improving its harmonic current mitigation capability.

CHAPTER 6

CONCLUSIONS

4.3 Summary and Conclusion

From this project, a three-phase power system feeding a nonlinear load connected to a shunt APF with DP topology is found to reduce more harmonic current compared to the conventional topology. The feedback shunt APF mitigates the 5^{th} and 7^{th} harmonics while the feedforward shunt APF mitigates the rest of the harmonic currents until the 31^{st} order.

The shunt APF with DP topology is capable of isolating the harmonic currents depending on the control system that controls the switching signals of the power devices. This is due to the charging of the DC capacitor through the diode and its discharging through the IGBT when the gate signals are received. The system response in isolating the harmonic currents is better when Fuzzy PI in contrast to the conventional PI is used as part of its controller.

The proposed Fuzzy PI controller for HCC makes the control system of the shunt APF with DP topology more efficient in generating the switching signals of the power devices. The percent THD of the three-phase source current is lower when the Fuzzy PI controller generates the switching signals compared to that of the PI controller. The percent THD is found to be further reduced when the Fuzzy PI controller uses more rules but the time taken to finish the simulation is too long.

As a conclusion, the objective of this project to reduce the harmonic currents due to non-linear load in a three-phase system has been fully achieved. The simulation design of the shunt APF with DP topology using PI and Fuzzy PI controller has been completed using Matlab/Simulink. This has allowed the analysis on the performance of the shunt APF for both conditions and can be used as a basis for further investigations.

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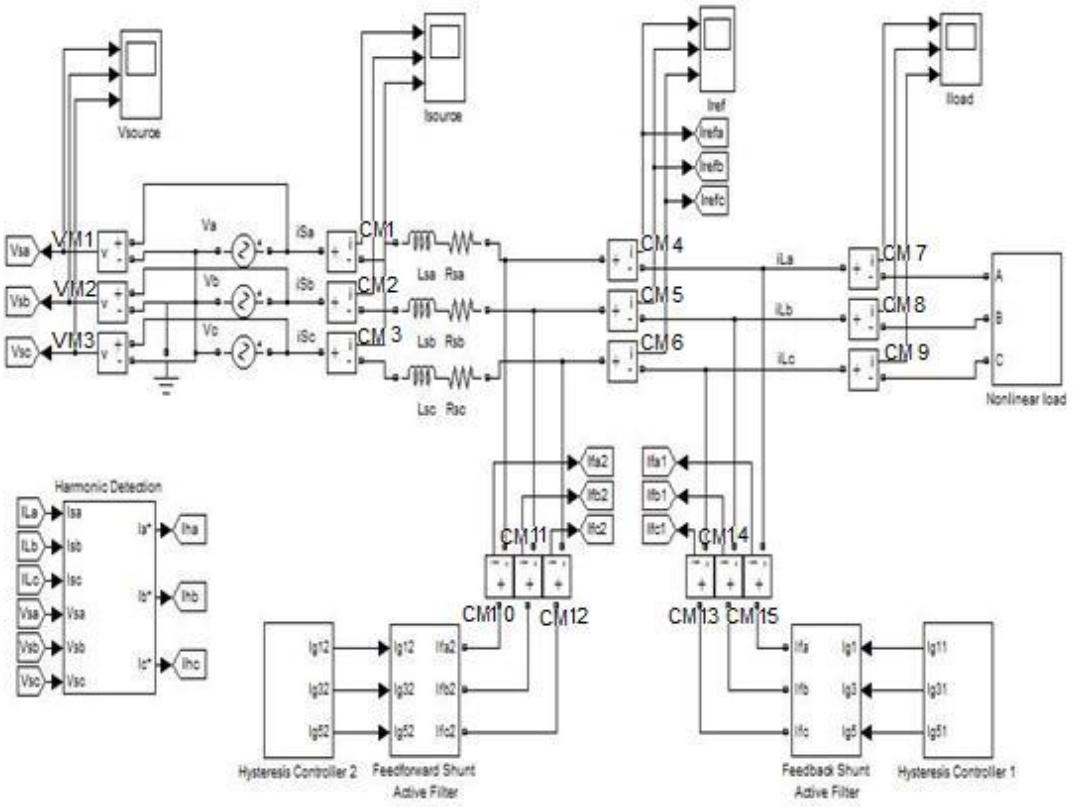
APPENDIX A

MATLAB DOCUMENTATIONS FOR SIMULATION MODEL

QISAPF_DP topology

Nurul Izuddin A Rahman

8-MAY-2009



Model QISAPF_DP topology

Full Model System

1. QISAPF_DP topology
2. APF
   - 2.1 Feedback Shunt APF
   - 2.2 Feedforward Shunt APF
3. Controller
   - 3.1 Hysteresis Controller 1
   - 3.2 Hysteresis Controller 2
4. Harmonic Detection
5. Nonlinear Load

Simulation Parameter	**Value**
Start time	0
Stop time	1
Solver	ode23t
Relative Tolarance	1e-3
Absolute Tolerance	auto
MaxStep	auto
MaxOrder	5
ZeroCross	on

System - QISAPF DP topology

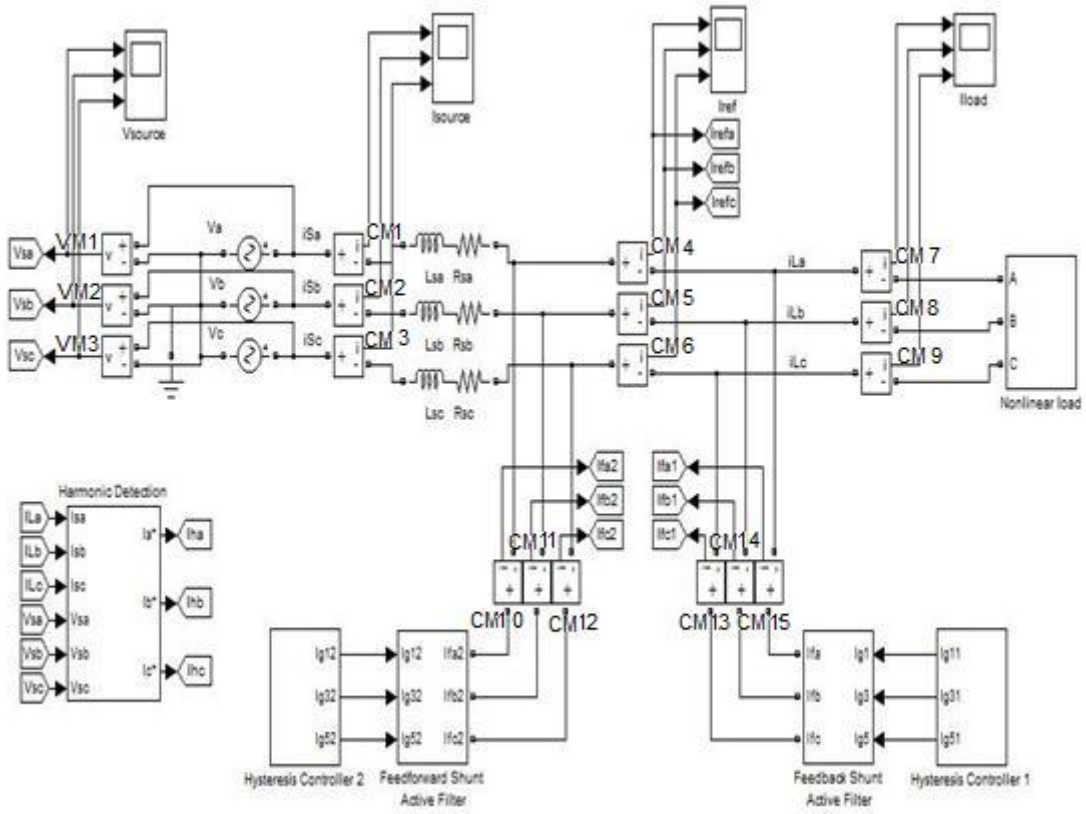


Table 1. Three-phase AC voltage source block properties

Name	SineType	Amplitude	Bias	Frequency	Phase	Measure
Va	time based	100	0	50	0	None
Vb	time based	100	0	50	120	None
Vc	time based	100	0	50	240	None

Table 2. Voltage Measurement block properties

Name	Phasor Simulation	Output Type	PSB output Type	PSB equivalent
VM1	off	Magnitude	0	0
VM2	off	Magnitude	0	0
VM3	off	Magnitude	0	0

Table 3. Current Measurement block properties

Name	Phasor Simulation	Output Type	PSB output Type	PSB equivalent
CM1	off	Magnitude	0	0
CM2	off	Magnitude	0	0
CM3	off	Magnitude	0	0

CM4	off	Magnitude	0	0
CM5	off	Magnitude	0	0
CM6	off	Magnitude	0	0
CM7	off	Magnitude	0	0
CM8	off	Magnitude	0	0
CM9	off	Magnitude	0	0
CM10	off	Magnitude	0	0
CM11	off	Magnitude	0	0
CM12	off	Magnitude	0	0
CM13	off	Magnitude	0	0
CM14	off	Magnitude	0	0
CM15	off	Magnitude	0	0

Table 4. Goto Block Properties

Name	GotoTag	Tag Visibility
Vsa	Vsa	global
Vsb	Vsb	global
Vsc	Vsc	global
Irefa	Irefa	global
Irefb	Irefb	global
Irefc	Irefc	global
Iha	Iha	global
Ihb	Ihb	global
Ihc	Ihc	global
Ifa1	Ifa1	global
Ifb1	Ifb1	global
Ifc1	Ifc1	global
Ifa2	Ifa2	global
Ifb2	Ifb2	global
Ifc2	Ifc2	global

Table 5. From Block Properties

Name	GotoTag	Define in
ILa	ILa	selector
ILb	ILb	selector
ILc	ILc	selector
Vsa	Vsa	selector
Vsb	Vsb	selector
Vsc	Vsc	selector

System - QISAPF_DP topology/APF/Feedback Shunt APF

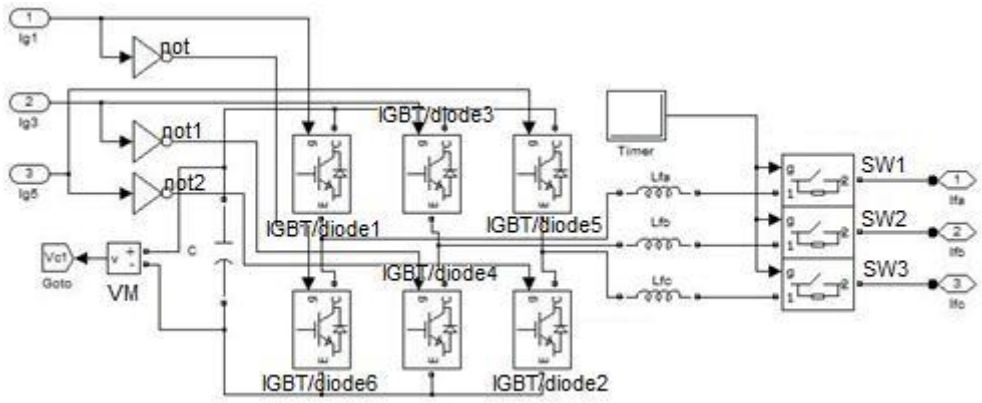


Table 1. Input block properties

Name	Port	Port Dimension	Sample Time	Define In
Ig1	1	-1	-1	switching signal 1
Ig3	2	-1	-1	switching signal 3
Ig5	3	-1	-1	switching signal 5

Table 2. Connection block properties

Name	Port	Port location on parent subsystem
Ifa	1	left
Ifb	2	left
Ifc	3	left

Table 3. Power switch block properties

Name port	Ron	Rs	Cs	Measurement
IGBT/diode1	1e-3	1e5	inf	off
IGBT/diode2	1e-3	1e5	inf	off
IGBT/diode3	1e-3	1e5	inf	off
IGBT/diode4	1e-3	1e5	inf	off
IGBT/diode5	1e-3	1e5	inf	off
IGBT/diode6	1e-3	1e5	inf	off

Table 4. Switch block properties

Name port	Ron	Initial state	Rs	Cs	Measurement
SW1	0.001	0	1e5	inf	off
SW2	0.001	0	1e5	inf	off
SW3	0.001	0	1e5	inf	off

Table 5. Timer block properties

Name	Times	Amplitude
Timer	[0 0.4]	1

Table 6. RLC branch block properties

Name	Resistance	Inductance	Capacitance	Measurements
Lfa	0	5.6mH	0	none
Lfb	0	5.6mH	0	none
Lfc	0	5.6mH	0	none
C	0	0	2.2mF	none

Table 7. Voltage Measurement block properties

Name	Phasor Simulation	Output Type	PSB output Type	PSB equivalent
VM	off	Magnitude	0	0

Table 8. Goto Block Properties

Name	GotoTag	Tag Visibility
Vc1	Vc1	global

Table 9. Logic Block Properties

Name	Operator	Inputs	AllPortsSameDT	OutDataTypeMode	LogicDataType
not	not	1	off	Logical	unit(8)
not1	not	1	off	Logical	unit(8)
not2	not	1	off	Logical	unit(8)

System - QISAPF_DP topology/APF/Feedforward Shunt APF

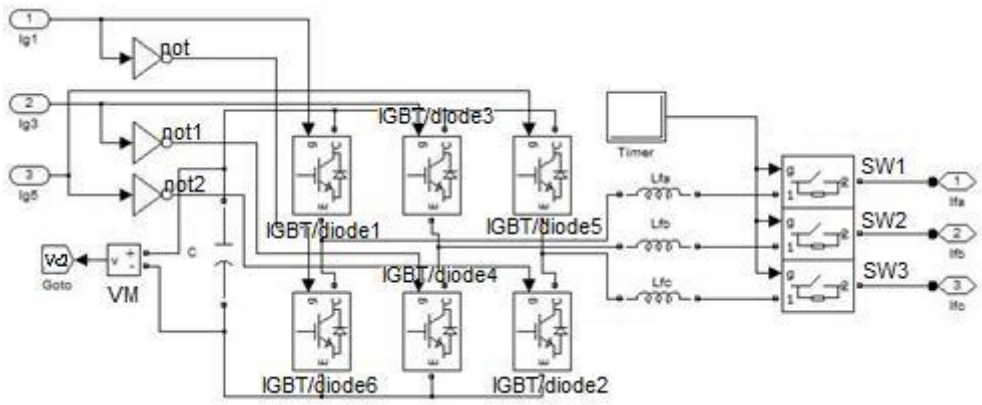


Table 1. Input block properties

Name	Port	Port Dimension	Sample Time	Define In
Ig11	1	-1	-1	switching signal
Ig33	2	-1	-1	switching signal
Ig55	3	-1	-1	switching signal

Table 2. Connection block properties

Name	Port	Port location on parent subsystem
Ifa	1	left
Ifb	2	left
Ifc	3	left

Table 3. Power switch block properties

Name port	Ron	Rs	Cs	Measurement
IGBT/diode1	1e-3	1e5	inf	off
IGBT/diode2	1e-3	1e5	inf	off
IGBT/diode3	1e-3	1e5	inf	off
IGBT/diode4	1e-3	1e5	inf	off
IGBT/diode5	1e-3	1e5	inf	off
IGBT/diode6	1e-3	1e5	inf	off

Table 4. Switch block properties

Name port	Ron	Initial state	Rs	Cs	Measurement
SW1	0.001	0	1e5	inf	off
SW2	0.001	0	1e5	inf	off
SW3	0.001	0	1e5	inf	off

Table 5. Timer block properties

Name	Times	Amplitude
Timer	[0 0.4]	1

Table 6. RLC branch block properties

Name	Resistance	Inductance	Capacitance	Measurements
Lfa	0	3mH	0	none
Lfb	0	3mH	0	none
Lfc	0	3mH	0	none
C	0	0	2.2mF	none

Table 7. Voltage Measurement block properties

Name	Phasor Simulation	Output Type	PSB output Type	PSB equivalent
VM	off	Magnitude	0	0

Table 8. Goto Block Properties

Name	GotoTag	Tag Visibility
Vc2	Vc2	global

Table 9. Logic Block Properties

Name	Operator	Inputs	AllPortsSameDT	OutDataTypeMode	LogicDataType
not	not	1	off	Logical	unit(8)
not1	not	1	off	Logical	unit(8)
not2	not	1	off	Logical	unit(8)

System - QISAPF_DP topology/Controller/Hysteresis Controller 1

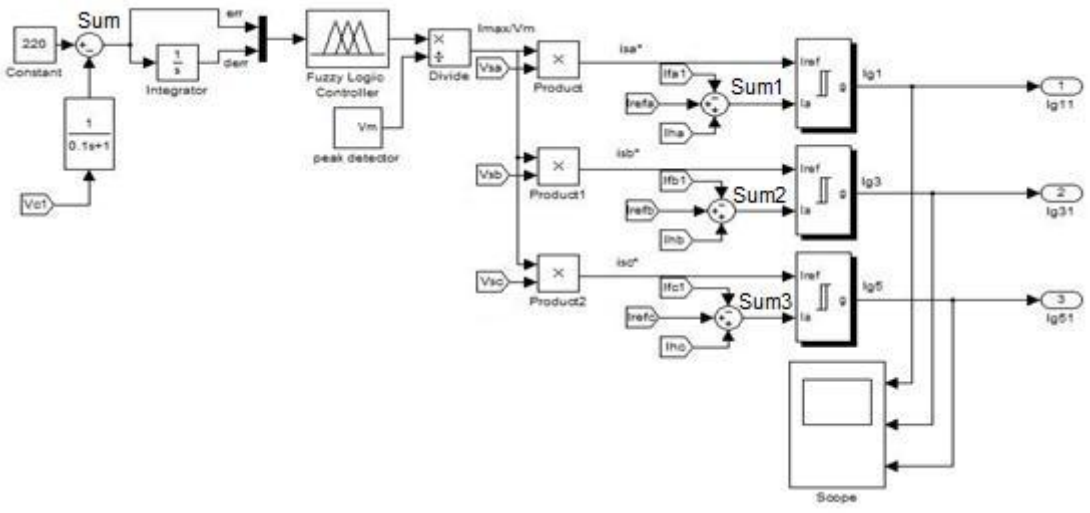


Table 1. Product Block Properties

Name	Inputs	Multiplication	InputSameDT	OutDataTypeMode

Product input	2	Element-wise(.*)	off	Same as first
Product1 input	2	Element-wise(.*)	off	Same as first
Product2 input	2	Element-wise(.*)	off	Same as first

Table 2. Sum Block Properties

Name	IconShape	Inputs	InputSameDT	OutDataTypeMode
Sum	round	-+	off	Inherit via internal rule
Sum1	round	-++	off	Inherit via internal rule
Sum2	round	-++	off	Inherit via internal rule
Sum3	round	-++	off	Inherit via internal rule

Table 3. Hysteresis Block Properties

Name	Hysteresis band
Ig1	2
Ig3	2
Ig5	2

Table 4. Outport Block Properties

Name	Port	Output When Disabled	Initial Output	Used By
Ig11	1	held	[]	Switching signal IGBT/diode1
Ig31	2	held	[]	Switching signal IGBT/diode3
Ig51	3	held	[]	Switching signal IGBT/diode5

Table 5. Fuzzy Block Properties

Name	Input	Output
Fuzzy logic controller	Error	Maximum current

Table 6. Constant Block Properties

Name	Value	Vector Params1D	Out Data Type Mode
Constant	220	on	Inherit from 'Constant value'

Table 7. From Block Properties

Name	GotoTag	Define in
Vc1	Vc1	selector
Vsa	Vsa	selector
Vsb	Vsb	selector
Vsc	Vsc	selector
Irefa	Irefa	selector
Irefb	Irefb	selector
Irefc	Irefc	selector
Iha	Iha	selector
Ihb	Ihb	selector
Ihc	Ihc	selector
Ifa1	Ifa1	selector
Ifb1	Ifb1	selector
Ifc1	Ifc1	selector

Table 8. Integrator Block Properties

Name	External reset	Initial condition source	Initial condition
Integrator	none	internal	0

Table 9. Product Block Properties

Name	No. of input	Dimension	Sample time
Divide	2	1	-1

System - QISAPF_DP topology/Controller/Hysteresis Controller 2

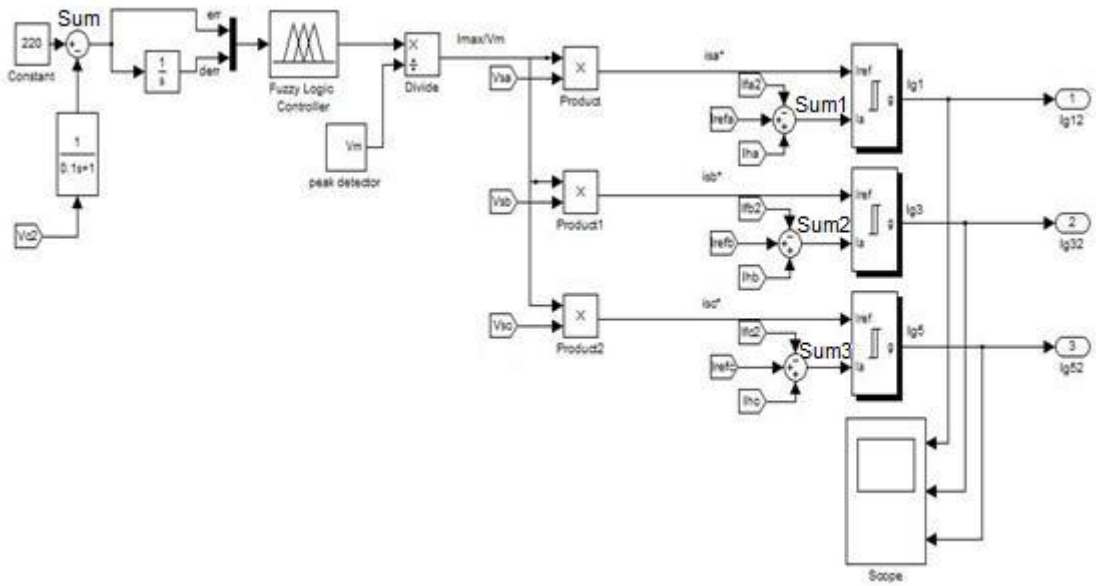


Table 1. Product Block Properties

Name	Inputs	Multiplication	InputSameDT	
	OutDataTypeMode			
Product	2	Element-wise(.*)	off	Same as first input
Product1	2	Element-wise(.*)	off	Same as first input
Product2	2	Element-wise(.*)	off	Same as first input

Table 2. Sum Block Properties

Name	IconShape	Inputs	InputSameDT	
	OutDataTypeMode			
Sum	round	-+	off	Inherit via internal rule
Sum1	round	-++	off	Inherit via internal rule
Sum2	round	-++	off	Inherit via internal rule
Sum3	round	-++	off	Inherit via internal rule

Table 3. Hysteresis Block Properties

Name	Hysteresis band
Ig1	2
Ig3	2
Ig5	2

Table 4. Outport Block Properties

Name	Port	Output When Disabled	Initial Output	Used By
Ig12	1	held	[]	Switching signal IGBT/diode1
Ig32	2	held	[]	Switching signal IGBT/diode3
Ig52	3	held	[]	Switching signal IGBT/diode5

Table 5. Fuzzy Block Properties

Name	Input	Output
Fuzzy logic controller	Error	Maximum current

Table 6. Constant Block Properties

Name	Value	Vector Params1D	Out Data Type Mode
Constant	220	on	Inherit from 'Constant value'

Table 7. From Block Properties

Name	GotoTag	Define in
Vc2	Vc1	selector
Vsa	Vsa	selector
Vsb	Vsb	selector
Vsc	Vsc	selector
Irefa	Irefa	selector
Irefb	Irefb	selector
Irefc	Irefc	selector
Iha	Iha	selector
Ihb	Ihb	selector
Ihc	Ihc	selector
Ifa2	Ifa2	selector
Ifb2	Ifb2	selector
Ifc2	Ifc2	selector

Table 8. Integrator Block Properties

Name	External reset	Initial condition source	Initial condition
Integrator	none	internal	0

Table 9. Product Block Properties

Name	No. of input	Dimension	Sample time
Divide	2	1	-1

System - QISAPF_DP topology/Harmonic Detection

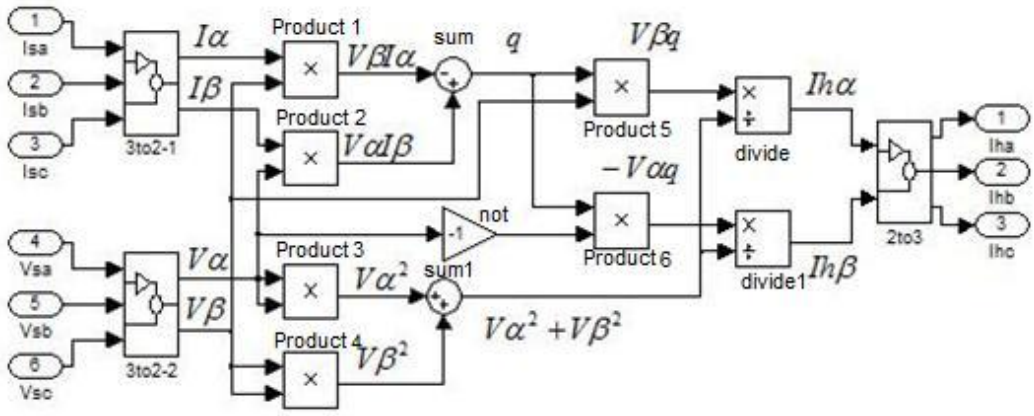


Table 1. Input Block Properties

Name	Port	Port Dimension	Sample Time	Define in
Isa	1	-1	-1	Current Phase A
Isb	2	-1	-1	Current Phase B

Isc	3	-1	-1	Current Phase C
Vsa	4	-1	-1	Voltage Phase A
Vsb	5	-1	-1	Voltage Phase B
Vsc	6	-1	-1	Voltage Phase C

Table 2. Output Block Properties

Name	Port	Port Dimension	Sample Time	Define in
Iha	1	-1	-1	Harmonic Current A
Ihb	2	-1	-1	Harmonic Current B
Ihc	3	-1	-1	Harmonic Current C

Table 3. Product Block Properties

Name	Input Mode	Mulfunction	Input Same DT	Output Data Type
Pruduct 1 input	2	Element-wise(.*)	off	Same as first
Pruduct 2 input	2	Element-wise(.*)	off	Same as first
Pruduct 3 input	2	Element-wise(.*)	off	Same as first
Pruduct 4 input	2	Element-wise(.*)	off	Same as first
Pruduct 5 input	2	Element-wise(.*)	off	Same as first
Pruduct 6 input	2	Element-wise(.*)	off	Same as first

Table 4. Logic Block Properties

Name	Operator	Inputs	AllPortsSameDT	OutDataTypeMode	LogicDataType
not	not	1	off	Logical	unit(8)

Table 5. Sum Block Properties

Name	IconShape	Inputs	InputSameDT	OutDataTypeMode
Sum	round	-+	off	Inherit via internal rule
Sum1	round	++	off	Inherit via internal rule

Table 6. Divide Block Properties

Name	Input Mode	Mulfunction	Input Same DT	Output Data Type
Divide	2	Element-wise(.*)	off	Same as first input

Divide input	2	Element-wise(.*)	off	Same as first

System - QISAPF_DP topology/Nonlinear load

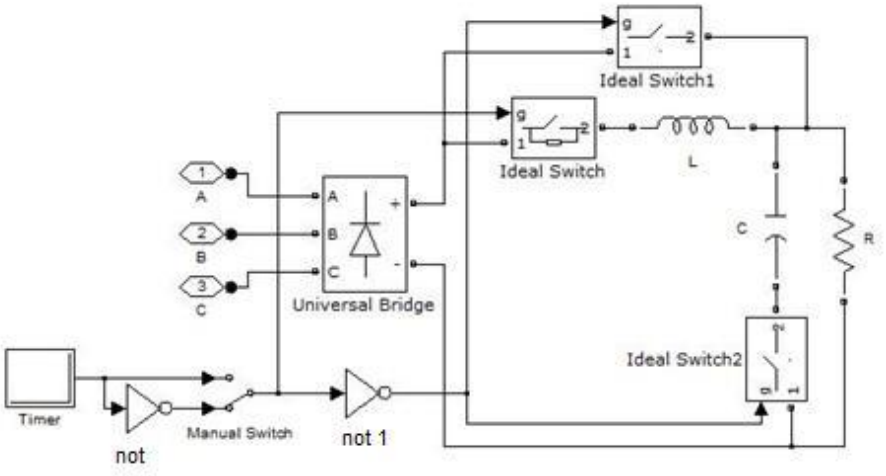


Table 1. Connection Block Properties

Name	Port	Port location on parent subsystem
A	1	Voltage Phase A
B	2	Voltage Phase B
C	3	Voltage Phase C

Table 2. Timer Block Properties

Name	Times	Amplitude
Timer	[0 0.7]	1

Table 3. Logic Block Properties

Name	Operator	Inputs	AllPortsSameDT	OutDataTypeMode	LogicDataType
not	not	1	off	Logical	unit(8)
not1	not	1	off	Logical	unit(8)

Table 4. Switch block properties

Name	Ron	Initial state	Rs	Cs	Measurement port
Ideal Switch	0.001	0	1e5	inf	off
Ideal Switch1	0.001	0	1e5	inf	off
Ideal Switch2	0.001	0	1e-5	inf	off
Manual Switch	0	0	0	0	none

Table 5. Load block properties

Name	Resistance	Inductance	Capacitance	Measurements
R	50	0	0	none
L	0	15mH	0	none
C	0	0	1.5mF	none

Table 6. Rectifier block properties

Name	Type	No.Bridge	Rs	Cs	Ron	Lon	Vf	Measurement
Universal Bridge	Diode	3	1e5	inf	1e-3	0	0	none