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Research Article

Design of CMOS Tunable Image-Rejection Low-Noise Amplifier with Active Inductor

Ler Chun Lee,[1,2] Abu Khari bin A'ain,[1] and Albert Victor Kordesch[2]

[1] *Microelectronics and Computer Department, Faculty of Electrical Engineering, University of Technology Malaysia, 81310 Skudai, Johor, Malaysia*
[2] *Device Modeling Department, Silterra Malaysia Sdn. Bhd., 09000 Kulim, Kedah, Malaysia*

Correspondence should be addressed to Abu Khari bin A'ain, abu@fke.utm.my

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A fully integrated CMOS tunable image-rejection low-noise amplifier (IRLNA) has been designed using Silterra's industry standard 0.18 μm RF CMOS process. The notch filter is designed using an active inductor. Measurement results show that the notch filter designed using active inductor contributes additional 1.19 dB to the noise figure of the low-noise amplifier (LNA). A better result is possible if the active inductor is optimized. Since active inductors require less die area, the die area occupied by the IRLNA is not significantly different from a conventional LNA, which was designed for comparison. The proposed IRLNA exhibits S21 of 11.8 dB, S11 of −17.8 dB, S22 of −10.7 dB, and input 1 dB compression point of −12 dBm at 3 GHz

1. INTRODUCTION

Recently, direct-conversion and low-intermediate frequency (low-IF) receivers have become highly popular choices in RFIC since they avoid the need for expensive external passive components such as surface-acoustic wave (SAW) filters for image rejection. Unfortunately, serious problems do exist for direct-conversion and low-IF receivers. The direct-conversion receiver is very sensitive to DC offset and low-frequency interference signals. Since IF of the direct-conversion receiver is zero, there is a little doubt that flicker noise will produce a maximum negative effect in direct-conversion receivers. A low-IF receiver has many of the attributes of a direct-conversion receiver but has lower sensitivity to DC offsets and flicker noise. However, the image rejection problem reappears [1].

The superheterodyne receiver is the most widely used receiver front-end architecture and exhibits good RF performance. Proper image signal filtering is required. This can be done by using external SAW filters. The drawbacks of using SAW filters are increased cost and device size [2]. To overcome these problems, recent research has focused on IRLNA that uses a notch filter to reject the image signals [3–6].

Unlike on-chip spiral inductors, active inductors have smaller die area, larger inductance, higher-quality factor (Q), tunable inductance, and Q. The Q of the spiral inductor is usually low, this being due to the wiring and substrate losses. Unfortunately, active inductors have poor noise performance, poor linearity, and higher-power dissipation, and are more sensitive to process, voltage supply, and temperature (PVT) variation compared to spiral inductors.

The paper is organized as follows: Section 2 introduces the concept and design of active inductors. Section 3 discusses several popular types of IRLNA that have been reported in the literature. The proposed IRLNA designed using an active inductor is presented in Section 4, with measurement results. Section 5 concludes the paper.

2. ACTIVE INDUCTOR CIRCUIT DESIGN

Active inductor is an attractive alternative to low-Q on-chip spiral inductors. For monolithic RFIC applications, the design of the active inductor using gyrator is best described in Figure 1(a). g_1, g_2, C_1, and C_2 are parasitic conductance and capacitance, respectively. G_{m1} and G_{m2} represent transconductors and are connected back-to-back to form a gyrator. The input admittance of the gyrator circuit, Y_{in}, is shown as follows:

$$Y_{\text{in}} = \frac{1}{Z_{\text{in}}} = g_1 + sC_1 + \frac{G_{m1}G_{m2}}{sC_2 + g_2}. \quad (1)$$

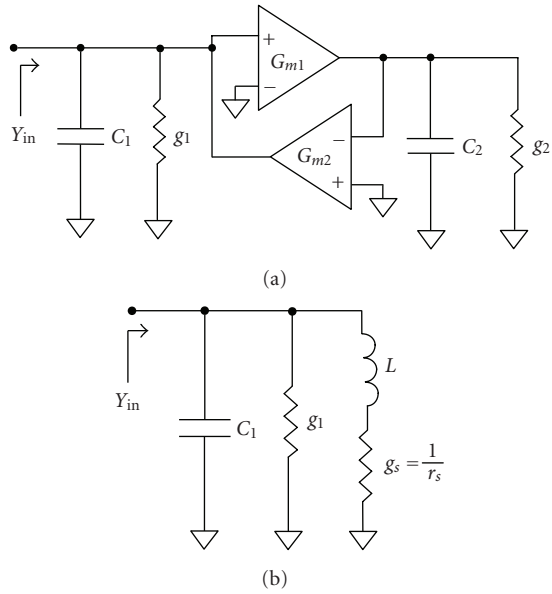


Figure 1: (a) Active inductor for RFIC applications; (b) simplified model for active inductor.

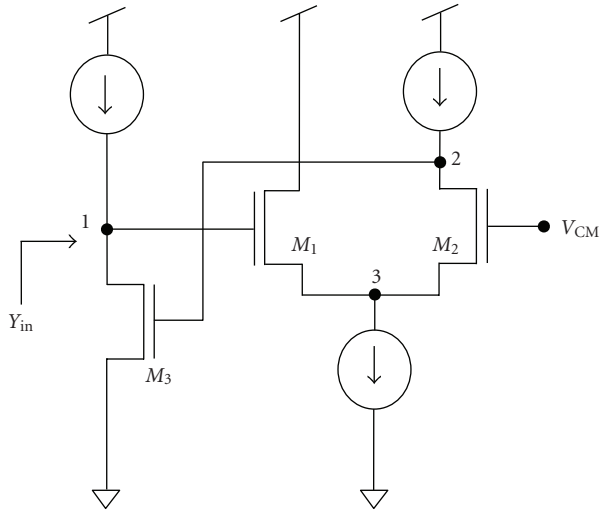


Figure 2: Simplified circuit diagram of the active inductor used in this design.

The third item in (1) behaves as an inductor with resistive loss. Based on (1), the active inductor can be modeled as a resonator as shown in Figure 1(b), where

$$L = \frac{C_2}{G_{m1}G_{m2}}, \qquad r_s = \frac{g_2}{G_{m1}G_{m2}}. \tag{2}$$

The active inductor proposed in [7] was used in this design. The simplified circuit design of the active inductor is shown in Figure 2. According to [7], if $g_{m1} \approx g_{m2} >> g_2$, then

$$G_{m1}(s) \approx \frac{0.5g_{m1}}{1 + s(C_{gs1} + C_3)/(g_{m1} + g_{m2} + g_3)}, \tag{3}$$

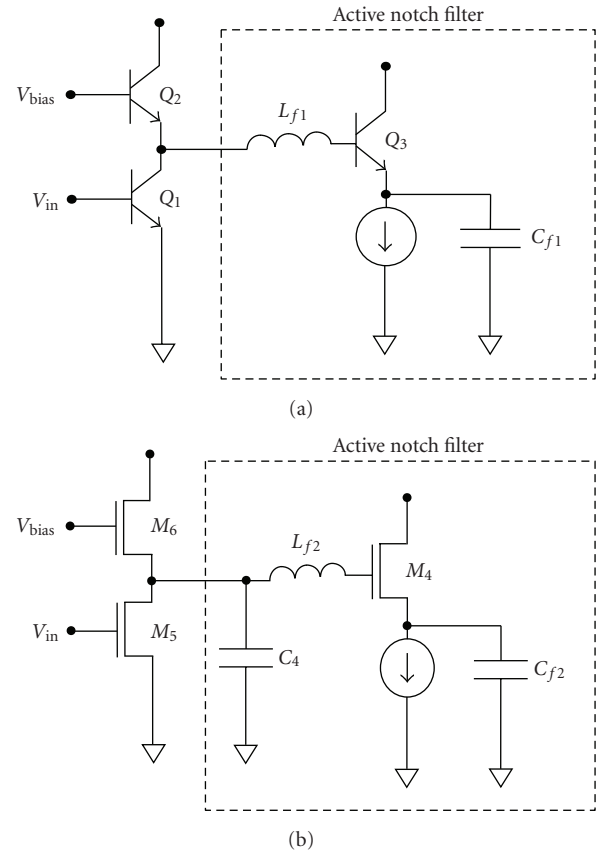


Figure 3: IRLNA with (a) second-order active notch filter and (b) third-order active notch filter.

where g_3 and C_3 are the parasitic conductance and capacitance at node 3, respectively. The input admittance, Y_{in} in Figure 2, can be calculated from (1) and (3) as follows:

$$Y_{in} = sC_1 + g_1 + Z_s^{-1},$$
$$Z_s \approx \frac{sC_2 + [g_2 - (\omega^2 C_2(C_{gs1} + C_3)/(g_{m1} + g_{m2} + g_3))]}{0.5g_{m1}g_{m3}}. \tag{4}$$

From (4), the inductance can be tuned by varying C_2, while Q of the active inductor can be tuned by varying C_3. Hence, two varactors are added at node 2 and node 3 for inductance and Q tuning, respectively.

3. OVERVIEW OF EXISTING IRLNA DESIGN

3.1. Second- and third-order active notch filters

The first fully integrated IRLNA using a second-order active filter was introduced in [8] using 0.5 μm bipolar technology with 25 GHz transit frequency. The second-order active notch filter is based on a series LC resonator that resonates at the image frequency. Figure 3(a) shows the cascade LNA

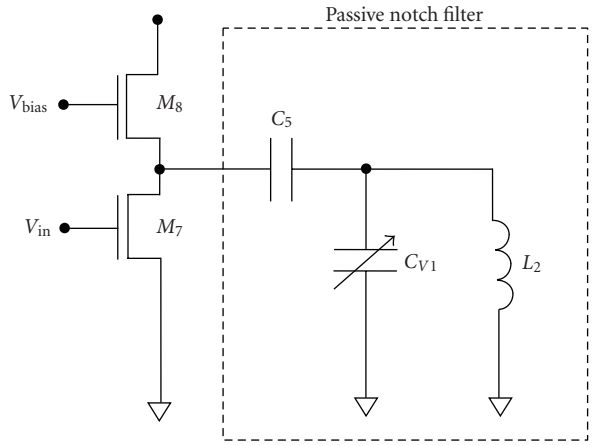


Figure 4: CMOS IRLNA with third-order passive notch filter.

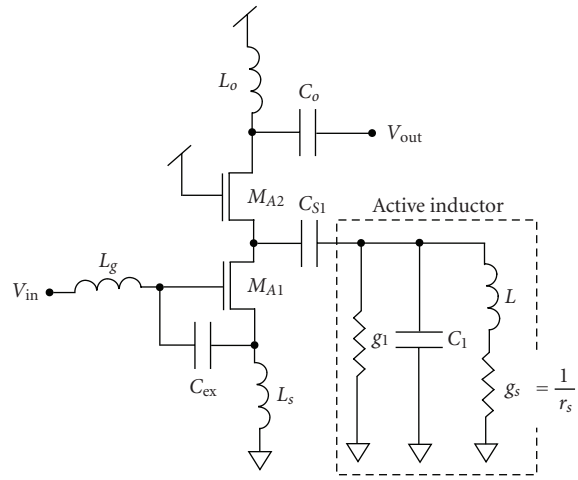


Figure 5: Complete schematic for the proposed IRLNA.

with thesecond-order active filter. The input impedance of the second-order active notch filter is given by [8]

$$Z_{in} = sL_{f1} + \frac{1}{sC_\pi} + \frac{1}{sC_{f1}} + R_{ind} + r_{bb} - \frac{g_m}{\omega^2 C_\pi C_{f1}}, \quad (5)$$

where C_π, g_m, and r_{bb} are the emitter-base capacitance, transconductance, and base resistance of $Q3$. R_{ind} is the resistive loss of the inductor. At image frequency, the input impedance of the active notch filter becomes minimum. That will decrease the gain of the LNA. However, the notch filter might have negative impact on the LNA because the input impedance of the second-order active notch filter might be lower than the case without the filter. The power gain and noise figure of the IRLNA will degrade due to the signal loss.

To overcome the limitation of the IRLNA proposed in [8], a CMOS third-order active notch filter has been proposed in [5], as shown in Figure 3(b). Assuming that all the parasitic components are cancelled, the input impedance of the active notch filter now can be expressed as follows [5]:

$$Z_{in} = \frac{s^2 L_{f2} C_{eq} + 1}{s\left(s^2 C_{tt} L_{f2} C_{eq} + C_{tt} + C_{eq}\right)}, \quad (6)$$

where $C_{tt} = C_4 + C_{gs4}$ and $C_{eq}^{-1} = C_{gs4}^{-1} + C_{f2}^{-1}$.

From (6), the active notch filter proposed in [5] can have high impedance at the wanted signal frequency and low impedance at the image signal frequency.

3.2. Third-order passive notch filter

Third-order passive notch filter technique was proposed in [3] for CMOS IRLNA, as shown in Figure 4. The input impedance of the passive notch filter as given by [3] is the following:

$$Z_{in} = \frac{L_2\left(C_{v1} + C_5\right)s^2 + 1}{C_{v1} C_5 L_2 s^3 + C_5 s}. \quad (7)$$

Similar to the notch filter proposed in [5], the passive notch filter shown in Figure 4 has low and high input impedance at image signal frequency and wanted signal frequency, respectively. Since CMOS spiral inductors usually have very low Q, a cross-connected differential transistor pair has been used as a negative impedance circuit to increase Q of the notch filter. The notch frequency tuning of the IRLNA can be done by using varactor C_{v1}.

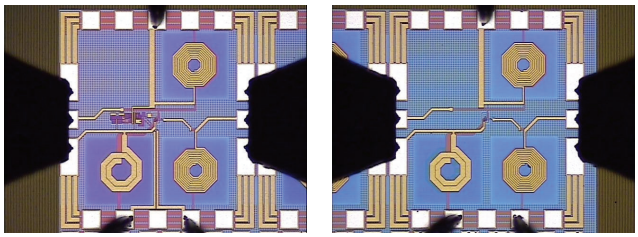
4. PROPOSED IRLNA USING ACTIVE INDUCTOR

Since spiral inductors consume large die area compared to active devices, the use of active inductor to replace spiral inductor becomes an attractive choice for notch filters. Circuit diagram of the proposed IRLNA using active inductor is shown in Figure 5. The spiral inductor in the notch filter in Figure 4 has been replaced by an active inductor. Since the notch frequency of the image-rejection notch filter can be tuned by the active inductor, the varactor in Figure 4 can be eliminated. If the Q of the active inductor is high enough, the input impedance of the notch filter shown in Figure 5 is approximated by (7).

The wanted signal frequency and image signal frequency are located at

$$f_{wanted} = \pm\frac{1}{2\pi\sqrt{LC_1}},$$
$$f_{image} = \pm\frac{1}{2\pi\sqrt{L\left(C_1 + C_{s1}\right)}}. \quad (8)$$

The active inductor shown in Figure 2 is used to implement our proposed IRLNA. The active die area for the active inductor including DC biasing circuits is $70 \times 162\,\mu m^2$, which is much smaller than a spiral inductor that typically requires $300 \times 300\,\mu m^2$. As mentioned in Section 2, two NMOSs in N-well varactors were added at node 2 and node 3 for inductance and Q tuning, respectively. The proposed IRLNA adopts popular source-degenerated LNA architecture for low-noise, which is shown in Figure 5. An extra capacitor C_{ex} together with L_g and L_s is used to obtain power-constrained simultaneous noise and input matching [5].



(a) (b)

Figure 6: Die micrograph for (a) proposed IRLNA and (b) LNA.

As mentioned before, C_{s1} together with the active inductor forms a third-order notch filter for image rejection. All the devices shown in Figure 5 are implemented on-chip.

The proposed IRLNA was fabricated using Silterra's 0.18 μm industry standard RF CMOS process. For comparison, an LNA identical to the proposed IRLNA but without notch filter was included in the fabrication. The die micrograph of the LNA and IRLNA is shown in Figure 6. All the DC, S-parameters, and noise figure measurements were performed on wafer using Cascade Microtech's RF probe station with GSG Infinity probes. Due to the DC biasing startup circuit problem, the actual DC biasing active inductor is different from the predicted value. Current sources located at node 1 and node 2 of the active inductor operate in linear region and this lowers Q of the active inductor. Measured Q of the active inductor returns a value of around 5 to 8, and this is lower than the expected value. The low-Q active inductor has a negative impact on the gain and noise performance of the IRLNA.

S-parameters of the IRLNA and LNA are shown in Figures 7 and 8. As can be observed from Figure 7, the notch filter designed using active inductor can provide additional 8.25 dB image rejection at 1.42 GHz. An active inductor with higher Q would further improve the image-rejection of the notch filter. A comparison between the performance of the proposed IRLNA and the LNA is shown in Table 1. S21 of the proposed IRLNA is 2.8 dB lower than the LNA, which is mainly due to the low-Q active inductor.

In Table 1, the noise figures (NFs) of the LNA and IRLNA are much higher than simulation results. The excess noise is contributed from the losses of Cascade Microtech high-frequency cable and GSG Infinity probe that precede the LNA and IRLNA. The calibration of the noise figure analyzer is unable to remove these losses. Further experiments showed that the Cascade Microtech high-frequency cable has additional loss around 1.3 dB compared to Agilent coaxial cable 11500F. Hence, it is reasonable to estimate that the loss preceding the LNA, including the input GSG Infinity probe, is at least 2 dB. In addition, system port mismatch due to the on-wafer NF measurement will further increase the uncertainties of the NF measurement [9]. Besides that, there is additional noise probably contributed by the DC power supply itself. Adding a large capacitor between VDD and ground can reduce that problem.

However, comparing noise factor difference ($F_{\text{difference}}$) between IRLNA and LNA, the measured $F_{\text{difference}}$ (after de-

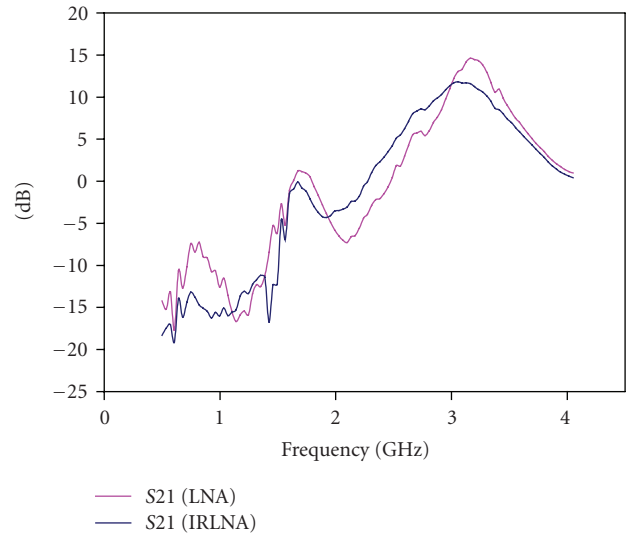


Figure 7: S21 of LNA and proposed IRLNA.

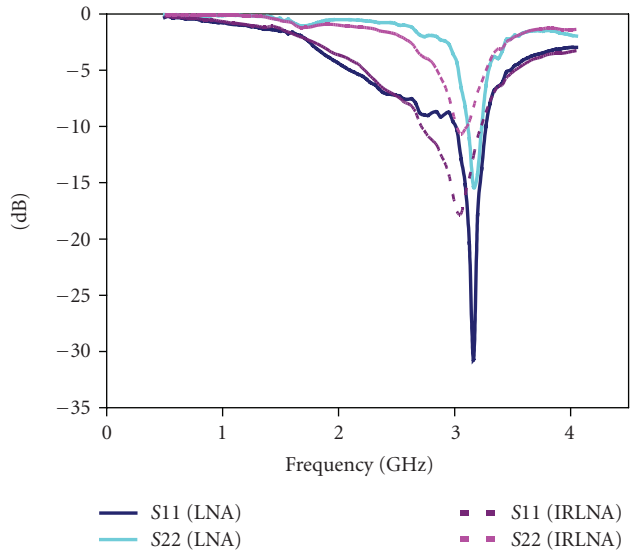


Figure 8: S11 and S22 of LNA and proposed IRLNA.

embedding) is 56% higher than simulation results. The discrepancy of $F_{\text{difference}}$ between measurement and simulation may be due to several factors mentioned below.

(a) Low-Q active inductor (due to the DC biasing circuit) results in lower gain of the LNA at the operating frequency. This can be observed from S21 of the LNA and IRLNA shown in Table 1. IRLNA's NF increases due to the lower gain.

(b) Actual losses preceding the LNA in the NF measurement system are more than 2 dB if all the losses (e.g., adapter loss and input port mismatch) are taken into consideration. Discrepancy of $F_{\text{difference}}$ in measurement and simulation will be smaller if all the losses preceding LNA are considered.

Table 1: Comparison between proposed IRLNA and LNA.

Parameters	Proposed IRLNA	LNA
Operating frequency	3.06 GHz	3.16 GHz
S11	−17.8 dB	−30.7 dB
S21	11.8 dB	14.6 dB
S12	−29.2 dB	−21.5 dB
S22	−10.7 dB	−15.4 dB
Noise figure (NF)		
Simulation	2.73 dB	1.44 dB
Measurement	6.95 dB	5.76 dB
Measurement*	4.95 dB	3.76 dB
Noise factor (F)		
Simulation	1.87	1.39
Measurement	4.95	3.77
Measurement*	3.13	2.38
1 dB compression point	−12 dBm	−15 dBm
Image-rejection (filter only)	8.25 dB	—
Image-rejection tuning range	1.25–1.49 GHz	—
Power dissipation	11 mW	7.2 mW

* Worst case estimated noise figures after de-embedding losses from cable and GSG Infinity probe. Actual noise figures will be better.

(c) Noise contributed from the active inductor is underestimated. Short-channel NMOS devices contribute more thermal noise than the value predicted by long-channel theory [10]. Long-channel thermal noise equation was used in the simulation.

Thanks to the active inductor, the actual die area occupied by the proposed IRLNA isapproximately the same as the LNA.

Besides noise performance, sensitivity of the active inductor to PVT variations is also a very important design challenge that needs to be considered. g_m of the MOSFET is the most sensitive parameter to PVT variations in the active inductor. A wider notch frequency tuning range can overcome PVT variations. Some applications like HIPERLAN require a tuning range of 150 MHz, whereas 802.11a requires tuning range of 675 MHz to cover the desired frequency band [1, 3]. The tuning range of the active inductor notch filter in this paper is limited by the varactor tuning range. A higher tuning range could be obtained by tuning MOSFET's g_m, rather than using varactors. The tuning range ($L_{\max}/L_{\min}$) of active inductors can reach more than 10 : 1 [11], which is sufficient to cover all the desired frequency bands and PVT variations.

5. CONCLUSION

Although the active inductor is noisy and has limited dynamic range compared to spiral inductors, in this paper we show that it is usable for IRLNA design. With proper design, the noise contribution from the active inductor can be reduced to its minimum level. Further improvements are still in progress, which aim to reduce the active inductor's noise contribution, power dissipation, and increase its frequency tuning range to compensate PVT variations.

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REFERENCES

[1] T. H. Lee, H. Samavati, and H. R. Rategh, "5-GHz CMOS wireless LANs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 268–280, 2002.

[2] T. Maeda, H. Yano, S. Hori, et al., "Low-power-consumption direct-conversion CMOS transceiver for multi-standard 5-GHz wireless LAN systems with channel bandwidths of 5-20 MHz," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 375–382, 2006.

[3] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 765–772, 2000.

[4] R. A. Baki and M. N. El-Gamal, "A 1.5V multigigahertz CMOS tunable image reject notch filter," in *Proceedings of the 14th International Conference on Microelectronics (ICM '02)*, pp. 144–147, Beirut, Lebanon, December 2002.

[5] T.-K. Nguyen, N.-J. Oh, C.-Y. Cha, Y.-H. Oh, G.-J. Ihm, and S.-G. Lee, "Image-rejection CMOS low-noise amplifier design optimization techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 538–547, 2005.

[6] A. A. M. Youssef, K. Sharaf, H. F. Ragaie, and M. M. Ibrahim, "VLSI design of CMOS image-reject LNA for 950-MHz wireless receivers," in *Proceedingsof the 1st IEEE International Conference on Circuits and Systems for Communications (ICCSC '02)*, pp. 330–333, St. Petersburg, Russia, June 2002.

[7] H. Xiao, R. Schaumann, W. R. Daasch, P. K. Wong, and B. Pejcinovic, "A radio-frequency CMOS active inductor and its application in designing high-Q filters," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '04)*, vol. 4, pp. 197–200, Vancouver, BC, Canada, May 2004.

[8] J. A. Macedo and M. A. Copeland, "A 1.9-GHz silicon receiver with monolithic image filtering," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 378–386, 1998.

[9] L. P. Dunleavy, "A Ka-band on-wafer s-parameter and noise figure measurement system," in *Proceedings of the 34th ARFTG Conference Digest-Winter*, vol. 16, pp. 127–137, Lauderdale, Fla, USA, November 1989.

[10] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, chapter 11, Cambridge University Press, New York, NY, USA, 2004.

[11] R. Mukhopadhyay, Y. Park, P. Sen, et al., "Reconfigurable RFICs in Si-based technologies for a compact intelligent RF front-end," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 81–93, 2005.