# MOBILITY ENHANCEMENT OF NANOSCALE BIAXIAL STRAINED SILICON METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

WONG YAH JIN

UNIVERSITI TEKNOLOGI MALAYSIA

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WONG YAH JIN

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## ABSTRACT

Scaling down of Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) devices has been a driving force in IC industry due to high speed and low power requirements. The recent MOSFET devices have been scaled down to 50nm gate lengths where the gate oxide thickness has become thin enough to suppress the short channel effect (SCE). However further scaling down of the MOSFET beyond 50nm will cause the SCE, degrading the current drivability and electron mobility of a MOSFET. Therefore further improvement without minimizing the gate length is strongly required. Strained silicon (Si) is a promising candidate for improving the performance of MOSFET technology without compromising the control of short channel effects since it provides device performance enhancements through changes in material properties rather than changes in device geometry or doping. In this research, the design, fabrication and characterization of high speed and low power performance for 100nm of strain silicon P-type Metal Oxide Semiconductor (PMOS) structures are experimented. With an oxide thickness of 5nm and germanium (Ge) concentration of 30%, the threshold voltage for the strained Si and unstrained structures are -0.74V and -0.96V, respectively. In addition, strained Si shows approximately 20% enhancement in drain current compared to the unstrained structure. The increase of valence band in strained Si as compared to unstrained Si indicates the split of the energy band. This causes holes to increasingly occupy the top band and would increase the mobility of strained Si . The strained Si shows mobility enhancement compared to unstrained structure. Meanwhile, the effect of Ge concentration to strained Si showed that as Ge concentration increased from 20% to 40%, the drain current and hole concentration is increased while the threshold voltage decreased. However moderate Ge concentration must be chosen with suitable strained Si thickness in order to prevent lattice mismatch. The results show that the strained Si critical thickness is 10nm with a 30% Ge concentration for the single channel strained Si. The strained Si exhibits low threshold voltage as the strained Si thickness increases from 5nm to 8nm. Therefore 7nm strained Si thickness was used to create strained Si with 30% Ge concentration. Simulations provide more realistic results and allow researchers to gain a better understanding of the effects of different device parameters on the overall device performance without fabrication.

## ABSTRAK

Pengecilan skala peranti *Metal-Oxide Semiconductor Field Effect Transistor* (MOSFET) merupakan dorongan kuat dalam industri litar bersepadu (IC) untuk memenuhi keperluan kepantasan dan penggunaan kuasa yang rendah. Peranti MOSFET terkini telah diskalakan sehingga panjang salirannya adalah 50nm di mana ketebalan get oksida telah menjadi cukup nipis untuk menyekat kesan saliran pendek (SCE). Walau bagaimanapun, pengecilan MOSFET di bawah julat 50nm akan menyebabkan SCE, dan seterusnya merendahkan kelancaran arus dan kelincahan elektron. Penambahbaikan selanjutnya tanpa memendekkan panjang saliran amat diperlukan. Silikon terik adalah satu calon yang menjanjikan pembaikan prestasi teknologi MOSFET tanpa menjejaskan kawalan terhadap SCE kerana ia memberi penambahan prestasi peranti melalui pengubahan dalam sifat bahan berbanding dengan perubahan dari segi geometri peranti atau pendopan. Dalam kajian ini, rekabentuk dan fabrikasi untuk struktur 100nm silikon terik akan dikaji. Penyelidikan terhadap penambahan kelincahan pada Si PMOS yang terterik telah dilakukan dan dibezakan dengan PMOS yang tidak terterik. Voltan ambang bagi silikon terik and tidak terterik ialah -0.74V dan -0.96V pada ketebalan oksida 5nm dengan 20% kepekatan germanium (Ge). Silikon terik juga menunjukkan peningkatan arus salir sebanyak 20% berbanding dengan silikon tidak terterik. Kenaikan jalur valens pada silikon terterik berbanding dengan silikon tidak terterik menunjukkan jalur tenaga terbahagi. Ini menyebabkan lohong bertambah banyak menetap pada puncak jalur dan meningkatkan kelincahan silicon terterik. Silikon terik mempamerkan peningkatan kelincahan elektron berbanding dengan silikon tidak terterik. Di samping itu, kesan daripada kepekatan Ge kepada silikon terik mempamerkan peningkatan arus salir dan kepekatan lohong bersama dengan penurunan voltan ambang apabila kepekatan germanium meningkat dari 20% hingga 40%. Walau bagaimanapun, kepekatan Ge yang sesuai dengan ketebalan silikon terik perlu dipilih untuk mengelakkan kesan kekisi tak padan. Keputusan juga menunjukkan ketebalan kritikal silikon terik ialah 10nm pada 30% kepekatan Ge. Silikon terik mempamerkan voltan ambang yang rendah apabila ketebalan silikon terik meningkat dari 5nm ke 8nm. Oleh itu, silikon terik dengan ketebalan 7nm dan kepekatan Ge 30% dipilih untuk membentuk silikon terikan. Kaedah simulasi memberi keputusan yang lebih realistik dan membenarkan penyelidik untuk memperolehi pemahamaman yang lebih baik tentang kesan daripada parameter peranti yang berbeza terhadap prestasi peranti tersebut secara menyeluruh, tanpa proses fabrikasi.

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