HGH SPEED SERIAL INPUT/OUTPUT (I/O) TIME AND FREQUENCY CHARACTERIZATION WITH CORRELATION METHOD

NEOH CHAI CHEN

UNIVERSITI TEKNOLOGI MALAYSIA

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ABSTRACT

High Speed serial data bus is developed to support data transfer between the CPU and peripherals on the PC motherboard in future generation applications. At high speed with multi-gigabit, impedance mismatch between the CPU and peripherals becomes critical and limits the possible maximum throughput. This effect can be modeled as a convolution process where the I/O bus behaves as a linear time invariant system that is defined by a channel impulse and frequency response. Since there are variations in the characteristic of the motherboards due to the fabrication and assembly process, it is desired to estimate the impulse response and frequency response of the High Speed I/O bus. Impulse response and frequency response can be used to gate the capability of the motherboard. Correlation method is used to find out channel impulse and frequency response. In order to evaluate the capability of the correlation method under actual manufacturing environment, the evaluation was performed on data collected from actual production test and MATLAB tools will be used for post processing. PCI Express Gen 1 is used to generate high speed data at 2.5Gbps. The results show that there is no difference auto-correlation and cross-correlation in measurement data except the overshoot amplitude and time delay in due to the internal built in equalization technique.

ABSTRAK

Data Bas Kelajuan Tinggi diperlukan untuk penghantaran data antara CPU dan periferal di atas papan utama komputer untuk applikasi masa depan. Dengan kelajuan yang begitu tinggi, iaitu berjuta-juta hantaran dalam satu saat. Keselarasan rintangan electrik antara CPU dan periferal menjadi kritikal dan boleh menhadkan penghatran maksimum data. Kesan ini boleh dimodelkan sebagai proses pendaraban di mana input dan output bus sebagai sistem tak ubah dengan masa dan ciri-cirinya boleh dinyatakan tindak balas delta atau tindak balas frekuensi. Oleh kerana wujudnya pengubah semasa proses perkilangan, pempaparan ciri-ciri dalam tindak balas delta dan frekuensi amat diperlukan untuk kemampuan papan utama komputer. Pengkajian tertumpu kepada proses perkilangan supaya keupyaan cara correlation dapat dinilai dan MATLAB digunakan untuk selepas proses analisis. PCI Express Gen 1 digunakan untuk menghasilkan data lajuan tinggi, iaitu 2.5 giga bit satu saat. Keputusan menujukkan tiada ada perbezaan antara auto-correlation dan cross-correlation kecuali ketinggian overshoot dan time delay.

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CHAPTER 1

INTRODUCTION

High Speed serial data bus is developed to support data transfer between the CPU and peripherals on the PC motherboard in future generation applications such as multimedia, games and broadband networks. For example, Serial Attached SCSI (SAS) is targeting 6Gbps in 2007 [1]. The PCI Express increases from 2.5Gbps to 5Gbps in 2006. At high speed with multi Gbps, impedance mismatch between the CPU and peripherals becomes critical and limits the possible maximum throughput. This effect can be modeled as a convolution process where the I/O bus behaves as a linear time invariant system that is defined by a channel impulse and frequency response. Since there are variations in the characteristic of the motherboards due to the fabrication and assembly process, it is desired to estimate the impulse response and frequency response of the High Speed I/O bus. This information can be used to gage the capability of the motherboard and use it as feedback to the relevant fabrication and assembly processes. Correlation method is used to find out channel impulse and frequency response. In order to evaluate the capability of the correlation method under actual manufacturing environment, the evaluation will be performed on data collected from actual production test of the I/O bus and MATLAB tools will be used for post processing. PCI Express Gen 1 is used to generate high speed data with 2.5Gbps in this project.

1.1 Background

This section discusses the background of the whole project.

1.1.1 Signal Integrity Challenge in High Speed I/O

The basic components that make up a computer system are CPU, memory, I/O and bus that connects them. Bus is a terminology used to describe the interconnecting between the components in the architecture organization. There have three's major busses: the address bus, the data bus, and the control bus. A bus is a collection of wires on which electrical signals pass between components in the system; the source output the components onto the bus, the destination component then inputs this data from the bus. These buses vary from processor to processor. However, each bus carries comparable information on all processors. Due to the increasing complexity of computer architecture, the bus system is much more efficient in less power consumption; less space and fewer pin than direct connect from component to component [2].

Moore's Law drives transistor scaling by 2x for every 21 months. Advanced computer system benefits from the transistor scaling allowing more processing capabilities can be achieved and higher data bandwidth is needed to support the increasing processing power (refer to Figure 1.1). The performance degrades if the computer spends most of its time waiting for the data. The needs of data bandwidth is even critical with the introduction of parallel processing, distribution computing system, multi core CPU and more efficient pipeline architecture while keep cache size smaller size or slower growing rate [3]. Figure 1.2 shows that busses have significant impact on system performance [4].

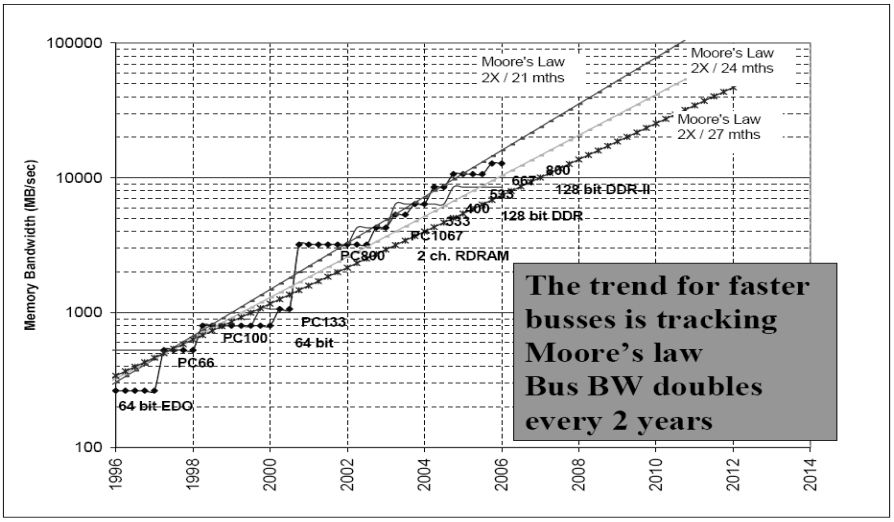

Figure 1.1: Relationship of Moore's Law and Bus Bandwidth (Courtesy of Intel® Corp)

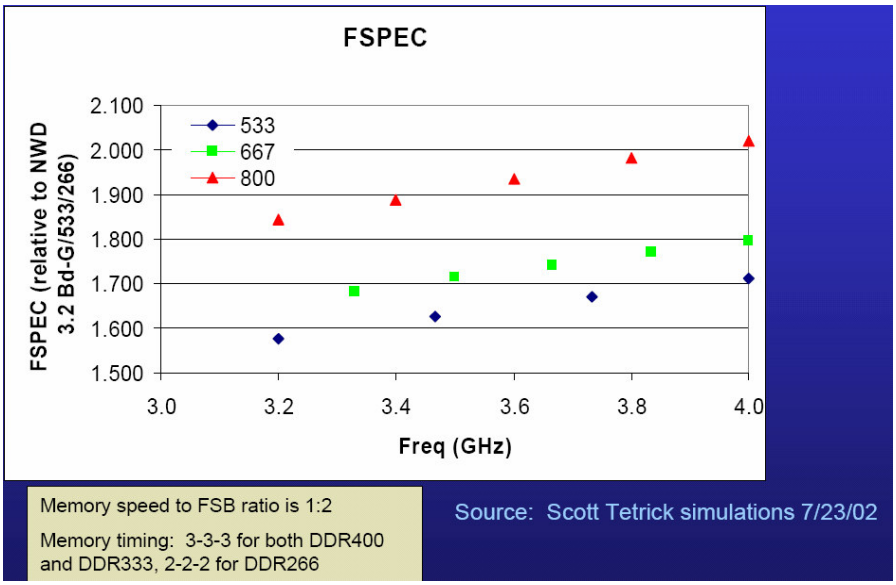

Figure 1.2: Prelim Simulation Data Show Busses Have Significant Impact on System Performance (Courtesy of Intel® Corp)

1.1.2 Transmission Bus Channel on communication point of view

From communication view of point, the transmission bus channel is breaks into blocks, each of which filters the signal (refer to Figure 1.3). The expression for the received signal, $r(t)$, at the input of the receiver is:

$$r(t) = x(t) * h_t(t) * h_c(t) + n(t)$$

$$x(t) = \left\{ \begin{array}{l} x_1(t) = 1, 0 \le t \le T \\ x_1(t) = 0, otherwise \end{array} \right\}$$

$h_t(t)$ = transmitter filter

$h_c(t)$ = channel impulse response

$n(t)$ = noise

$r(t)$ = received signal

*= convolution operation

The receiver output is the convolution of h(t) and x(t) plus noise, n(t).

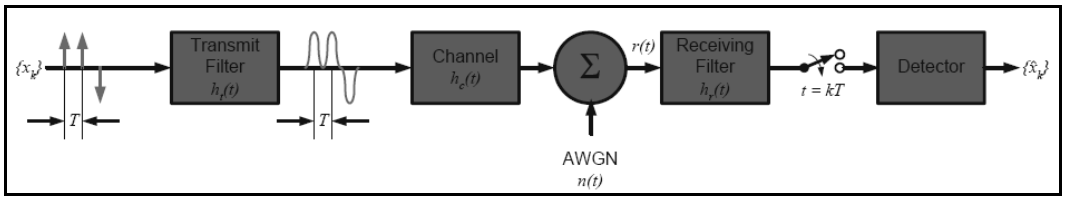

Figure 1.3: Transmission Line from Communication Point of View

For ideal case, the transmission bus channel is behaves as a band limited. We want the amplitude of impulse response of the channel to be constant over this signal bandwidth and phase of the impulse response be a linear function of frequency so that we can get distortion less transmission, and open data "eye". Anyways, in practice, the transmission bus channel is behaves a low pass filter (refer to Figure 1.4) where losses increase with frequency since amplitude of the impulse response not constant and the phase of impulse response not linear. Amplitude and phase distortion cause "smearing" of pulse (ISI) which closes the "eye" diagram [4].

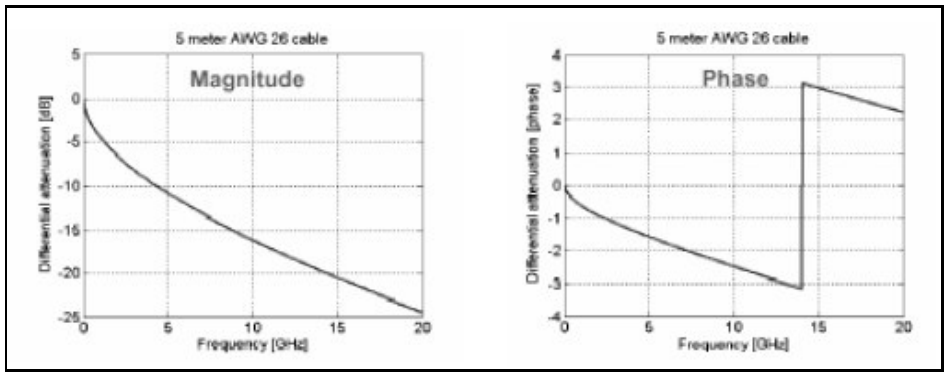

Figure 1.4: Frequency Response of Transmission Line Behaves like a Low Pass Filter

Equalizing filter is added to the channel to improve the signal quality by introducing the inverse characteristic of the transmission bus channel so that both equalizer and channel can cancel each other to retrieve the original transmitting data. The equalizer can be placed at the transmitter, receiver or both. Figure 1.5 is the general taxonomy of equalizer implementation in communication systems. There are basically three domains that equalizer can be designed: digital, analog or mixed signal [5].

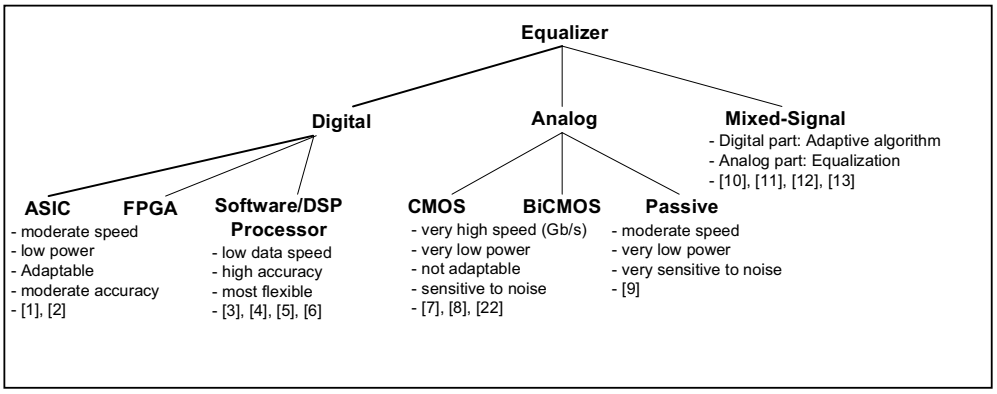

Figure 1.5: Taxonomy of Equalizer Implementation for Communication Systems

1.2 Objective

The objective of this project is to evaluate the performance and parameters of the correlation method in high speed transmission bus channel characterization with data collected from actual production test. The evaluation includes comparison the power spectrum with scattering parameter which collects under real manufacturing environment.

1.3 Scope

This study is focus on system level and excluding any pre-silicon level simulation. The study is based on actual production data and the analysis will be done using simulation software MATLAB. Scattering parameter will be used as a bench-mark. The study focuses on electrical parameters and assumes the transmission bus channel is a time invariant system. Measurement is taken using Textronic Digital Storage Oscilloscope and Network Analyzer.

1.4 Problem Statement

The shared multi-drop bus has been exploits to its full potential. Many techniques have been applied such as increasing the frequency, widening the interface, pipelining transactions, splitting transactions, and allowing out of order completion yet higher data transmission rates require a different strategy. The industry is moving away from parallel buses and relatively slow differential signals toward high speed differential signaling schemes. These high-speed signals solve many design challenges: they offer new levels of bandwidths, they lower overall system cost, and they make designs easier by addressing the skew issues of large parallel buses. However, with these improvements comes a new challenge: maintaining signal integrity. Increasing bus width reduces the maximum achievable

frequency due to varying skew between signals. Increased numbers of signals results in more device pins, printed circuit board (PCB) traces and larger connectors, increasing product cost and reducing the number of interfaces a design can provide. As data frequency and bus width increase, having more than a few devices attached to a shared bus becomes a difficult design challenge. Several factors contribute to the frequency dependent loss of a typical channel. Dielectric loss and skin effect combine to create a significant loss above 1 GHz. With today's serial I/O standards approaching 10 Gbps, this loss become a design issue. As signal travels across a channel, a bit is degraded to the point where it interfaces with neighboring bits; this is known as inter-symbol interference (ISI). The high-frequency components are subject to losses that are greater than the low-frequency components. The edges that contain the high-frequency components are degraded, resulting in added jitter and eye closure. Equalization techniques must be included in the transmitter and receiver circuitry to compensate for the lossy characteristics of the transmission channel due to signal integrity degradation. Conventional method such as Scattering Parameters measurement cannot characterize the bus in active operation condition thus an active bus channel characterization is proposed to resolve the problem

1.5 Research Methodology

The study focus on data collected from actual production test of the I/O Bus and MATLAB tools will be used for post processing. Scattering parameter will be taken using Vector Network Analyzer (VNA) from transmission line start point and end point when the channel does not operate for active bus channel characterization. Refer to Figure 1.6, probing at location A & C. VNA cannot be used for active measurement, discussion will be done in later chapter. Passive elements from transmission bus channel including package, printed circuit board routing, connector and cable are modeled in RLC SPICE format using electromagnetic simulator tool. Ansoft® Maxwell Q2D and Q3D. The simulator captures electromagnetic behavior then transform to RLC matrix elements. Transmission line such as cables and traces are modeled using Q2D assuming energy flows to one direction while Q3D is used for energy flow in 3D. Each component is modeled into RLC or Scattering

parameters matrix. Then they are hook up to build circuit netlist as show in Figure 1.6. For hardware measurement, correlation method can be done by operating the channel in normal mode then measure the transmitter start point and receiver end point.

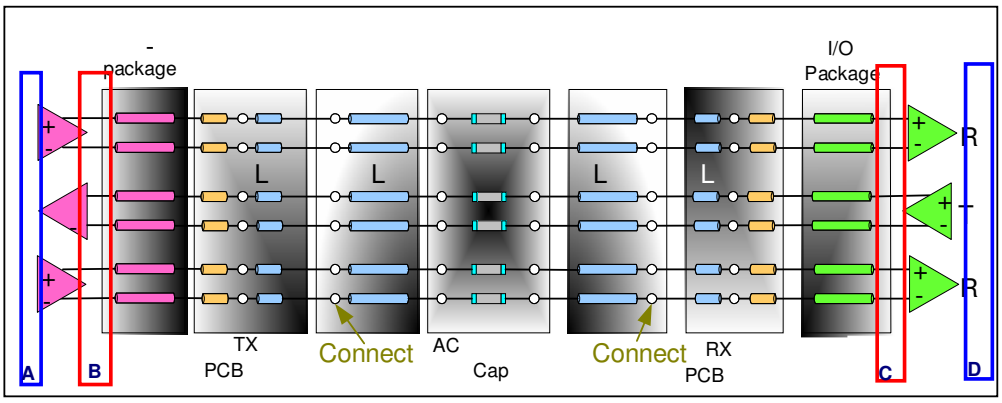

Figure 1.6: Transmission Line Interconnect Circuit Net list (Courtesy of Intel® Corp)

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