DEVELOPMENT OF SINGLE BOARD COMPUTER BASED ON 32-BIT 5-STAGE PIPELINE RISC PROCESSOR

KOAY BOON WOOI

UNIVERSITI TEKNOLOGI MALAYSIA

DEVELOPMENT OF SINGLE BOARD COMPUTER BASED ON 32-BIT 5-STAGE PIPELINE RISC PROCESSOR

KOAY BOON WOOI

A project report submitted in partial fulfillment of the
requirements for the award of the degree of
Master of Engineering (Computer & Microelectronic System)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

NOVEMBER 2009

To my beloved family, friends and lecturers

who have guided and supported me along this journey

ACKNOWLEDGEMENT

In preparing this thesis, I was in contact with many people, researchers and practitioners. They have contributed towards my understanding and thoughts. I would like to take this opportunity to express my deepest gratitude and appreciation to everyone, who helped me along my journey in my Master Project. In particular, I wish to express my sincere appreciation to my thesis supervisor, Professor Dr. Mohamed Khalil bin Hj. Mohd Hani, for encouragement, guidance and inspired me to do better in every aspects. Without his continued support and interest, this thesis would not have been the same as presented here.

My fellow postgraduate students should also be recognized for their support. My appreciation to Lim Jonie and Selva Kumar for their supports in ramp me up on Jonie's previous work.

I am truly grateful to my family members and friends, who motivated and supported me the most throughout this research.

ABSTRACT

In 21st century, embedded system design is a popular alternative to typical microprocessor design as it takes advantage of application characteristics to optimize its design for adequate performance at lower cost. Single Board Computer is a standalone digital system which capable to perform logical computation and data manipulation. Single Board Computer has CPU (Central Processing Unit), memory controller hub and I/O devices controller hub (interface chip) embedded to a single platform such as SoC (System-on-Chip) and embedded system. It is an economical and portable digital system with optimum logic gates and devices utilization. Single Board Computer has capability to synchronize data transfer between CPU and I/O peripheral devices, perform CPU operation as well as running program coded in machine code that utilize all its interfacing hardware devices. This thesis proposes a design of Single Board Computer in Verilog RTL, by extending from previous UTM student's research on 32-bit 5-stage pipeline RISC processor, targeted at FPGA implementation in System-on-Chip (SoC) designs. ISA (Instruction Set Architecture) of RISC(Reduced Instructions Set Computer) processor is enhanced to cover control instruction. I/O controllers are designed to support insertion of input data and display of output data. This Single Board Computer is designed in compact form and generalized to comply with RISC CPU specifications and some basic I/O protocols, which will be a valuable asset in UTM soft core IP bank as to help in its future SoC researches.

ABSTRAK

Pada abad ke-21, rekaan sistem *embedded* merupakan satu alternatif popular kepada rekaan sistem mikro pemprosessan kerana ia direka berdasarkan cara pengunaanya yang spesifik dan ini dapat membantu untuk menghasilkan rekabentuk yang mempunyai fungsi yang memcukupi dengan kos yang lebih murah. Komputer dalam satu platform (*Single Board Computer*) merupakan satu sistem digital yang mampu beroperasi secara tunggal untuk pemprosesan logikal dan data manipulasi. Komputer dalam satu platform ini mempunyai peranti pemprosesan mikro, peranti pengawalan blok ingatan dan peranti pengawalan input dan output seperti rekaan *System-on-Chip* (SoC) dan rekaan sistem *embedded*. Ia merupkan satu rekaan digital yang murah dan mudah-alih dengan pengunaan peranti dan logik yang optimum. Ia berkemampuan untuk melaraskan semua data penghantaran di antara peranti pemprosesan mikro dan peranti persisiran, melaksanakan operasi pengkomputeran dan melaksanakan program yang ditulis dalam bahasa mesin dengan bantuan semua peranti persisiran yang disambungkan kepadanya. Thesis ini melanjutkan penyelidikan pelajar UTM yang lalu yang berasaskan peranti pemprosesan mikro *RISC* dengan 32-bit 5-pipeline untuk menghasilkan sebuah komputer dalam satu platform dengan *Verilog RTL*. Rekaan ini direalisasikan dengan penggunaan FPGA menerusi rekabentuk SoC. ISA (*Instruction Set Architecture*) untuk RISC CPU diperluaskan dengan merangkumi arahan kawalan. Peranti pengawalan input dan output turut direka untuk membolehkan kemasukan data input dan paparan data output.. Rekaan ini memenuhi semua spesifikasi piawai untuk CPU dan peranti persisiran. Ia merupakan suatu asset yang penting kepada UTM dalam penyelidikan SoC.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ALU	-	Arithmetic logic unit
CU	-	Control Unit
DU	-	Datapath Unit
FPGA	-	Field programmable gate array
FSM	-	Finite State Machine
HDL	-	Hardware Description Language
IR	-	Instruction Register
ISA	-	Instruction Set Architecture
LED	-	Light emitting diode
NOP	-	No operation
MAR	-	Memory address register
PC	-	Program Counter
RAM	-	Random access memory
ROM	-	Read only memory
RTL	-	Register Transfer Level
I/O	-	Input and Output
SBC	-	Single Board Computer
RISC	-	Reduced Instruction Set Computer
USB	-	Universal Serial Bus
VGA	-	Video Graphic Array
BCD	-	Binary coded decimal

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

This project report proposes the setup of SBC (Single Board Computer) based on 32-bit 5-stage pipeline RISC processor design[1] via FPGA implementation using Altera DE2 Board. The design is to produce a generic and yet robust processor that works well with various I/O devices to provide adequate logical functions. This chapter covers the background, research motivation, objectives, scope of work, and the report organization.

1.1 Background and Research Motivation

Microprocessor is one of the most revolutional invention in 20^{th} century. In general computing, microprocessor acts as the Central Processing Unit(CPU) that keeps all I/O devices intact together to perform pre-determined task and function stored in memory element. RISC is one of the simple and yet popular processor architectures in computing industry. The design philosophy of RISC processor is to reduce the complexity of the ISA by limiting the instruction set in to a smaller number of more frequently used instruction that yields better efficiency in modern computing.

RISC architecture was first introduced by IBM in 1975. However, RISC designs such as Berkeley's RISC processor and Stanford's MIPS processor which were introduced by respective university research teams were gaining higher popularity in term of public RISC design. Various research efforts and evolutional development of RISC processor throughout the years had made the RISC design to become one of the most sophisticate and successful processor core which are widely used in many application. For instance, ARM processor that dominates the embedded system and smart phone such as PDA and cellular phones by major handset manufacturer such as Nokia and Samsung are originated from RISC architecture. Moreover, MIPS is also found in residential gateways and game consoles like Sony PlayStation. Besides, SPARC, Motorola 88000 and DLX are all inheriting the RISC architecture[2].

SBC (Single Board Computer) are complete computer built on a single circuit board. The design is centered on a microprocessor with memory, I/O and all other features needed to be a functional computer on one board[3]. The recent availability of advanced chip sets providing most of the I/O features as embedded components allows mother board manufacturers to offer motherboards with I/O traditionally provided by daughterboard. This development trend is converging to SBC design especially on those embedded system that requires to be designed in small form factor and lower cost. Besides, the SBC is also improving the user experience as the it is a highly portability digital devices as compared to traditional PC. Furthermore, SBC design is aligned to development of SoC (System On Chip) in semiconductor industry whereby a smaller and more compact digital devices can be placed within a single wafer die with the use of advanced silicon process technology. As a result, SoC design offers great advantage on silicon chip fabrication cost reduction.

In this research, the Single Board Computer of 32-bit 5-stage pipeline RISC processor is implemented on hardware (FPGA) with the interfacing of I/O peripheral devices, which can be booted and execute the pre-programmed instruction based on contents stored in memory module. The target board to be used in this project is Altera DE2 board which is suitable to setup as a SRC (Simple RISC computer) and availability of various on-board I/O devices.

1.2 Objectives

From the discussion from previous section, this report set out objectives as listed at below:

i. To construct Single Board Computer oriented on Altera DE2 board that consists of
   a. RISC processor design implementation via FPGA (Cyclone II 2C35)
   b. On board memory modules: ROM and RAM modules for CPU bootstrapping purpose
   c. I/O devices such as keyboard and LCD display I/O controllers that communicate with RISC CPU core.
ii. To enhance ISA such as J-type instruction for verilog HDL design of 32-Bit 5-Stage Pipeline RISC Processor.
iii. To explore the execution of simple test program via RISC processor that link all I/O and memory modules to perform some simple instruction.

1.3 Scopes of Work

Based on available resources, limited time frame and expertise, this research project is narrowed down to the following scope of work:

i. Verilog code of 32-Bit 5-Stage Pipeline RISC Processor Design will be enhanced with appropriate ISA (Instruction Set Architecture) to support the interconnection of I/O peripheral devices for Single Board Computer setup.

ii. The usage of switches and keyboard as inputs to RISC processor will be developed while on-board LCD display will be enabled as its output. All I/O controller design will be coded in Verilog. Various logic converters are residing in I/O controllers to ensure the input data can be read and stored in memory for RISC CPU processing as well as display the output data in correct format at output devices.

iii. This project involves HDL design, synthesis, simulate and verify the design correctness with Altera Quartus II.

iv. Target implementation is Altera DE2 Board which consists of Cyclone II 2C35 FPGA chip.

v. A simple functional application (written in machine code) that pre-loaded to memory acts as a test case to ensure all interfacing I/O devices are functioning according to their designated functions.

1.4 Significant of Work and Research Contributions

i. I/O device compatibility is a crucial aspect to assure the robustness and functionality of Single Board Computer. A RISC processor core with I/O interfacing capability that coded in Verilog HDL and implemented via FPGA on Altera DE2 board provides great flexibility in future enhancement and allows customization and configuration of Single Board Computer design.

ii. It is important for UTM to have its own 32-bit RISC processor IP thus to enable future Microprocessor / SoC (System On Chip) researches.

iii. Performance of the processor is important thus pipelining is the most viable technique to improve the performance without pushing clock frequency which consumes more power.

1.5 Organization of Project Report

This report is organized into 6 chapters. The outlines of each individual chapter are stated as:

Chapter 1 A brief introduction to RISC processor, project's objectives and scopes and the organization of this project report.

Chapter 2 Background and ISA of RISC processor and literature review on architectural details on bootstrapping technique, memory interface architecture and on-board hardware I/O devices on Altera DE2 board.

Chapter 3 Research and design methodology, verification and validation procedure and tools involved in this project.

Chapter 4 Discussion of architecture for 32-bit 5-stage pipeline RISC Processor IP core. J-type instruction of RISC processor is coded as prerequisite for bootstrapping implementation. Challenges and solutions of this design and ISA enhancement are discussed throughout this chapter.

Chapter 5 Design of PS/2 Keyboard controller, LCD Display Controller and 7-Segment LED Display Controller are discussed in detail. Verilog design implementation of all decoding logics and logic converter sub-modules such as BCD to Integer, BCD to LCD Pattern, Binary to BCD, Keyboard's ScanCode to BCD and etc. are covered.

Chapter 6 Brief discussion on I/O Memory Arbitrator design and its functions. Single Board Computer integration via modular design approach is illustrated and coded in Verilog design.

Chapter 7 Simulation result from Altera Quartus II and on-board hardware testing observation using Altera DE2 board are obtained and analyzed based on RISC CPU Test Case and Basic Calculator Test Case stored in memory blocks. Design functionality, performance and resource utilization studies are reported.

Chapter 8 Conclusion and future works

1.6 Summary of Chapter 1

Project background, objective, scopes of work and significance of research are discussed. The project report organization is also discussed.