THE IMPACT OF FAULT CURRENT LIMITER IN POWER SYSTEM PERFORMANCE

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To my beloved mother and father

who have been my greatest teachers in life

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ABSTRACT

Continues growth of electrical energy demand is resulting in a corresponding increase in the short circuit in power system. Several solutions have been implemented, including the use of Fault Current Limiter (FCL), in order to reduce circuit breakers rated capacity and to limit the electromagnetics stress in associated equipment. This project presents a comprehensive study of the impact of fault current limiter in power system performance. The FCL use for this study is solid-state type because it has advantages in term of flexibility and control over superconducting type. In order to evaluate the impact of fault current limiter in power system performance, simulation model of power system performance with solid-state FCL are used. For simulation model development, MATLAB Simulation Tools: SIMULINK software is used. A distribution system fed from single source is used to assess the impact of FCL to power system performance. The FCL is evaluated in term of its performance in limiting fault current from about 50 kA to a lower value of 1.7 kA. Results show that the solid-state FCL is effective for reducing short circuit currents up to 98% and also can be used to protect busbars from voltage sag when the system is subjected to various types of faults.

ABSTRAK

Perkembangan pesat terhadap permintaan tenaga elektrik telah menyebabkan peningkatan arus kerosakan di dalam sistem kuasa. Pelbagai jalan penyelesaian telah dilaksanakan, termasuk penggunaan penghad arus kerosakan, untuk mengurangkan kapasiti pemutus litar dan menghadkan tekanan elektromagnetik pada peralatan yang berkenaan. Projek ini membentangkan tentang kajian lengkap terhadap kesan penggunaan penghad arus kerosakan pada prestasi sistem kuasa. Jenis penghad arus kerosakan yang digunakan dalam projek ini adalah pengehad arus kerosakan keadaan tepu kerana ia lebih fleksibel dan lebih kawalan berbanding penghad arus kerosakan jenis konduktor lampau. Untuk menilai prestasi sistem kuasa, model simulasi sistem kuasa dengan penghad arus kerosakan keadaan tepu akan digunakan. Untuk pembangunan model simulasi, perisian MATLAB Simulation Tools: SIMULINK akan digunakan. Sebuah sistem pengagihan yang mendapat bekalan elektrik daripada satu sumber digunakan utk menilai kesan penghad arus kerosakan terhadap prestasi sistem kuasa. Prestasi penghad arus kerosakan akan dinilai berdasarkan kebolehan menghad arus kerosakan daripada 50 kA kepada nilai yang lebih kecil iaitu 1.7 kA. Hasil kajian menunjukkan bahawa penghad arus kerosakan mampu menghad arus kerosakan sehingga 98% dan dapat mengurangkan lenturan voltan semasa kerosakan berlaku pada sistem kuasa.

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LIST OF ABBREVIATIONS

FCL	–	Fault Current Limiter
SFCL	–	Superconductor Fault Current Limiter
SSFCL	–	Solid-state Fault Current Limiter
FCLID	–	Fault Current Limiting and Interrupting Devices
SSCB	–	Solid-state Circuit Breaker
V	–	Magnitude of system phase voltage
Z_{FCL}	–	Impedance of current limiting reactor
I_{FCL}	–	Fundamental current of fault current limiter
L_{FCL}	–	Inductance of current limiting reactor
Z_{LOAD}	–	Load impedance
Z_S	–	Source impedance
V_S	–	Voltage source
Pm	–	Power of the motor
Tm	–	Mechanical torque of the motor
f	–	Frequency of the supply
p	–	Number of poles
n	–	Synchronous speed

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CHAPTER 1

INTRODUCTION

1.1 Introduction

In today circumstances, rapid development of power network cause the fault current of the system increased greatly. The levels of fault current in many places have often exceeded the withstand capacity of existing power system equipment. As implication to this matter; security, stability and reliability of power system will be negatively affected. Thus, limiting the fault current of the power system to a safe level can greatly reduce the risk of failure to the power system equipment due to high fault current flowing through the system. Because of that, there is no surprise to fault current limiting technology has become a hotspot of fault protection research since this technology can limit the fault current to a low level.

In power system design view, limiting the fault current to a low level can reduce the design capacity of some electrical equipment in the power system. This will lead to the reduction to the investment cost for high capacity circuit breakers and construction of new transmission line. Consequently, from both technical and economical points of view, fault current limiting technology for reducing short circuit current is needed.

1.2 Project Background

A short circuit cannot be neglected in the power system due to numerous causes. When short circuit occurs in power system, large current will flow in the system which can cause damage to the equipment due to heating effects and electromagnetic forces. Furthermore, during fault, some point in the power system network (depending on the distance of the fault point) will experience voltage sag. This problem may cause to a complete shutdown of healthy plants connected to the network. Power utilities associate that 80-90% of their customers complaining about voltage sags problem [1].

One of the main concerns related with the continuous growth of electricity demand is the corresponding increase in short circuit currents. This matters has been discussed since early 1960s, several solutions based on different principles have been suggested and implemented [2]. Replacing existing switchgear with others of higher rating is certainly a solution this problem. This solution probably is the best to solve this matter which, solving the increment of the switchgear rating problem as well as providing for future growth. However, this is the most expensive of all the other solution and also consumes a lot of time to replace all existing switchgear which leads to reduction of power system reliability for that period of time.

Bus splitting is definitely a cheaper solution to this problem. This entails separation of sources that could possibly feed a fault by the opening of normally closed bus ties, or splitting the existing busses. This effectively reduce the number of sources that can feed a fault, but also reduces the number of sources that supply load current during normal or contingency operating conditions. However, this option may require additional changes in the operational philosophy and control methodology. Furthermore, splitting the bus has implication on network reliability.

Other conventional solution to this matter is sequential breaker tripping. Sequential tripping scheme prevent circuit breakers from interrupting excessive fault currents. If a fault is detected, a breaker upstream to the source of fault current is tripped first. This reduces the fault current seen by the breaker within the zone of protection at the location of the fault. This breaker can then open safely. One of disadvantages of the sequential tripping scheme is that it adds a delay of one breaker operation before final fault clearing. Also, opening the breaker upstream to the fault affects zones that were not originally impacted by the fault. Therefore, a better option is to use FCL.

A questionnaire was sent out in 2003 from CIGRE WG A3.16 asking about the typical structures of distribution systems, type of protection used in the networks and the need of limitation of short circuit currents in MV and HV networks [3]. Based on 53 responds from 14 different countries, 74% shows the needs for short circuit current limitation and only 26% state otherwise. Figure 1.1 shows the pie chart that represented responses from this survey.

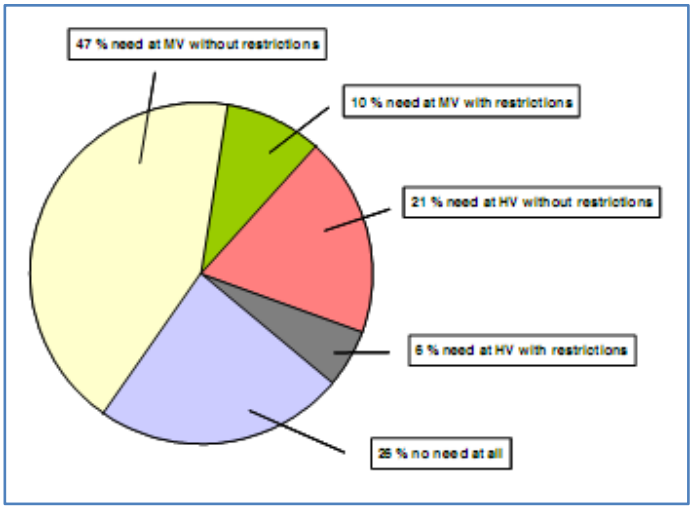

Figure 1.1 – Responses from CIGRE WG A3.16 questionnaire survey

Over the last four decades, different types of FCLs have been under the spotlight in power protection research. In recent years, various types of FCL have been proposed and developed in many countries. Mainly two types of them are discussed most. One is superconductor fault current limiter (SFCL), the other one is solid state fault current limiter (SSFCL). This interest comes not just due to their excellent current limiting characteristics but also due to their positive contribution to the quality of supply [4]. FCLs can be effective in reducing supply outage and mitigate voltage sag on power network.

1.3 Problem Statement

Recent researches show that the implementation of FCL can be used to control the short circuit capacity of power system. Thus, a study needs to be carried out to investigate the performance of power system when using FCL in various conditions [1,5,6];

i) Normal condition
ii) Balanced fault condition
iii) Unbalanced fault condition

Different types of fault can cause voltage sag to healthy busbar in power system network and FCL is the solution to mitigate this issue.

1.4 Project Objective

The objectives of this project are mentioned in the following;

i) To review fault current limiting technologies
ii) To develop a simulation model of SSFCL
iii) To study the power system performance with and without FCL under normal and abnormal condition
iv) To compare the power system performance with and without current limiter
v) To investigate the voltage sag mitigation of the load voltage using FCL

1.5 Project Scope

The scope of this project is limited to the following works;

i) There are two different types of FCL discussed most; Superconductor FCL and Solid-state FCL. In this project, only Solid State FCL will be discussed.
ii) A distribution system fed from a single source radial system is used in this project.
iii) Fault condition used in this project as following;
    a) Single line to ground
    b) Phase to phase fault
    c) Double line to ground fault
    d) Three phase to ground fault

iv) Parameter to be monitored in this study as following;
v) Pre-fault, fault and post-fault current
vi) Bus bar Voltage
vii) MATLAB r2009a: Simulink software will be use to simulate the FCL and the power system model in order to accomplish project's objectives.

1.6 Thesis Organization

This report consists of 5 chapters. In the first chapter, a general introduction about fault current limiter has been presented briefly. Then, the project background, problem statements, objectives and project scope are stated respectively.

Chapters 2, the fault current limiting technology are reviewed and the concepts of general fault current limiter explained. Additionally, the types of fault current limiter and its characteristic are highlighted. In Chapter 3, methodology of SSFCL simulation modeling is explained. This includes the SSFCL mode of operation, its control system, as well as SSFCL model verification. Subsequently, the power system model used for this study is explained at the end of this chapter. Chapter 4 discuss about the results obtained from the simulation model which has been developed in previous chapter. This chapter can be grouped into two major studies; fault current limitation and voltage sags mitigation for different types of fault occurred in power system.

Finally, Chapter 5 concluded the overall works of this project. Moreover, the future works and study are suggested briefly.