NETWORK-ON-CHIP NETWORK ADAPTER

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Specially dedicated to my parents,

family and my beloved wife.

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ABSTRACT

Network-on-Chip (NoC) is a new paradigm for System-on-Chip (SoC) on-chip communication to replace existing bus-based system which is inadequate to cater the growing complexity of SoC. This on-chip design involves a huge number of components that need to communicate with each other to carry their functions, which could affect the design effort, scalability and testability of the SoC in general. This report presents the design and implementation of NoC network adapter which by using Wishbone interface to interconnect IP cores to the network. This network adapter architecture provides four types of best-effort (BE) services to IP core with blocking-type operation. NA segmentizes, packetizes the outgoing data into flits, and sends to router. NA also reassembles and decodes the incoming flits into original data before present them to destination core. NA is designed in Verilog hardware language using Altera Quartus II development software. Functional simulations and performance for each BE types are analyzed to ensure the design can function and meet the objectives and specifications of the project. This architecture uses 575 logic elements and could operate up to 139.74 MHz. This NA dissipates power approximately 90 mW for read operation and 98mW for write operation. NA BE latency depends on type of operations, which vary from 16.5 to 22.5 clock cycles.

ABSTRAK

Network-on-Chip (NoC) telah menjadi satu paradigma baru dalam sistem komunikasi System-on-Chip (SoC). Hal ini adalah kerana, system komunikasi berasaskan bas tidak lagi mampu menampung keperluan SoC yang semakin kompleks. Rekabentuk komunikasi dalam cip membabitkan banyak komponen yang perlu berinteraksi antara satu sama lain untuk melaksanakan fungsi-fungsinya. Dalam erti kata lain, ini sebenarnya akan menyukarkan lagi para pereka bentuk untuk mereka cip, mengecilkan skala penggunaannya dan juga member kesan kepada kesediaan cip untuk pengujian. Laporan ini membincangkan reka bentuk dan implementasi *network adapter* yang mana ia bertindak sebagai perantara yang menggunakan antara muka *Wishbone* untuk menyambungkan *core* kepada rangkaian. *Network adapter* ini dapat melaksanakan empat jenis *best-effort* servis dengan operasi *blocking*. NA menstruktur, memisahkan serta mempakejkan data yang hendak dihantar kepada *router* dalam beberapa *flit*. Di samping itu, NA juga bertindak untuk mencantumkan semula semua *flit* yang masuk kepada data yang asal dan operasi *decode* sebelum dihantar ke destinasi. NA direkabentuk dalam bahasa pengaturcaraan Verilog dengan menggunakan perisian pembangunan Altera Quartus II. Simulasi dan prestasi untuk setiap jenis *best-effort* (BE) di analisis bagi memastikan rekabentuk ini berjaya dan pada masa yang sama, dapat memenuhi objektif-objektif dan spesifikasi projek yang ditetapkan. Rekabentuk ini menggunakan lebih kurang 575 elemen *logic* dan mampu berfungsi pada kelajuan maksimum 139.74 MHz. Operasi baca melepaskan sebanyak 90mW tenaga manakala 98mW tenaga dilepaskan ketika operasi tulis dilakukan. Operasi BE mengambil masa antara 16.5 hingga 22.5 kitaran jam, yang mana masa yang diambil adalah bergantung kepada jenis operasi yang dilakukan.

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LIST OF ABBREVIATIONS

NOC	-	Network-on-Chip
SOC	-	System-on-Chip
NA	-	Network adapter
IP	-	Intellectual property
HDL	-	Hardware description language
FPGA	-	Field programmable gate array
OSI	-	Open system interconnection
GALS	-	Globally asynchronous, locally synchronous
RMW	-	Read-modify-write
FSM	-	Finite state machine
OCP	-	Open core protocol
FIFO	-	First in first out
ASM	-	Algorithmic state machine
GS	-	Guaranteed services
BE	-	Best effort
EOF	-	End-of-flit
AMBA	-	Advanced microcontroller bus architecture

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CHAPTER I

INTRODUCTION

1.1 Introduction

Network-on-Chip (NoC) is a new paradigm for System-on-Chip (SoC) on-chip communication. At present, SoC designs are becoming more complex as many processing elements need to be combined into a single silicon chip [1]. In one particular design alone, there has been a proportionate increment in the number of cores to the number of busses and bridges. This exciting yet challenging fact places direct impact on design effort, scalability, and testability in general. Shared-bus architecture inherits non-scalable characteristic, which means that it is no longer suitable to handle complex communications where hundreds of IP core need to be synchronized and communicated in parallel [2]. Other than that, the increment in the static and dynamic power dissipation in SoC has also placed designers in a tough position. Interconnection is also one of the big issues that need to be addressed. Long delay wire in physical connection makes global distribution of fast clocks more difficult and lead to timing and synchronization problem between different components [2]. NoCs are viewed as one of the solutions [3] to this challenge by adapting the traditional concept of computer networks into on-chip communication systems especially in interconnection aspects in large chip designs. NoC is constructed from multiple point-to-point data links interconnected by routers, such that messages can be relayed from any source module to any destination module over

several links. Routing decisions are made at the routers. The routers and links transport data from one destination to another, and network adapter (NA) decouples communication from computation by providing the intellectual property (IP) cores with a standard interface [4].

1.2 Problem Statement

The main problem in SoC is its interconnectivity. To address this issue, NoC has a reliable solution for this problem. It localizes the big SoC system into smaller systems that executes the tasks completely independent to each other [3]. In term of scalability and network reconfiguration, NoC offers vast opportunity for component reuse and plug-and-play functions [2]. Plug and play capability removes the need to adjust or reprogramming the core to make it works with SoC. In order to achieve this capability, a network adapter with a standardized and well-defined interface to the IP cores is definitely required.

1.3 Project Objectives

The main purpose of this project is to propose an architecture of a NoC network adapter. There are three sub-objectives to be achieved for this project.

(i) To propose a master/slave (duplex) NoC network adapter architecture. This architecture uses Wishbone as standardized communication protocol for attached Intellectual Property (IP) core.

(ii) To implement the master/slave network adapter using Verilog Hardware Description Language (HDL).

(iii) To verify for network adapter to ensure that the intended design specification and functionality are achieved.

1.4 Scope of the Project

The scope of this project covers the network adapter for duplex communication between IP cores in SoC, including their synchronization process. Network adapter only handles four types of best effort packets. There are read request, read response, write request, and write response. Request or response packets are sent to the network in pre-determined flit format that both router and network adapter able to interpret it. Flit is sent one by one to network. To simplify the design, router address is assumed to be similar as core address. Hence, network adapter will not have its own route table. Flits transmission and routing is done by the router. This architecture will be implemented using HDL and synthesis to a *field-programmable gate array* (FPGA) device.

1.5 Thesis Organization

This thesis is organized as follows. Chapter 2 focuses to related literature and previous works. General NoC architecture and components, NoC abstraction layers and the Wishbone protocol are discussed in Chapter 2. Chapter 3 covers the adopted methodology used for this project. This includes the architecture and in-depth explanations of NA implementation. The project result is discussed in Chapter 4. Conclusion and future works are in the last chapter.

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