DESIGN OF TUNABLE DIFFERENTIAL TRANSCONDUCTANCE-CAPACITANCE LOW PASS FILTER

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To my beloved family, friends and lecturers
who have guided and inspired me along this journey.

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ABSTRACT

This project presents the design of a tunable differential transconductance-capacitance (g_m-C) low pass filter for hearing aid application. Low power consumption and transconductor with very low transconductance are the main focus and challenges in this project. Several low transconductance OTA and low power design techniques published are discussed and compared. A differential 3rd order g_m-C low pass filter is designed and characterized at typical process corners and compared with cross skew corners down to layout level design base on TSMC 0.25µm process technology. The active silicon area is estimated to be ~8mm^2 working at 1.35V with a typical hearing aid 1.4V Zinc-air battery. The filter designed dissipates ~12µW and the -3 dB cut-off frequency is 10.5 KHz with -20 dB attenuation at around 22 KHz. Simulation results are shown and are in good agreement with the theoretical results. Tanner Tools S-edit and L-edit are used in this project for schematics and layout design and simulated using Tanner T-Spice simulator.

ABSTRAK

Projek ini menyampaikan sebuah penyelidikan tentang rekabentuk penapis laluan rendah transkonducktans-kapasitans (g_m-C) diferensial untuk aplikasi alat bantuan pendengaran. Matlamat dan cabaran utama dalam rekabentuk ini adalah mencapai penggunaan kuasa yang rendah dengan transkonduktor yang transkonduktansnya sangat rendah. Dalam kajian ini, beberapa kaedah rekabentuk OTA bertranskonducktans rendah dan penggunaan kuasa rendah akan dibincangkan dan dibandingkan. Penapis laluan rendah g_m-C diferensial tahap 3 direkabentuk dan dicirikan untuk berfungsi pada proses silikon tipikal dan juga proses silicon pelbagai kecondongan lain, sampai ke tahap layout berdasarkan teknologi proses TSMC 0.25µm. Keluasan silikon sebenar dianggarkan dalam ~8mm^2, dan rekabentuk ini berfungsi pada tahap voltan 1.35V yang biasanya dibekalkan oleh sebuah bateri Zink-udata 1.4V untuk alat bantuan pendengaran. Penapis ini menggunakan kuasa sebanyak ~12µW dan mencapai lebar jalur -3 dB pada frekuensi 10.5 KHz dengan julat jalur henti -20 dB lebih kurang 22 KHz. Keputusan simulasi dipaparkan, dan didapati bersamaan dengan pengiraan yang berdasarkan teori. Lukisan skematik dan layout dalam projek ini dihasilkan dengan menggunakan Tanner Tools S-edit dan L-edit dan simulasi dilaksanakan dengan menggunakan perisian T-Spice Tanner simulator.

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LIST OF ABBREVIATIONS

g_m - transconducatance
LPF - Low Pass Filter
CMOS - Complementary Metal-Oxide-Semiconductor
BTE - Behind the Ear
ITE - In the Ear
ITC - In the Canal
CIC - Completely in the Canal
AGC - Automatic Gain Control
PDM - Pulse Duration Modulation
SNR - Signal to Noise Ratio
A/D - Analog to Digital
opamp - Operational Amplifier
GBW - Gain Bandwidth
PB - Passband
SB - Stopband
ω_c - Cut-off frequency
ω_s - Stopband frequency
A_{max} - Passband ripple
A_{min} - Stopband attenuation
$F(s)$ - Rational function
$M(\omega)$ - Approximating function
DSP - Digital Signal Processing
OTA - Operational Transconductance Amplifier
CMFB - Common Mode Feedback

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CHAPTER 1

INTRODUCTION

This report is about analog CMOS design of tunable differential transconductance-capacitor (g_m-C) low pass filter (LPF) and its implementation in Research Project II. It includes the research studies on the design challenges of low power analog circuit design with low voltage power supply in CMOS process. A tunable differential g_m-C LPF design is used as an example for the analysis with spice simulation results down to layout level. This chapter includes the background of the project, objectives, scope of work, problem statements, and report organization.

1.1 Background

The design of active filters with very low cut-off frequencies and low power consumption is very important in medical electronics as electrical activity of the human body is relatively low. Hearing aid for instance is an example with strong low voltage and low power specification. Human ear is able to detect frequencies from 20 Hz to 20 KHz and speech normally occurs between 250 Hz to 8 KHz. One of the popular approaches to design low-frequency active filters is g_m-C continuous-time filtering.

Battery technology is also a critical design constraint to portable devices which imposes very low voltage operation (down to 1.1V), thus low power design is essential to prolong the battery life time. According to Oticon product information sheet, current standard hearing aid product battery life time is around 60-220 minutes with a typical hearing aid 1.4V Zinc-air battery. Besides, high programmability is desired to fit different products (i.e. Behind the Ear (BTE), In the Ear (ITE), In the Canal (ITC), and Completely in the Canal (CIC)), and the CMOS technology process variations.

A general block diagram description of a hearing aid is shown in Figure 1.1 (Francisco Serra-Graells, Lluis Gomez and Oscar Farres, 2001). The transducer at the front end is used to adapt the impedance of different input sources such as electrets microphone, telecoil and direct audio connector and mix them according to programmable weights. The curvilinear and adaptive AGC next to the transducer are used to modify the signal dynamic range according to the user loss through Compression Ratio and Threshold Knee Point parameter. Some high pass filter and low pass filter are inserted along the chain with selectable corner frequencies and filter orders apart from the inherent filtering in the AGC loop which is the portion that will be designed in this project.

The overall system application is set by the volume control and the programmed user pain threshold is controlled by the output power limit. The low-impedance receivers are driven by the Class-D output amplifier, which must be based on frequency programmable Pulse Duration Modulation (PDM) to minimize quiescent consumption and high frequency losses. Finally, the control processor optimizes the overall SNR by adjusting automatically G_{AGC} and G_{VOL}.

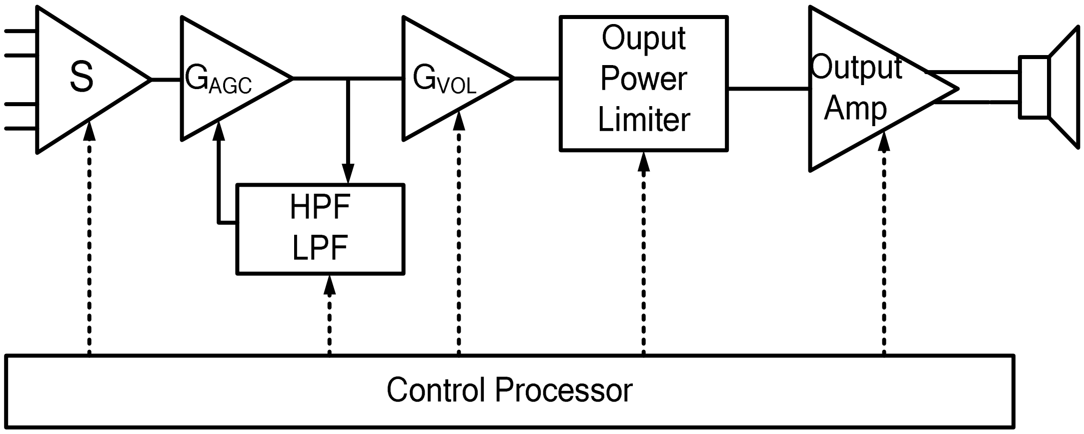

Figure 1.1: General block description of Hearing Aid

1.2 Objectives

The objective of this project is to design a low power and low frequency tunable differential g_m-C (LPF) for hearing aid application, this is done at TSMC 0.25 µm process typical corner and compare with the cross skew corners down to layout level design.

1.3 Scope of Work

The scope of this research project involve research studies on various methods to realize on chip filter design approaches and then design a low power and low frequency g_m-C LPF for hearing aid applications. The design is characterized at typical process corner down to layout level design base on TSMC 0.25 µm process technology. Tanner S-edit and L-edit are used in this project for schematics and layout design and simulate using Tanner T-Spice simulator.

1.4 Problem Statements

In recent CMOS processes, continual decreases of minimum transistor dimensions and the supply voltage are mainly driven by the performance of digital systems. This trend has successfully increases the transistor performance (speed) and at the same time reduces the cost with smaller die area and lower power consumption. However, the performance of analog or mixed-signal circuits such as phase-locked-loops, power-on-resets, analog-to-digital (A/D) converters, filters and other analog circuits in newer CMOS generations does not necessarily improve as in digital circuits.

Anne-Johan Annema (1999) shows that the power consumption decreases down to about the 0.25-0.35 μm CMOS generations and increases with the newer CMOS generations thereafter by maintaining the analog circuit performance. Besides, the capacitance is not scaling at the same scale as technology causing dynamic power per unit area increases which also add up into the power cost. Hence, low supply voltage in newer CMOS process is one of the main limiting factors of analog circuit or performance feasibility.

The design of very low frequency filters is not straightforward, especially for integrated circuit implementations where chip realization of large time constants is needed, which imply large capacitors and very low transconductances. There are two entirely independent angles to the problem that need to be solved in a g_m-C LPF with low cut-off frequency ($g_m/2\pi C$).

One of it is OTA with very low transconductance (order of nA/V) where very small current is required, they are usually not easy to generate and not well controlled. In order to generate small current for the biasing circuit, transistors with very long channel length (L) are required which is hard to match in layout. The other issue is the realization of very large capacitors (order of nF) on chip, however passive components are very sensitive to process and temperature variations. Besides, driving huge load capacitor requires an operational amplifier (opamp) with very high Gain Bandwidth (GBW) in order to meet the required cutoff frequencies, several important opamp architectures will be discussed in the latter chapters and compared their performances.

In addition, low supply voltage also is a critical design challenges in this project as the nominal voltage supply of TSMC 0.25µm process is at 0.25V. This project is intend to design the filter operating at 1.35V which reduces the headroom for the opamp and requires high precision biasing circuits to maintain the filter performance.

Also, high linearity is required to suppress the distortion to the output, hence feedback and cancellation techniques are required to reduce distortion especially at low supply voltages.

1.5 Report Organization

Chapter 1	Give a brief introduction to the g_m-C LPF design for hearing application and the project's objectives and scope.
Chapter 2	Literature review on the techniques of low power and low frequency g_m-C LPF realization and g_m tuning technique.
Chapter 3	Definition of the filter design specification. Design methodology used in this project to realize the top level tunable differential g_m-C LPF design all the way from transconductance cell design and simulation modeling.
Chapter 4	Spice pre-layout and post layout simulation result and analysis.
Chapter 5	Conclusion and future suggestion for enhancements.

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