CLASSICAL AND DAMAGE MECHANICS-BASED MODELS FOR LEAD-FREE SOLDER INTERCONNECTS

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A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Engineering (Mechanical)

Faculty of Mechanical Engineering
Universiti Teknologi Malaysia

DECEMBER 2009

To my beloved parents and family

ACKNOWLEDGEMENT

First and foremost, I would like to express my heartfelt appreciation to my respectful supervisors, Prof. Dr. Mohd. Nasir Tamin and Dr. Nazri Kamsah for their invaluable advice and supervision throughout this research. The same credit also goes to Dr. Loh Wei Keat from Intel Technology (M) Sdn. Bhd.. They have spared their precious time for me and guided me with their knowledge and experiences diligently. Without their outstanding academic and industrial supports, the completion of my project would not be possible.

Grateful acknowledgement is also made for financial support by INTEL Technology Malaysia through UTM-INTEL contract research grant No. 68709.

Apart from this, I am thankful to Computational Solid Mechanics Laboratory (CSMLab) members who have shared valuable information, knowledge and thought with me generously. It helps me to solve a lot of problems and difficulties. Their constructive ideas and opinions are also making this research a success indirectly.

Last but not least, further gratitude is forwarded to my beloved family members and friends for their continuous supports and encouragements throughout these years. Most important of all, a special thank to my dearest parents. I am greatly indebted to them for their unconditional love and ever-loving care toward me.

ABSTRACT

Solder joint reliability (SJR) is the key concern in electronics packaging, primarily for ball grid array (BGA) packages. It affects the overall performance and reliability of electronics devices. In this project, the response of Sn-4.0Ag-0.5Cu (SAC405) lead-free solder joints in a typical BGA package is examined. Finite element (FE) analysis is employed along with published experimental data in establishing a thorough understanding of the mechanics and failure process of the solder joints. The accuracy of FE results for SJR is highly dependent on the solder constitutive behavior prescribed in the analysis. In the respect, unified inelastic strain theory (Anand model) is employed with model parameters extracted from series of published tensile tests data at different temperatures and strain rates. The model is refined further to ensure better predictive capability. The SJR of a BGA test package subjected to solder reflow process and temperature cycles is examined. The critical solder joint is identified at location near to the die corner. The highest stress and inelastic strain magnitudes are calculated at the component side of the solder/intermetallics compound (IMC) interface. Stress-strain hysteresis suggested that solder joint fatigue is primarily contributed by localized shear effect. Both strain- and energy-based life prediction models have been developed for the accelerated reliability cycles. The failure process of solder/pad interface under applied monotonic loading is described. In this respect, the Cohesive Zone Model (CZM) is evaluated within the FE framework to simulate the relatively brittle interface. Materials parameters for CZM are established based on published data of solder ball shear tests. It was found that localized cracking of the solder/pad interface in lead-free solder joints under shear test setup is initiated by tensile stress field due to shear tool clearance.

ABSTRAK

Kebolehpercayaan sambungan pateri (*SJR*) adalah faktor penting dalam pembungkusan elektronik, terutamanya bagi pakej *ball grid array* (*BGA*). Ia mempengaruhi prestasi dan kebolehpercayaan keseluruhan alat elektronik. Dalam projek ini, gerakbalas sambungan pateri bebas plumbum *Sn-4.0Ag-0.5Cu* (*SAC405*) dalam pakej *BGA* biasa dikaji. Analisis unsur terhingga (*FE*) digunakan bersama dengan data eksperimen yang telah diterbitkan untuk mendapatkan pemahaman lengkap sifat mekanik dan proses kegagalan sambungan pateri. Ketepatan keputusan *FE* bagi *SJR* sangat bergantung kepada perilaku konstitutif pateri yang digunakan dalam analisis. Dalam hal ini, teori penyatuan terikan tak anjal (model *Anand*) digunakan. Parameter model diekstrak daripada siri data ujian tegangan pada pelbagai suhu dan kadar terikan yang telah diterbitkan. Model diperbaiki lagi bagi memperolehi keupayaan ramalan yang lebih baik. *SJR* pakej ujian *BGA* yang dikenakan dengan proses *reflow* pateri dan kitaran suhu dikaji. Sambungan pateri kritikal dikenalpasti terletak berhampiran dengan penjuru *die*. Magnitud tegasan dan terikan tak anjal yang paling tinggi didapati di permukaan pateri/lapisan sebatian antara logam (*IMC*) di bahagian komponen. Histeresis tegasan-terikan menunjukkan bahawa lesu sambungan pateri kebanyakannya disumbangkan oleh kesan ricih setempat. Kedua-dua model ramalan hayat yang berdasarkan terikan dan tenaga telah ditubuhkan bagi kitaran kebolehpercayaan yang dipercepatkan. Proses kegagalan di permukaan pateri/*pad* dibawah pembebanan *monotonic* dikaji. Dalam hal ini, *Cohesive Zone Model* (*CZM*) digunakan di dalam rangka kerja *FE* untuk mensimulasikan lapisan antara muka yang agak rapuh. Parameter bahan bagi *CZM* diperolehi berdasarkan data ujian ricih bola pateri yang telah diterbitkan. Terdapat retak setempat di permukaan pateri/*pad* dalam sambungan pateri bebas plumbum bagi ujian ricih yang dimulakan dengan kawasan tegasan tegangan yang disebabkan oleh toleransi alat ricih.

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LIST OF ABBREVIATIONS

BGA	-	Ball Grid Array
BK	-	Benzeggagh-Kenane
C4	-	Controlled Collapse Chip Connection
CTE	-	Coefficient thermal expansion
CZM	-	Cohesive zone model
ENIG	-	Electroless Nickel Immersion Gold
FC	-	Flip-Chip
FCBGA	-	Flip Chip Ball Grid Array
FE	-	Finite element
FSCSP	-	Folded Stacked Chip Scale Package
IC	-	Integrated circuit
IMC	-	Intermetallics compound
NSMD	-	Non-solder mask defined
OSP	-	Organic Solderability Perservative
PBGA	-	Plastic Ball Grid Array
PCB	-	Printed circuit board
PDA	-	Personal digital assistant
PGA	-	Pin Grid Array
PTH	-	Plated Through Hole
SAC	-	Sn-Ag-Cu
SAC405	-	Sn4.0Ag0.5Cu
SJR	-	Solder joint reliability
SMT	-	Surface Mount Technology
SMD	-	Solder mask defined

LIST OF SYMBOLS

E	-	Young's modulus
N_f	-	Number of cycle to failure
UTS	-	Tensile strength
σ_y	-	Yield stress
v	-	Poisson's ratio
T_L	-	Liquidus melting temperature
T_S	-	Solidus melting temperature
ε_T	-	Total strain
ε_e	-	Elastic strain
ε_{in}	-	Total inelastic strain
ε_p	-	Time-independent plastic strain
ε_{Cr}	-	Time-dependent creep strain
ε_{vp}	-	Time-dependent visco-plastic strain
$\dot{\varepsilon}_p$	-	Inelastic strain rate
σ	-	Stress
T	-	Temperature
s	-	Anand model internal variable
s_0	-	Anand model initial value of internal variable
Q/R	-	Anand model activation energy
A	-	Anand model pre-exponential factor
ξ	-	Anand model stress multiplier
m	-	Anand model strain rate sensitivity of stress
h_0	-	Anand model hardening coefficient
$\hat{s}$	-	Anand model coefficient for deformation resistance saturation. value
n	-	Anand model strain rate sensitivity of saturation value

a	-	Anand model strain rate sensitivity of hardening coefficient
s^*	-	Anand model saturation value of internal variable
G & i	-	Parameters of strain-based fatigue model
H & j	-	Parameters of energy-based fatigue model
$\varepsilon_{in,acc}$	-	Acumulated inelastic strain per cycle
$W_{in,acc}$	-	Acumulated plastic work density per cycle
$\Delta\sigma$	-	Total stress range
$\Delta\varepsilon$	-	Total strain range
$\Delta\varepsilon_e$	-	Total elastic strain range
$\Delta\varepsilon_p$	-	Total inelastic strain range
δ	-	Separation
δ^F	-	Separation at failure
δ_{pp}	-	Separation at failure for perfectly plastic criterion
δ_{pro}	-	Separation at failure for progressive softening criterion
δ_{lin}	-	Separation at failure for linear softening criterion
δ_{Ne}	-	Separation at failure for Needleman criterion
δ_{reg}	-	Separation at failure for regressive softening criterion
G_C	-	Critical fracture energy
δ_e	-	Elastic extension
P	-	Force
L	-	Thickness
R	-	Area
σ_C	-	Material strength
K_p	-	Stiffness
δ_0	-	Separation at damage initiation
D	-	Damage
S_n	-	Cohesive element normal stress
S_{s1}	-	Cohesive element shear stress at direction-1
S_{s2}	-	Cohesive element shear stress at direction-2
S_n^0	-	Cohesive element tensile strength
S_{s1}^0	-	Cohesive element shear strength at direction-1
S_{s2}^0	-	Cohesive element shear strength at direction-2
C	-	Failure envelope parameter
G_I	-	Mode I strain energy release rate

G_{II}	-	Mode II strain energy release rate
G_{IC}	-	Mode I critical strain energy release rate
G_{IIC}	-	Mode II critical strain energy release rate
η	-	BK mixed-mode parameter
S_s	-	Cohesive element resultant shear stress
K_n	-	Cohesive element tensile modulus
K_s	-	Cohesive element shear modulus
p	-	Quadratic coefficient of quadratic equation
q	-	Linear coefficient of quadratic equation
r	-	Constant coefficient of quadratic equation
Δ	-	Discriminant of quadratic equation
U_y	-	Displacement in axis-Y
UR_x	-	Rotation about axis-X
UR_z	-	Rotation about axis-Z
U_x	-	Displacement in axis-X
UR_y	-	Rotation about axis-Y
UR_z	-	Rotation about axis-Z
R_{SR}	-	Reflow cooling rate
ΔT	-	Range of temperature cycles
T_{TC}	-	Ramp rate of temperature cycles
t_{dwell}	-	Dwell time
σ_{vm}	-	von Mises stress
τ_{13}	-	Shear stress at direction-13
τ_{23}	-	Shear stress at direction-23
σ_{33}	-	Normal stress at direction-33
φ	-	Damage

CHAPTER 1

INTRODUCTION

1.1 Background of Study

Several studies have been carried out in addressing solder joint reliability (SJR) issues at the computational solid mechanics laboratory (CSMLab), UTM. These include determination of solder material constitutive inelastic behavior [1] and assessment of SJR by predicting the fatigue lives of solder joint in electronic assembly using strain- and energy-based approaches for loadings of temperature cycles, cyclic twisting and cyclic bending [2]. It continued by the determination of solder/intermetallics compound (IMC) interface behavior and modeling of solder ball shear test [3]. All of those studies are preformed on Sn-40Pb (leaded) solder material. The current study is a continuation of those projects and on Pb-free solder alloy.

In this study, some of those previous methods are employed, but for lead-free solder material since the leaded solder material has gradually been substituted by lead-free solder material due to health and environmental concerns. In comparisons to those previous works, several improvements have been made. These include the establishment of new modified Anand model for improving the prediction of solder joint inelastic behavior, development of solder joint life prediction models utilizing the material model established in the current study, and improvement of cohesive zone model (CZM) for simulating solder joint interface fracture.

1.2 Overview

In the year of 1965, Gordon Moore dictated that the number of transistor in an integrated circuit (IC) will be doubled every year. After that, he changed it to every 18-24 months. The prediction of Moore's Law, as shown in Figure 1.1, is still applicable today. Besides that, he also forecasted that the coming 20 years trend will still follow the Moore's Law [4]. IC with higher transistor number has faster data processing speed. This type of IC is designed for more advanced electronics device usage. Consequently, the heat dissipation in modern IC has been rapidly growing along with rising of transistor number and clock frequency.

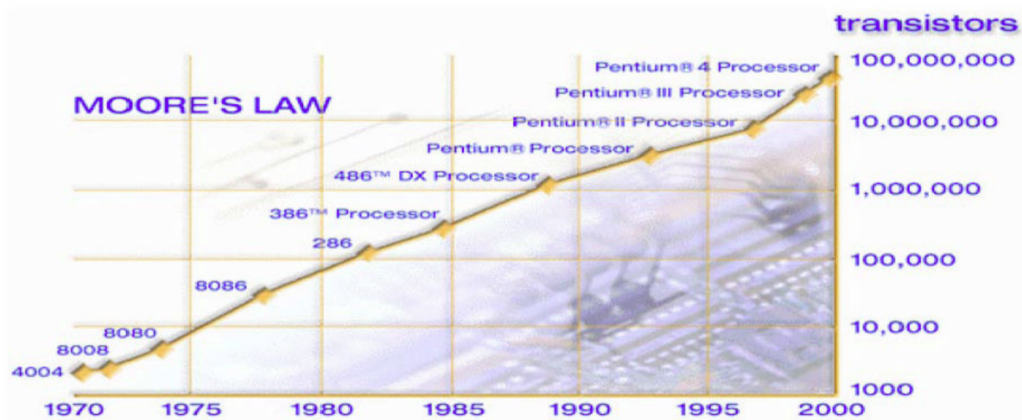

Figure 1.1: Intel CPU transistors double every ~ 18 months [5]

Another significant trend is the combination of various functionalities in a single electronics device or system. For example, new generation personal digital assistant (PDA) and mobile phone offer a range of functionalities such as computing, communication, photography, web browsing, etcetera. It means that extra functionalities are added into the electronics package and assembly. Soon, ideas of die stacking, package stacking and device integration are introduced to produce electronics package and assembly that can provide more functionalities. As a result, more complex and compact type of electronics package and assembly will be available. The insertion of additional functionality in a smaller package will induce higher heat density [6]. For instance, Folded Stacked Chip Scale Package (FSCSP), as shown in Figure 1.2, is known as next generation package that will be developed to combine multiple memory and logic chips into a single package.

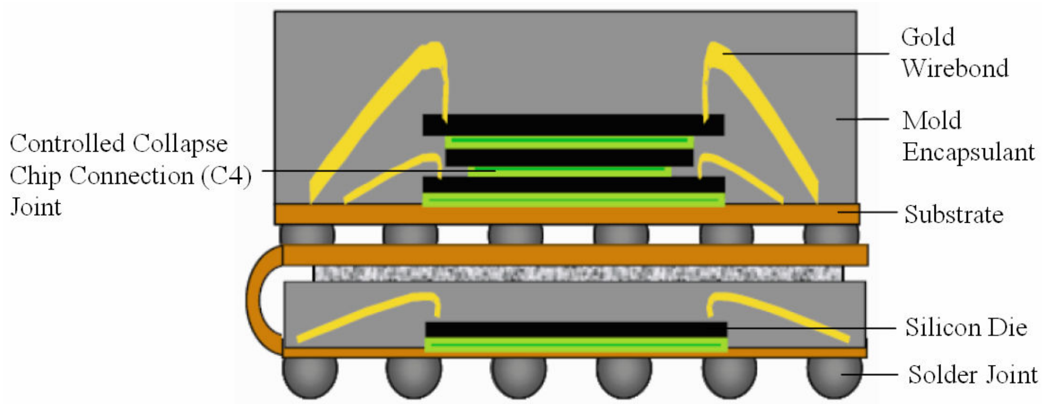

Figure 1.2: FSCSP electronics package [7]

In addition to those trends, it is believed that leaded solder material will gradually be replaced with lead-free solder material in the future. Sn-Pb (Leaded) material is the main choice for the solder joint interconnection in the past. It is because it has few good material properties such as reflow properties and low melting temperature [8]. But soon it will be substituted by lead-free solder material due to the environmental and health issues. Japan, Europe and U. S. already took some actions to ban or reduce the usage of leaded material as solder joint interconnection [9].

Those electronics packaging trends mentioned above put higher requirements on electronics packaging technology. These trends aggravate the SJR issue. The followings are some of the explanations:

1. Heat is unavoidable for electronics assembly due to increasing of clock frequency and higher heat density in the future. Unfortunately the coefficient thermal expansion (CTE) mismatch of electronics assembly that caused by heat will influence the reliability of solder joint interconnection.
2. Smaller electronics part such as solder joint interconnection will be introduced to meet the demands of more connections, smaller pitch and compact size of electronics package. The trends of pin count and pitch are illustrated in Figures 1.3 and 1.4. During the manufacturing process or usage of the electronics assembly, the solder joint connection is probably exposed to several mechanical loadings such as cyclic temperature, bending cycles and drop impact. Those mechanical loadings are critical especially for small tiny

solder joint. It is no doubt that smaller solder joint connection will face higher risk of mechanical failure such as fracture.

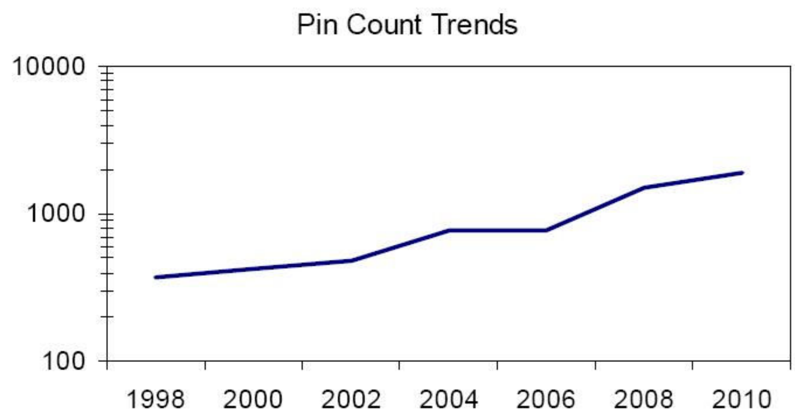

Figure 1.3: Pin count trends [10]

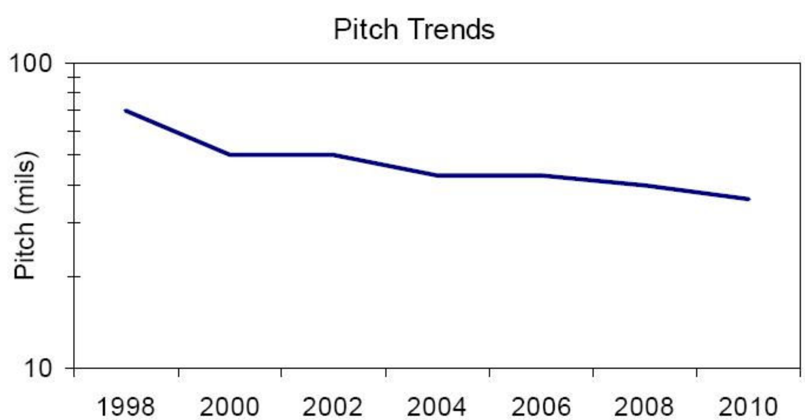

Figure 1.4: Pitch trends [10]

3. Changing of solder material from leaded type to lead-free type weakens the solder joint in the electronics assembly. It is believed that Sn4.0Ag0.5Cu (SAC405) lead-free solder alloy demonstrating a greater susceptibility to brittle fracture than Sn-Pb (Leaded) solder [11]. Besides that, lead-free solder material requires reflow profile with higher peak temperature (260 ^{o}C) compared to leaded solder material (230 ^{o}C). It is because lead-free solder material has higher liquidus temperature, T_L (217 – 219 ^{o}C) than leaded solder material (183 ^{o}C) [12]. So, it will lead to higher initial deformation (warpage) of electronics assembly and larger residual stress and strain at the solder joint connection after the reflow process.

1.3 Problem Definition

A good design of electronics packaging and material selection can ensure that the circuit works properly and increase the reliability of electronics products. Among mechanical failures found in the electronics assembly include die cracking, solder joint fracture, underfill/substrate delamination and underfill/die delamination [13]. Based on Gibson *et al.* [14] paper, 70% of failures in electronics components are the fracture of the solder joint. Thus, this project focused on SJR issues. Since the solder joint is small and electronics device is expensive, electronics assembly experimental tests such as cyclic temperature, drop impact and vibration are often time consuming and involving high cost. Finite element (FE) analysis is an alternative method for investigating the SJR issues. By using FE analysis, the mechanics behavior of small solder joint such as distributions and evolution of stress and strain can be predicted. Besides, FE simulation results can be used to predict the solder joint fatigue life and solder joint interface strength. Good solder joint material model is needed because the accuracy of FE simulation results is highly dependent on material constitutive model, accurate geometry, loading conditions and boundary conditions employed in the FE model. Existing studies on leaded solder material such as solder joint material models, life prediction models and interfacial damage models need to be re-evaluated for lead-free solder material.

1.4 Objectives

The objectives of this study are:

1. To determine the unified inelastic strain model parameters for lead-free solder material.
2. To develop a predictive FE model for life prediction of solder joint in BGA package under prescribed loading conditions.
3. To determine the damage mechanics-based model parameters for describing solder/pad interface failure process.

1.5 Scope of Work

The present study focuses on SJR issues and is limited to the following scope of work:

1. SAC405 alloy is used as a demonstrator lead-free interconnect material.
2. Published experimental data of lead-free solder material is gathered for verification and validation purposes.
3. Unified inelastic strain model (Anand model) for describing the response of solder material is refined for Pb-free solder joints.
4. Flip Chip Ball Grid Array (FCBGA) electronics packages with typical dimensions are used in FE modeling for predicting SJR.
5. CZM is evaluated for application in predicting fracture of solder/pad interface system.