FAST FOURIER TRANSFORM MODULE FOR IMPLEMENTATION IN NIOS II EMBEDDED PROCESSOR

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Specially dedicated to

my beloved mother and father

“Only those who dare to fail greatly, can ever achieve success greatly”

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ABSTRACT

The Fast Fourier Transform is an indispensable algorithm in many digital signal processing applications but yet is deemed computationally expensive cost when designed it on hardware. This thesis proposes a design and implementation of Fast Fourier Transform algorithm in embedded system by utilize it in Nios II embedded processor and integrate with Nios II floating point custom instruction. The design is based on Decimation-In-Time and Decimation-In-Frequency radix-2 for the better performance and speed. Hardware implementation, the ALTERA CYCLONE II EP2C35F672C6 (DE2 board) is used. Hardware interfacing, Graphical User Interface (GUI) has been developed using MATLAB software; it's an original method for interfacing between ALTERA Field Programmable Gate Array (FPGA) and software in host PC. Input values are sent from MATLAB to ALTERA development board via serial port and the calculation data return back to MATLAB. The purpose of this technique is take advantages of the MATLAB in analysis and plot the result.

ABSTRAK

Penukaran Pantas Fourier merupakan suatu algoritma yang mustahak dalam kebanyakan aplikasi pemprosesan isyarat digital dan hanya dianggap sebagai suatu kos pengiraan yang tinggi bila ia direka bentuk dalam sesuatu “hardware”. Tesis in mencadangkan suatu corak dan implementasi algoritma Fast Fourier Transform dalam system yang terikat dan diaplikasikan di dalam prosessor Nios II dan dintegrasikan dengan arahan khas titik terapung Nios II. Corak tersebut adalah berasakan Decimation-In-Time dan Decimation-In-Frequency radix-2 untuk mendapatkan hasil yang lebih bermutu dan cepat. Dalam implementasi “hardware”, ALTERA CYCLONE II EP2C35F672C6 (DE2 board) digunakan. “Hardware interfacing “,Antaramuka Grafik Pengguna telah dikembangkan dengan menggunakan “software” MATLAB; ia adalah kaedah tulen untuk mewujudkan sesuatu ruang hubung kait antara ALTERA Field Programmable Gate Array (FPGA) dan “ hos software” dalam PC. Nilai input dihantar dari MATLAB ke ALTERA development board melalui port serial dan data pengiraan pula dihantar balik ke MATLAB. Tujuan teknik ini digunakan adalah untuk meggunakan faedah MATLAB dalam analisis dan untuk mengeplot hasil / keputusan yang diperoleh.

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CHAPTER 1

INTRODUCTION

This thesis proposes a design of Fast Fourier Transform and applies it into Nios II Embedded Processor. This chapter covers the motivation, problem statement, project objectives, scope of work, project contributions and finally thesis organization.

1.1 Motivation

The Fast Fourier transform is a critical tool in digital signal processing where its value in analyzing the spectral content of signals has found application in a wide variety of applications. The most prevalent of these applications is being in the field of communications where the ever increasing demand on signal processing capabilities have given rise to the importance of the Fourier transform to the field. However, the Fourier transform is a part of many systems in a wide variety of industrial and research fields. Its uses range from signal processing for the analysis of physical phenomena to analysis of data in mathematical and financial systems.

The majority of systems requiring Fourier transforms are real time systems which necessitate high speed processing of data. Given the complexity in performing The Discrete Fourier, the implementation of high speed Fast Fourier transform has required the use of dedicated hardware processors. The majority of high performance Fourier transforms has required the use of full custom integrated circuits and has typically been in the form of an application, specifically integrated circuit. Although much work has been put into raising performance while reducing hardware requirements, and also cost, the cost of full custom hardware still limits the availability of Fourier transform hardware to low volume production.

Nevertheless the development of programmable logic hardware has produced devices that are increasingly capable of handling large scale hardware. High density field programmable gate arrays (FPGA) that are already available in the market can boast upwards of 180,000 logic elements, nine megabits of memory, and on board processors.

The use of FPGA in implementing hardware eliminates the need for the long and costly process of creating a full custom integrated circuit and the time and cost of testing and verification. Saving cost in designing, testing, and time from design to a functional device.

These features of the FPGA make it especially attractive for the purpose of creating embedded processors for research and development purposes.

However the design of any of embedded processors must consider two important factors efficiency and flexibility for reaching an ideal design.

1.2 Problem Statement

Efficiency and flexibility are two of the most important driving factors in embedded system design. Efficient implementations are required to meet the tight cost, timing, and power constraints present in embedded systems. Flexibility, albeit

tough to quantify, is equally important; it allows system designs to be easily modified or enhanced in response to bugs, evolution of standards, market shifts, or user requirements, during the design cycle and even after production.

Various implementation alternatives for a given function, ranging from custom-designed hardware to software running on embedded processors, provide a system designer with differing degrees of efficiency and flexibility. Unfortunately, it is often the case that these are conflicting design goals. While efficiency is obtained through custom hardwired implementations, flexibility is best provided through programmable implementations.

Hardware/software partitioning separating a system's functionality into embedded software (running on programmable processors) and custom hardware (implemented as coprocessors or peripheral units) is one approach to achieve a good balance between flexibility and efficiency.

1.3 Project Objectives

The aims of this project are as follow:

1. Design and implementation of Fast Fourier Transform (FFT) algorithm into embedded system by:

    a) Utilizing Nios II embedded processor.
    b) Integrating it with Nios II Floating Point Custom Instruction.

2. Developing MATLAB user interface to verify the proposed FFT system.

1.4 Scope of Work

Taking into account the resources and time available, this project is narrowed down to the following scope of work.

1. This project only considers 32 point FFT floating point. The Decimation-In-Time (DIT) algorithm is chosen.
2. The algorithm is implemented in C++ language.
3. Floating Point Custom Instruction is targeted for Nios II platform and implemented in ALTERA Cyclone II DE2 board.
4. MATLAB Graphical User Interface (GUI) has been used for the purpose of interfacing with FPGA hardware to provide inputs and display outputs.
5. Serial port (RS232) is used for transmitting and receiving data between FPGA board and MATLAB.
6. This Embedded system is applied in Spectral Analysis as an application.

1.5 Project Contributions

The most important contributions of this project are:

1. Integration framework of MATLAB and ALTERA development kit platform.

2. Utilizing Nios II Floating Point Custom Instruction in the design to increase performance and accelerate speed.

3. Created a simple protocol that is used for interaction with and communication between hardware and software via computer serial port.

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