MATHEMATICAL MODELLING AND OPTIMIZATION OF MULTISITE EFFICIENCY TO REDUCE COST OF TEST IN SEMICONDUCTOR FINAL TEST PROCESS USING TAGUCHI METHOD

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A dissertation submitted in partial fulfilment of
the requirements for the award of the degree of
Doctor of Engineering (Engineering Business Management)

Razak Faculty of Technology and Informatics
Universiti Teknologi Malaysia

DECEMBER 2021

DEDICATION

This dissertation is dedicated to the semiconductor test industries

ACKNOWLEDGEMENT

First, I am thankful to God the Almighty for granting me a healthy body and continued presence of mind when confronting and overcoming the numerous challenges in completing my research. I am hope that this research will contribute to the betterment of human society as part of God's will for mankind.

I would like to express my gratitude to Ts. Dr. Rozzeta Dolah and Assoc. Prof. Ts. Dr. Habibah @ Norehan Hj Haron for their full support in facilitating the completion of this dissertation. I sincerely thank them for their invaluable advice and guidance throughout the entire duration of this research. I would like to dedicate the appreciation to Dr. Faizir Bin Ramlie for his advice and guidance throughout my entire engineering doctorate journey. His well-planned coordination has make the study process enjoyable and valuable.

I would like to thank my family for their love and moral support, which gave me the strength to complete this dissertation successfully. I would also like to thank all my friends and those who have helped me directly or indirectly to complete my thesis journey.

Finally, I wish to acknowledge the contributions of members of the test operation department, especially for their useful insights, dedicated assistance and support throughout the tests periods. I would like to especially thank Ts. Dr. Puvanesvaran Gunalan, who is my Industry Supervisor for this research project, for allowing me to use the test equipment for my data collection. Without his help, this research will not be completed successfully.

ABSTRACT

This study proposes improved equations for semiconductor multisite testing process. It contributes to the derivation of the new equations which have better prediction accuracy of multisite efficiency (MSE), testing throughput, and cost of test than the conventional ones to enable accurate conduct of test equipment optimization. This process is achieved by developing new equations which consider ten MSE variables identified in the previous literature and equipment technical specifications where three equations, namely, the MSE equation, testing throughput equation, and cost of test equation, are developed. The developed equations are validated through a Mean Absolute Percentage Error (MAPE). The testing throughput equation is validated to be accurate with 2.58% MAPE compared with 24.02% MAPE for the conventional testing throughput equation. This finding shows that the equations need to include all the related variables for accurate prediction. The study conducts optimized parameter setting for MSE and testing throughput using the Taguchi robust parameter design (L9 orthogonal array), and then analyzes confirmation test for MSE and testing throughput. The MSE and testing throughput are verified to be reproducible with a percentage gain difference of 5.38 (optimum versus worst) and 1.94 (optimum versus current) for MSE and 1.54 (optimum versus worst) and 4.67 (optimum versus current) for testing throughput, which is below 30% of the gage repeatability and reproducibility acceptable level. This finding proves that the control factors significantly affect the MSE and testing throughput. The ideal function graph for MSE and testing throughput shows that the increment of test site significantly affects the MSE and testing throughput, where the higher test site configuration eliminates the effect of the noise factors compared with the lower test site configuration. A cost of test analysis is performed with the Taguchi Loss Function (TLF) to determine which multisite setting produces the cheapest cost of the test relative to MSE. The finding shows that the increment of test site reduces the MSE percentage to achieve the break-even point. If all test site configurations have the same MSE level, then, the X32-site produces the cheapest cost of test. If the MSE of the X32 site drops by 5% compared with the X16 site, then, the X16 site produces a cheaper cost of test. Similarly, if the MSE of X16 sites drops by 5% compared with the octal site, then, the octal site produces a cheaper cost of test. The configuration of X32 sites needs to maintain at least 91% MSE to produce a cheaper cost of the test compared with octal sites. This finding concludes that if the increment of test site cannot sustain the MSE, then, the cost of the test increases. The novelty of this research is the guideline development for cost-effective multisite configuration which is very critical in the semiconductor industry, and it has never been mentioned in any study before. It is a major contribution to the semiconductor test industry, particularly for selecting a cost-effective multisite configuration so that firms can manage their profit and loss accurately rather than simply increasing the test site without understanding its effect on the cost of the test.

ABSTRAK

Kajian ini mencadangkan persamaan yang lebih baik untuk proses ujian pelbagai tapak semikonduktor. Ia menyumbang kepada terbitan persamaan baharu yang mempunyai ketepatan ramalan yang lebih baik bagi kecekapan pelbagai tapak (MSE), *throughput* ujian dan kos ujian berbanding dengan persamaan konvensional supaya pengoptimuman peralatan ujian dapat dilakukan dengan tepat. Ini dapat dicapai dengan membangunkan persamaan baharu yang mempertimbangkan sepuluh pemboleh ubah MSE yang dikenal pasti daripada literatur sebelumnya dan spesifikasi teknikal peralatan di mana tiga persamaan, iaitu MSE, *throughput* ujian, dan kos ujian telah dikembangkan. Persamaan baharu disahkan dengan *mean absolute percentage error* (MAPE). Persamaan *throughput* ujian disahkan tepat dengan 2.58% MAPE berbanding dengan 24.02% MAPE untuk persamaan *throughput* ujian konvensional. Dapatan kajian ini menunjukkan bahawa pemboleh ubah persamaan yang berkaitan perlu merangkumi semua pemboleh ubah untuk ramalan yang tepat. Kajian ini menjalankan tetapan parameter yang dioptimumkan untuk MSE dan *throughput* ujian menggunakan reka bentuk parameter teguh Taguchi (tatasusunan ortogon L9) dan kemudian menganalisis ujian pengesahan untuk MSE serta *throughput* ujian. MSE dan *throughput* ujian disahkan boleh diterbitkan semula dengan perbezaan peratusan perolehan 5.38 (optimum berbanding terburuk) dan 1.94 (optimum berbanding semasa) untuk MSE, manakala 1.54 (optimum berbanding terburuk) dan 4.67 (optimum berbanding semasa) untuk *throughput* ujian, iaitu 30% di bawah ukuran kebolehulangan dan terbitan semula yang boleh diterima. Dapatan kajian ini membuktikan bahawa faktor kawalan mempengaruhi MSE dan *throughput* ujian secara signifikan. Graf fungsi ideal untuk MSE dan *throughput* ujian menunjukkan penambahan bilangan tapak ujian memberi kesan ketara kepada MSE dan *throughput* ujian dengan konfigurasi tapak ujian yang lebih tinggi menghapuskan kesan faktor hingar berbanding dengan konfigurasi tapak ujian rendah. Analisis kos ujian dilakukan dengan *Taguchi Loss Function* (TLF) untuk menentukan tetapan berbilang tapak yang menghasilkan kos ujian termurah berbanding dengan MSE. Dapatan kajian menunjukkan bahawa pertambahan bilangan tapak ujian dapat mengurangkan peratusan MSE untuk mencapai titik pulang modal. Sekiranya semua konfigurasi tapak ujian mempunyai tahap MSE yang sama, maka tapak X32 menghasilkan kos ujian termurah. Sekiranya tapak MSE X32 turun sebanyak 5% berbanding dengan tapak X16, maka tapak X16 menghasilkan kos ujian lebih murah. Begitu juga, jika tapak MSE X16 turun sebanyak 5% berbanding dengan tapak oktal, maka tapak oktal menghasilkan kos ujian lebih murah. Konfigurasi tapak X32 perlu mengekalkan sekurang-kurangnya 91% MSE untuk menghasilkan kos ujian yang lebih murah daripada tapak oktal. Dapatan kajian ini merumuskan jika penambahan tapak ujian tidak dapat mengekalkan MSE, maka kos ujian meningkat. Kebaharuan penyelidikan ini adalah pembangunan garis panduan untuk konfigurasi pelbagai tapak yang kos efektif, yang sangat kritikal dalam industri semikonduktor, dan ia tidak pernah disebut dalam mana-mana kajian sebelum ini. Ini merupakan sumbangan utama kepada industri ujian semikonduktor, terutamanya untuk memilih konfigurasi pelbagai tapak yang kos efektif agar firma dapat mengurus untung dan rugi mereka dengan tepat daripada sekadar menambah tapak ujian tanpa memahami kesannya terhadap kos ujian.

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LIST OF ABBREVIATIONS

ADC	-	Analog-to-Digital
APE	-	Average Percentage Error
ASP	-	Average Selling Price
ATE	-	Automated Test Equipment
BCT	-	Balancing Circular Tree
BIST	-	Built in Self-Test
BOST	-	Built Off Self-test
$C_{ATE,0}$	-	Tester Equipment Cost
$C_{capital}$	-	Capital Equipment Cost
CDA_{cost}	-	Compressed Air Cost
C_{die}	-	Per Unit Cost
COT	-	Cost of Test
CPH_{UTIL}	-	Cost Per Utilization Hour
CPU_{GOOD}	-	Cost Per Good Unit
CPU	-	Central Processing Unit
C_{Reject}	-	Bad Part Cost
$C_{testcell}$	-	Test Equipment Cost
C_{1Ch}	-	Channel Card Cost
C_{1Site}	-	Per Test Site Resource Cost
Dep	-	Equipment Depreciation Cost
DFT	-	Design for Test
DIB_{cost}	-	Engineering Development Cost
DL	-	Direct Labor Cost
DOE	-	Design of Experiment
DIB_{cost}	-	Engineering Development Cost
DRAM	-	Dynamic Random Access Memory
DSP	-	Digital Signal Processor
DUT	-	Device Under Test
EDC	-	Depreciation Cost
EEPROM	-	Electrically Erasable Programmable Read-only Memory Chip

EPROM - Erasable Programmable Read-only Memory Chip

E_{rate} - Electricity Rate Per KWh

FSC - Floor Space Cost

GA - Gate Assembly

GPL - Graphic Processing Logic Chip

GR&R - Gage Repeatability and Reproducibility

IC - Integrated Circuits

ITRS - International Technology Roadmap of Semiconductor

KGD - Known Good Die

KWh - Kilowatt Per Hour

MAD - Mean Absolute Deviation

MAPE - Mean Absolute Percentage Error

MCBJ - Mean Cycle Before Jamming

MCU - Microcontroller Unit

MGC - Management Cost

MHz - Megahertz

MIPS - Million instructions per second

MSD - Mean Square Deviation

MSE - Multisite Efficiency

MTBA - Mean Time Before Assist

MTBF - Mean Time Before Failure

MTTA - Mean Time To Acknowledgement

MTTR - Mean Time To Resolve

$N_{ATE\ CH}$ - Maximum Number of Available ATE Channels

N_{Ch} - Number of Device Pins Cost

N_{DUT} - Number of DUTs

N_{site} - Number of Test Site

OA - Orthogonal Array

OH - Overhead Cost

PaRent - Parallel and Current Method

PCB - Printed circuit boards

PPI - Price Per Index

P_{rating} - Power Rating

PTE	-	Parallel Test Efficiency
RQI	-	Robust Quality Index
SD	-	Squared Deviation
SNR	-	Signal-to-Noise Ratio
SOC	-	System On Chip
SRAM	-	Static Random Access Memory Chip
STDM	-	Space and Time Division Multiplexing
t_1	-	Single-site Test Time
TAM	-	Test Access Mechanisms
TAT	-	Test Application Time
TCH	-	Total Cost
TDE	-	Touchdown Efficiency
TDM	-	Time Division Multiplexing
TEFP	-	Test Equipment Footprint
T_{index}	-	Single-site Indexing Time
TIPE	-	Test Item Priority Estimation
t_{ms}	-	Multisite Test Time
T(N)	-	Total Multisite Test Time
TTB	-	Test Time for Bad Units
TTG	-	Test Time for Good Units
T_{test}	-	Single-site Test Time
t_{total}	-	Test Time Executed
UPH_{GOOD}	-	Good Unit Per Hour
W_{TAM}	-	TAM Width
$(1-Y)^N$	-	Bad Unit Yield
$(1-(1-Y)^N)$		Good Unit Yield

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The Industrial Revolution began in Great Britain in the late 1770s and later spread to North America and other parts of the world (Hall, 1998). The year 1960 ushered in a new era marked by the introduction of electronic devices, such as computers, radios, television sets, mobile phones, and calculators. These devices have changed the way people perform certain tasks. For example, information is no longer transferred through post but via e-mail and the short messaging system. Telecommunication has become a quick and highly effective method of transferring information and data. Engineering and accounting tasks are completed conveniently and accurately by computers and calculators. Global communication has therefore hastened with the advent of the electronic era. Consumers today do not simply purchase electronic devices but also consider the manufacturers, competitors, and specifications (e.g., processor speed, graphical resolution, and functionality) of these devices. Computers that are faster and smarter than those before are currently required. Thus, smartphones are now designed to perform various functions, such as Internet surfing, e-mail retrieval, and global positioning system navigation. The performance of electronic devices has been improved to meet the speed and functionality demands of users. The semiconductor is the main component of electronic devices. Thus, semiconductors require further enhancement and constant updating to meet current market demands.

Semiconductors, either as chips or integrated circuits (ICs) (Beal, 2013), are the main components of electronic telecommunication devices and automotive and household items. Figure 1.1 presents an example of a semiconductor. Semiconductors are built with silicon, a material similar to glass and is made of sand. Numerous transistors that serve as Nano electronic circuits are built on a silicon surface.

Transistors are the smallest and most basic building blocks of most electronic devices developed in the 1950s. Many combinations of electronic circuits have different functions owing to the design specifications of various operations.

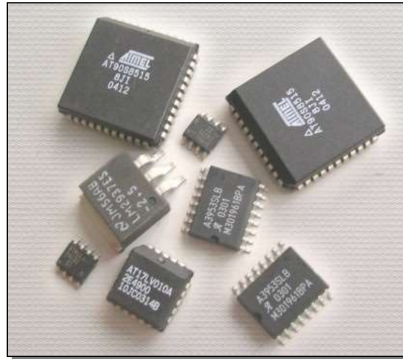

Figure 1.1 Semiconductor integrated circuits/chips

Many types of semiconductors are currently available. They can be differentiated on the bases of device functions or uses. The basic categories of semiconductor chips are as follows (Ross, 2007):

(1) Memory components (data storage)

(2) Logic devices

(3) Combination of memory components and logic devices

(4) Microprocessors

The transistor is the main circuit inside a semiconductor chip. Turley (2009) showed that the development of semiconductors is a major step in the evolutionary ladder: from resistors, capacitors, diodes, and inductors to semiconductors. The continuous demand to improve the performance of current electronic devices prompts the development of semiconductor chips. This trend requires designing and fabricating semiconductor chips with multifaceted functionality, which would consequently increase the number of transistors per chip.

1.2 Problem Background

Moore (1965) predicted that the number of transistors on a chip would double every 18 months to support future technological requirements. Moore’s prediction eventually happened and was established as Moore’s Law, which is still currently used in developing semiconductor chips. This prediction was realized by developing nanotechnology (Kapur, 2001) and system-on-chip (SOC) devices (Zorian, 2000). Nowadays, ICs are built with 10 billion transistors per chip ("Moore's Law―The Number of Transistors on Integrated circuit chips (1976–2016)," 2016). Increasing the number of transistors per chip directly affects the manufacturing cost. However, the average selling price (ASP) of electronic devices does not increase as the performance of these devices improve. The selling price of electronic devices, such as personal computers and cell phones, is continuously reduced as a marketing strategy to maintain competitiveness. The ASP of personal computers has decreased by approximately 34.4% from 2005 to 2015 (from USD 805 to USD 599) (Holst, 2018).

The performance of the microprocessor (a main semiconductor chip in the computer) has improved from 10 MHz in 1970 to 100,000 MHz in 2017, which denotes an improvement of 10,000 times (Chen, 2016). However, a comparison of the ASP trend versus the performance trend reveals that microprocessors with enhanced performance are not selling at their performance price; instead, their price has declined by approximately 36% in 10 years (*PPI industry data for Semiconductors and related device mfg, not seasonally adjusted*, 2019). Therefore, semiconductor chip manufacturers need to reduce their manufacturing costs to ensure profitability.

Semiconductor manufacturing has two main process stages, namely, assembly and testing. On average, the overall assembly cost was annually reduced by 25% to 30% in the last 50 years (Goodall et al., 2002). However, the testing process is having difficulty keeping the Cost of Test low for SOC devices due to the increment in the number of transistors on semiconductor chips. In the year 2016, up to 10 billion transistors can be embedded on a single chip ("Moore's Law―The Number of Transistors on Integrated circuit chips (1976–2016)," 2016). The device complexity trend published in the "ITRS Test Team 2014 Update" (2014) predicted that test time

will increase twice every four years, and this increment will slow down the overall testing and increase the Cost of Test.

The increment of Cost of Test will negatively affect the overall manufacturing costs (Moore, 1965; Waldrop, 2016). Predictions also show that assembly costs and Cost of Test are equal in the year 2019 (*International Technology Roadmap for Semiconductors—Test and Test Equipment*, 2015). Therefore, the Cost of Test needs to be reduced while ASP declines to maintain the profit margin. The semiconductor test industry has developed multisite test equipment to overcome the Cost of Test problems (Dworak et al., 2015).

Multisite testing means that a test equipment tests multiple chips in parallel. For example, Figure 1.2 shows five chips being tested in parallel.

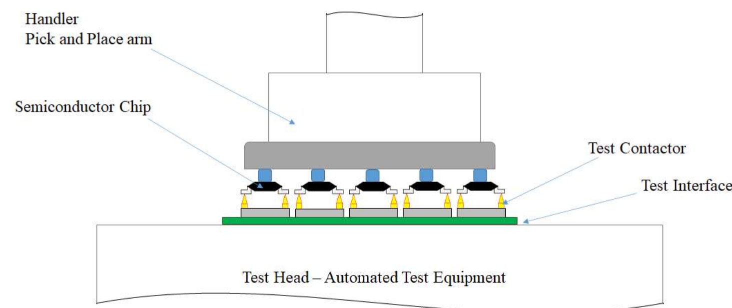

Figure 1.2 Multiple chips are test in parallel

Testing semiconductors requires automated testing equipment (ATE) or a tester to check the electrical and electronic functionality of semiconductor chips. However, ATE cannot perform the test by itself and requires integration with other supporting modules (shown in Figure 1.3) as follows:

(1) Test interface. This module is an electronic interface that connects a semiconductor chip to an ATE. It allows the ATE to measure the signal and functionality of a particular semiconductor chip by ensuring that the chip is performing in accordance with the design specifications.

(2) Test socket or contactor. A load board can function only if a test socket or contactor that connects a chip and the load board is installed.

(3) Test handler. This fully automated equipment is simply a robotic module that handles and transfers chips to the load board and test socket for testing. Afterwards, the test handler sorts the chips on the basis of quality (favorable or unfavorable).

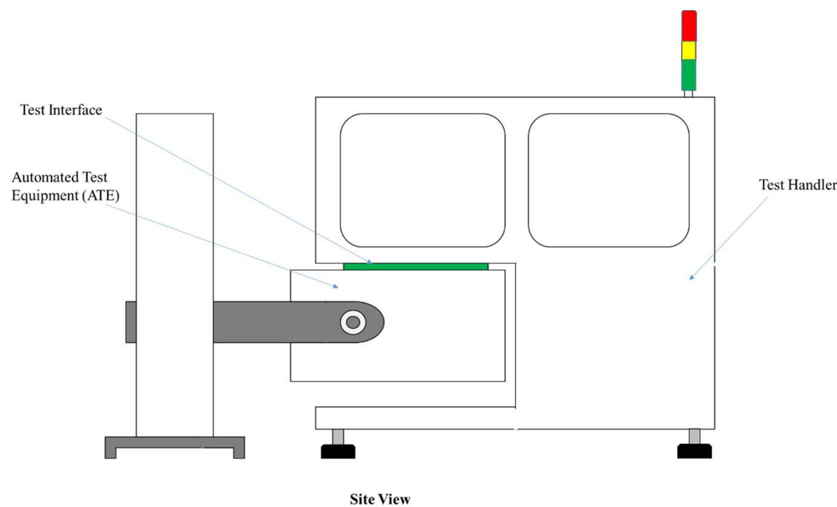

Figure 1.3 Pick and place test equipment

Test equipment contributes directly to the Cost of Test. Cost of Test consists of three main test operation expenses. The first one is the cost of probers and handlers that accounts for approximately 15%. The second one is the Cost of Test consumables, which include the test interface (e.g., the load board and test contactor), and it accounts for approximately 42%. The third one is the cost for ATE that accounts for approximately 43% (*International Technology Roadmap for Semiconductors—Test and Test Equipment*, 2015). Figure 1.4 presents an overview of the fundamental flow of the pick-and-place testing process as explained below.

(a) The input pick arm collects the chips from the input tray and transfers them to the input shuttle.

(b) The test arm takes the chips from the input shuttle and punches them into the test contactor to begin the testing.

(c) The tested chips are replaced with new ones and are then transferred to the output shuttle.

(d) The chips are sorted by the output sorting pick arm into the good tray for the tested good chips and the rejected tray for the tested bad chips.

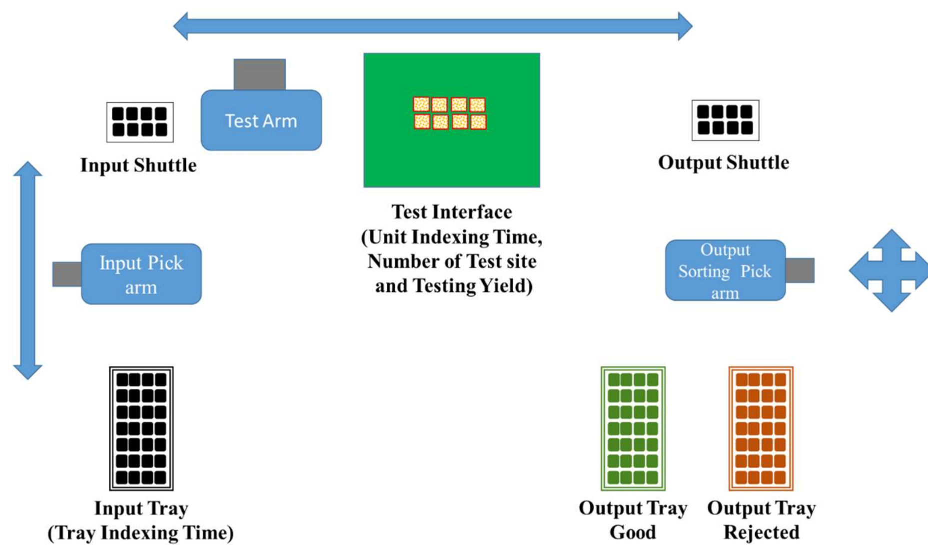

Figure 1.4 Flowchart of the testing process: pick and place handler

The overall testing process highlights the importance of understanding the Cost of Test determined by the amount of time spent on testing a semiconductor chip. The Cost of Test is directly affected by the testing throughput or speed at which a test cell completes the testing of a semiconductor chip. The multisite testing approach is used to test multiple chips in parallel to improve the testing throughput and reduce costs. Its effectiveness depends on multisite efficiency (MSE).

MSE refers to the efficiency of multisite test equipment. Many factors affect MSE, namely, (a) single-site and multisite test times; (b) single-site and multisite indexing times; (c) number of test sites; (d) tray indexing time; (e) testing yield; (f) equipment utilization; and (g) jam rate. MSE is the deciding factor in improving the

testing throughput which will reduce the Cost of Test (Kramer, 2018; Lee et al., 2017; Smith, 2006). However, adding numerous test sites does not guarantee that the testing throughput will be improved, and the investment to increase test sites must be justifiable; according to average cost theory, the per unit cost is equal to the total cost divided by the total output (Waldman & Jensen, 2016). If the testing throughput improvement is not greater than the multisite investment, then, the per unit cost can be higher than that indicated in the test site configuration (Kim et al., 2014).

1.3 Problem Statement

The number of chips per transistor increases by more than double every two years to fulfil the market requirements for semiconductor speed and functionality (Moore, 1965; Waldrop, 2016). This trend has caused the test time to increase twice in every four years ("ITRS Test Team 2014 Update," 2014). An increased test time affects the Cost of Test. Slow testing makes the test much more expensive due to the low testing throughput. If the Cost of Test problem is not addressed effectively, then, the overall profit margin of the semiconductor chip itself will be affected because the ASP of electronic devices, such as desktop computers are continually decrease (Holst, 2019).

Over the past 5 years, multisite testing has been implemented to overcome the Cost of Test problem. The *International Technology Roadmap for Semiconductors—Test and Test Equipment* (2015) has shown that the increment in test sites with unsustainable MSE will not guarantee testing throughout improvement. The MSE equation developed by the *International Technology Roadmap for Semiconductors—Test and Test Equipment* (2015) is only based on the test time and number of test sites. However, from the literature review, eight other variables have a direct impact on MSE which will affect the accuracy of the investment on multisite testing.

Among the literatures which highlighted the other eight variables included the research conducted by Lee et al. (2014), who concluded that testing throughput is

affected by test time and test site configuration. From another study, a high test time corresponds to low testing throughput (Dworak et al., 2015). The study on the octal-site configuration showed that when the test time is reduced by 10.09%, then, the testing throughput is improved by 9.26%. However, the 12-site configurations produce more throughput than quad- and six-site configurations. The same finding was obtained by a study using the "Strip Test Handler" (2013), where the X32-site configuration produced a higher throughput than the X16-site configuration, but the throughput depreciated when the test time was increased.

Meanwhile, Velamati and Daasch (2009) concluded that a high testing yield corresponds to improved MSE regardless of the test site configuration. In another study, MSE affected the Cost of Test; the highest MSE corresponded to the lowest Cost of Test depending on the test site configuration. Further addition of test sites reduced the Cost of Test. When MSE was below 90%, the Cost of Test increased when more test sites were added. For example, with 75% MSE, the Cost of Test for the X32-site configuration was 0.7% compared with the X16-site configuration, which produced 0.5% (lower by 0.2%) (Smith, 2006).

In addition, Smith (2006) concluded that production lot sites affect the Cost of Test. Small production lots have higher Cost of Tests than large ones because the equipment is underutilized. Meanwhile, large production lots have lower Cost of Tests than small ones because of the high equipment utilization rate. However, the Cost of Test increases relative to the test site increment regardless of lot size. The same finding was obtained by Kramer (2018), who found that equipment utilization affects the Cost of Test.

Furthermore, Kim et al. (2014) concluded that if MSE is not sufficiently high to improve the test throughput, then, the Cost of Test will increase relative to the test site increment because an increase in test sites requires more investment. Lee et al. (2007) concluded that the tray matrix influences the testing throughput. More chips on the tray correspond to a high testing throughput. The testing throughputs for all tray matrixes 3X8, 4X9, and 5X12 are saturated when the test time reaches 4 sec.

Jam rate was also discussed by Smith (2006) as a testing throughput variable. The testing throughput is affected by MSE, and all the variables that affect the testing throughput must be included as part of the MSE study; otherwise, it will not reflect the actual MSE situation and will affect the Cost of Test.

As indicated in the literature review, the ten variables include all the Pick and Place Test Equipment variables, namely, single-site test time, multisite test time, single-site indexing time, multisite indexing time, number of test sites, tray indexing time, test yield, equipment utilization, jam rate, and MTTR. However, no research comprehensively analyzed how one variable relates to another and what the comprehensive effects are on MSE and testing throughput. This research aims to fill these gaps by comprehensively developing an MSE and testing throughput equations that include all the relevant variables.

With the newly developed MSE equation, the multisite configuration optimization produces the lowest Cost of Test; hence, a high profit margin can be achieved. Good MSE produces the highest testing throughput, but the per unit cost or Cost of Test is not the lowest if the multisite investment is greater than the throughout improvement (Kim et al., 2014). Therefore, MSE needs to be optimized from the perspective of Cost of Test instead of considering only the testing throughput improvement. The proposed MSE equation will be incorporated into average cost theory to obtain per unit cost for MSE. This approach will allow semiconductor testing manufacturers to determine the optimized MSE configuration that can produce the lowest Cost of Test and ultimately understand how MSE affects the Cost of Test. Taguchi robust parameter design is used for MSE optimization because of the signal-to-noise ratio (SNR), which was developed to measure product quality and the robustness of process performance in response to noise, that is, a high ratio corresponds to great robustness, thereby producing the optimum output signal (Taguchi & Chowdhury, 1999). The goal of a robust parameter design is to determine factor settings that will minimize the variability of the response on some ideal target value (or target function in the case of a dynamic response experiment). Taguchi methods do this task through a two-step optimization process ("Minitab,"). The first step concentrates on minimizing variability base on SNR, and the second focuses on

hitting the target by adjusting the level of one or more factors that substantially affect the mean (or slope) to put the response on target ("Minitab,").

In addition, the Taguchi orthogonal array (OA) is a better DOE approach, especially for investigating the effect of multiple factors or parameters; it can reduce the number of experiment trial runs significantly compared with the traditional DOE method. Finally, the Taguchi loss function analysis, which measures the deviation from the target as the loss, is a more accurate method of Cost of Test (COT) study from the perspective of MSE corresponding to better profit margin. This approach is different from the traditional loss function, which determines that loss occurs when some COTs are beyond the control limit. The proposed MSE equation is expected to help enhance the body of knowledge on MSE and solve the current and future industry Cost of Test issues, which is currently the main problem faced by firms.

1.4 Research Aims

This research aims to develop a new MSE and testing throughput equations by considering all related variables to achieve optimization of MSE to increase testing throughput, hence possibly reducing cost of test.

1.4.1 Research Objectives

This research attempts to achieve the following objectives:

(1) To determine the variables which have a significant effect on MSE and testing throughput;

(2) To develop a new MSE and testing throughput equation for semiconductor testing;

(3) To validate the MSE and testing throughput equations through the optimization of MSE and testing throughput with the robust parameter setting;

(4) To investigate how MSE affects the Cost of Test reduction.

1.5 Research Questions

The research questions are as follows:

(1a) What are the variables which have a significant effect on MSE and testing throughput?

(2a) How do the 10 variables affect MSE and testing throughput?

(3a) What is the optimized parameter setting that produces the highest MSE?

(3b) Which parameter has the most sensitive effect on MSE?

(3c) What is the optimized parameter setting that produces the highest testing throughput?

(3d) Which parameter has the most sensitive effect on testing throughput?

(4a) Does MSE exert a significant effect on Cost of Test?

(4b) What is the optimized multisite configuration for producing the lowest Cost of Test?

1.6 Scope of Research

On the basis of the goals of this study, a Taguchi robust parameter design is conducted on MSE optimization for several reasons. First, previous studies and predictions did not consider all the 10 MSE variables. A new MSE equation needs to be developed for comprehensive MSE research (objective 1 and 2). Second, testing throughput is affected by MSE, because an increment in the number of test sites affects the testing throughput loss caused by inefficiency (objective 3). Third, the effects of

MSE and testing throughout on Cost of Test are not fully understood by semiconductor test manufacturers; they simply add test sites, which does not reflect the actual Cost of Test reduction because the average cost is equal to the total cost divided by total output (objective 4) (Waldman & Jensen, 2016). Lastly, no optimization research has been conducted by using the Taguchi robust parameter design, where the main function of SNR is to be minimally sensitive to factor variability at the lowest cost (Taguchi & Chowdhury, 1999). The SNR, which is the measurement method for the Taguchi robust parameter design, is the index of robustness of a product or process in response to noise; a high ratio corresponds to high robustness of a product or process, thereby enabling the optimization to be conducted more effectively compared with the conventional "whack-a-mole" engineering approach (Taguchi & Chowdhury, 1999). particularly for the MSE study because robustness is the opposite of inefficiency.

Currently, Malaysian semiconductor test manufacturers are heavily involved in multisite testing. This approach is selected as an experimental subject because Malaysian manufacturers have the world's most advanced multisite technologies, including the wafer prober, the strip test handler, and the pick-and-place handler, which can provide crucial data required for MSE optimization research. This study focuses only on the pick-and-place handler because this technology is commonly used in the industry. Other test handler types exist, such as gravity feed, strip test, and wafer prober, which are not part of this research and can be further investigated in future research. Data are gathered from a semiconductor test manufacturer in Penang to obtain sufficient data for all 10 MSE variables. A comparison of the different tray matrices is performed for three different test site configurations. The details of this research scope are discussed further in Chapter 3.

1.7 Significance of Research

The MSE predicted by the *International Technology Roadmap for Semiconductors - Test and Test Equipment* (2015) is based on test time and number of test site (Equation 2.1). However, other variables exert a direct impact on MSE; these variables are (1) single-site test time, (2) multisite test time, (3) single-site indexing

time, (4) multisite indexing time, (5) number of test sites, (6) wafer/strip indexing time, (7) tray indexing time, (8) testing yield, (9) equipment utilization, (10) jam rate, and (11) MTTR. Previous MSE studies were conducted without considering all related variables; thus, they are inaccurate and do not reflect the actual testing improvement situation and Cost of Test. In addition, many multisite studies have been conducted, but none of them used all 10 MSE variables. For example, the root device under test (DUT) algorithm implemented by Kim et al. (2014) focused on testing time, number of test sites, and indexing time. The BOST interface method applied by Seo et al. (2017) focused on test time and number of test sites. The test program optimization method implemented by Lee et al. (2017) concentrated on the single-site and multisite test time and number of test sites. The multisite test equipment used by Khoo (2015) and Evans (1999) focused on single-site and multisite test time, single-site and multisite indexing time, and testing yield. The parallel and concurrent method (PaRent) applied by Dworak et al. (2015) focused on test time. The real-time yield monitoring method used by Khasawneh et al. (2018) focused on test time. Lastly, the testing scheduling method utilized by Vartziotis et al. (2014) focused on test time. Therefore, the current research is a study of multisite test equipment from the perspective of MSE to improve the testing throughput and reduce cost by using all related variables, thus ensuring that MSE optimization can be achieved. Without a comprehensive MSE study using all the variables, the results of previous studies do not reflect the actual situation of MSE. Hence, the optimization of the multisite configuration is inaccurate, and the worthiness of the multisite investment becomes questionable and misleading. This issue has been facing the industry for past 10 years and requires immediate attention to address the question of whether adding more test sites to improve the testing throughput will reduce the COT.

1.8 Operation Definition of MSE Variables

(a) Single-site and Multisite Test Times

Testing time is the time an ATE spends on measuring all of the semiconductor chip parameters to ensure that the performance is in accordance with the design

specification (Kim et al., 2014). If the conventional serial testing sequence is used in the multisite environment, then even the indexing time is reduced; however, MSE is affected by prolonged testing time because multiple chips are tested in parallel (*International Technology Roadmap for Semiconductors - Test and Test Equipment*, 2015; Khoo, 2015). The measurement of MSE for testing has been examined in relation to the increment in multisite test time versus single test time. The smaller the increment in multisite test time is, the better MSE is. This is because when the test time is short then the testing throughput will improve, this lead to the MSE improvement as well.

(b) Single-site and Multisite Indexing Times

Indexing time is the chip transfer or replacement time from tested chips to new chips (Evans, 1999; Khoo, 2015; Seo et al., 2017; Smith, 2006). An example of indexing time is as discussed as follow; (a) the first tested chips are indexed forward and replaced by the second chips until they are completely tested; (c) the second chips are then indexed forward to be replaced by the third chips and so on. For multisite testing, multiple chips are tested in parallel. For example, eight chips are in the first group. When all the chips are completely tested, they are indexed forward and replaced by another eight chips that are in the second group and so on. When multiple chips are tested in parallel, the indexing time is reduced depending on the number of test sites. For MSE calculation, the multisite indexing time is compared with the single-site indexing time to measure the percentage of improvement, which ultimately reflects the testing throughput (Evans, 1999; Khoo, 2015; Seo et al., 2017; Smith, 2006).

(c) Number of Test Sites

Number of test sites is the test site configuration to handle the number of chips for parallel testing. The test site configuration involves the load board or probe card layout and the number of test contactors or probe pins to be used in multisite testing (Kim et al., 2014; Kramer, 2018). It also includes ATE resources, such as channel cards, and additional ATE resources need to have more chips tested in parallel (Kim et al., 2014; Lee et al., 2017). In this case, an additional cost for the tester interface,

such as the load board, probe card, test contactor and probe, and the ATE hardware is required to enable multisite testing; however, if the testing throughput improvement is not greater than the additional cost, then the per unit cost increases instead of decreasing (Evans, 1999; Khoo, 2015; Kim et al., 2014; Valdez, 2018). Therefore, MSE is important in justifying the multisite configuration investment because an increment in the number of test sites with a low MSE does not guarantee testing throughput improvement (*International Technology Roadmap for Semiconductors - Test and Test Equipment*, 2015; Smith, 2006).

(d) Tray Indexing Time

Tray indexing time is the amount of time spent on replacing an empty tray where the chips have been fully picked up with a new tray with fully loaded chips until the chips are fully picked up from the tray; in other words, it is the time spent between the last chip of the first tray until the last chip of the second tray and so on (Lee et al., 2007). The tray indexing time is affected by two variables, namely, the tray matrix and the number of test sites (Lee et al., 2007). The tray matrix pertains to how many chips are arranged and placed on the tray. Large chips mean fewer chips on the tray, and small chips mean more chips on the tray. When numerous chips are placed on the tray, the tray exchange sequence is reduced but still depends on the number of chips tested in parallel. The tray sequence increases when numerous chips are tested in parallel.

(e) Testing Yield

For advance-complexity chips, billions of transistors are built on them via nanotechnology, and the transistor size is reduced by 96% within 12 years (Flamm, 2018). When the transistor count on a chip increases by 100,000,000%, the line width is reduced by 100,000% (Byrne et al., 2018). This means that the chips' contact point, such as lead, pad or solder ball, needs to have a very fine size, which requires a highly accurate test handler or prober to align the contact positioning accurately. One of the critical challenges in the multisite testing environment is contact accuracy; inaccurate contact causes the electrical resistance to increase, which then affects the testing measurement accuracy (Lehner, Kuhr, Wahl, & Brück, 2014). Another factor that can

affect the electrical resistance is the length of the wire trace from the tester to the contactor. This influence is due to multiple chips that are tested in parallel. Therefore, the location of every chip is different, and the wire trace lengths to every test site also vary. This problem was discussed in the paper of Lehner et al. (2014), who concluded that test sites have different electrical resistances, and in the paper of Yang et al. (2015), who reported that the probe marks on BGA balls are offset by positioning inaccuracy. The electrical resistance affecting the accuracy of the testing measurement ultimately affects the testing yield. The electrical resistance is affected by the site-to-site variation caused by the different trace lengths, tester resource arrangements and handler alignment (Farayola et al., 2020). In this case, testing yield is one of the important variables for MSE. This measurement focuses on increasing the number of test sites to provide the same testing yield to guarantee that gage repeatability and reproducibility (GR&R) is achievable. The lower GR&R is, the poorer MSE is.

(f) Equipment Utilization

Equipment utilization is the percentage of an equipment that is occupied with productivity activities (Peng, 2016). Kramer (2018) concluded that equipment utilization has a direct impact on the Cost of Test due to the fact that if a test equipment is under-utilized, then the per unit cost will increase relative to the fixed cost. If the test equipment is 100% utilized, then the subsequent production lot will require additional test equipment, which will affect the overall production cost. It will increase and slowly decrease as the second test equipment utilization increases until the third test equipment is required for additional production loading. Therefore, equipment utilization affects MSE, especially the additional test equipment that are required when the production loading is increased (Kramer, 2018).

(g) Jam Rate

Jam rate has been identified as one of the important variables in MSE because the test equipment stability for handling multiple chips to be tested in parallel is important in ensuring that the equipment is performing well even though the test sites are increased (Fenton, 2014). The jam rate can be measured in many ways. Most test

equipment developers use the mean cycle before jamming (MCBJ), which pertains to the number of cycles a test equipment is able to repeat before it jams or stoppages occur ("High Performance Strip Handler," 2018; "Strip Test Handler ", 2013). Another way to measure the jam rate which is mean time between assists (MTBA), which is the performance indicator for automated equipment to measure the total running or productive time between assists. Assists pertain to the situation when the automated equipment stops due to certain jamming and human assistance is required to recover the automated operation (Gupta, 1987; Mathia, 2010). The fewer the assists are, the higher the performance efficiency of an equipment is.

(h) Mean Time to Acknowledgement

Mean time to acknowledgement (MTTA) is another variable identified by Kramer (2018) and Smith (2006) that exerts a direct impact on testing throughput. MTTA is the time required to recover from jamming or stoppages so that the test equipment can resume testing (Smith, 2006). The shorter MTTA is, the better MSE is. If MTTA increases in the higher test site configuration, then MSE will decrease as more chips are tested in parallel. In other words, if the higher parallelism configuration requires much time to recover from stoppages, then MSE will be low, which will ultimately reduce the testing throughput.

(i) Mean Time to Resolve

Mean time to resolve (MTTR) is the measurement of how much time is required to resolve an incident. MTTR measurement begins from the moment an incident occurs to the moment when it is resolved and normal operation or performance resumes (Knapp, 2012). For testing equipment, MTTR measures how much time is needed to resolve test equipment jamming from the moment the equipment stops until it recovers and resumes its normal operation. MTTR measurement can be used to track the total amount of down time in a test equipment utilization hour so that the actual utilization time can be obtained; it contributes to MSE and testing throughput ultimately (Kramer, 2018).

1.9 Organization of the Dissertation

This dissertation is divided into six chapters. Chapter 1 provides an overview of the semiconductor industry, manufacturing cost and testing cost, multisite efficiency, problem statement, research questions, research objectives, research scope, and research significance. Chapter 2 provides a literature review, including cost of testing, the cost model, and variables contributing to multisite efficiency; testing throughput cost of testing; and the Taguchi robust parameter design. Chapter 3 presents the research methodology. Chapter 4 discusses the analysis results of the research objective. Chapter 5 discusses the research finding, and the final chapter concludes the dissertation and recommends future work to be adopted.

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LIST OF PUBLICATIONS

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1. Khoo, V. C., Dolah, R., Haron, H. N., Ramlie, F., & Hassan, M. Z. (2020). Comprehensive Multisite Efficiency Equation for Semiconductor Test Equipment. Journal of Engineering Science and Technology, 15(6), 3971-3982. **(Indexed by SCOPUS and Web of Science Q3)**

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2. Khoo, V. C., Dolah, R., & Haron, H. N. (2021). Optimization of Semiconductor Final Test Multisite Efficiency and MSE Equation validation using Taguchi Method. In 5th International Conference on Robust Quality Engineering 2021. **(Indexed by J-STAGE)**

Non-Indexed Conference Proceedings

3. Khoo, V. C., Dolah, R., & Haron, H. N. (2021). Validation of the Semiconductor Cost of a Test Equation with a Taguchi Robust Parameter Design. In 9th & 10th International Conference on Engineering Business Management 2021.