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Design and Analysis of Electrical Characteristics of 14nm SOI-based Trigate Gaussian Channel Junctionless FinFET

Design and Analysis of Electrical Characteristics of 14nm SOI-based Trigate Gaussian Channel Junctionless FinFET

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Abstract. Planar MOSFETs are reaching their physical limits. To overcome the limitations and improve channel gate control, FinFET technology, which uses many gate devices, is a superior choice while lowering the size of planar MOSFETs even further. In this paper, 14nm Silicon-On-Insulator-based Trigate Gaussian Channel Junctionless FinFET is presented. The gate length of 14nm is considered along with an Equivalent Oxide Thickness of 1nm, 5nm as fin width, and the work function of the gate metal is 4.75eV. The device architecture has a non-uniform doping profile (Gaussian distribution) across the fin's thickness. It is devised to address the effects of Random Dopant Fluctuations such as channel mobility degradation in Junctionless FinFET based devices. The impact of fin height (F_h), gate dielectric and spacer dielectric on the Drain Induced Barrier Lowering, Subthreshold Swing, drain current of GC-JLFinFET is analyzed. The results show that the I_{on}=101.5μA/μm and I_{on}/I_{off} is $3.2x10^7$ are obtained for the proposed device structure compared to the existing structure, which has I_{on}/I_{off} of $1.1x10^7$. Furthermore, the proposed design shows better efficiency in short channel characteristics, namely DIBL=25.3 mV/V, Subthreshold Swing=63.88 mV/dec and Transconductance =$3.621x10^5$ S/μm. Thus the Gaussian Channel-based FinFET architecture can provide optimum results for Junctionless-based FinFET devices.

1. Introduction

The industry of conventional Metal Oxide Field Effect Transistors (MOSFET) focuses on creating the transistors with metallurgical junctions during fabrication. As propounded by the International Technology Roadmap for Semiconductors (ITRS) road map, the primary area of focus will take on the continued reduction in the size of CMOS (Complementary-Metal-Oxide-Semiconductor) and system integration [1]. As the size of MOSFET gets reduced, the Short Channel Effects (SCEs) tends to increase, affecting the device's performance. Several solutions such as Silicon On Nothing (SON) technology, Silicon On Insulator (SOI) technology and Multi Gates FET architectures have been propounded to address the issues mentioned above [2-3]. However, when the transistors enter the nanoscale regime, the fabrication becomes difficult due to the presence of junctions as it increases the complex thermal budget of the device. An interesting concept of Junctionless Transistors has been introduced to solve the issues mentioned above, which is free from any p-n junctions and a simplified fabrication process [4-6]. The Junctionless Transistors operate in bulk conduction, unlike their counterparts, such as the accumulation and inversion mode FETs that function in surface conduction. When the Junctionless Transistors works in bulk conduction mode, it results in augmented performance

in Subthreshold and trivial surface scattering [7]. The multi-gate Junctionless Transistors structures such as Double Gate FETs [8] and Tri-Gate FETs have been developed in which the Tri-Gate architecture has better controllability of gate, reduced DIBL, Subthreshold Swing and increased ON current [9]. The primary requirement of Junctionless architecture is high uniform doping concentration from source to drain of (10^{19}-10^{20} cm^{-3}) to sustain high current during ON state and total depletion of the channel during OFF state conditions. The concept of high-k spacers has been presented to improve the device's scalability and operation [10-14].

It is demonstrated that the high-k spacer reduces the fringing field while improving the OFF-state current without affecting the ON current. Finally, Bae MS et al. studied the process variability in the Junctionless FinFETs due to Random Dopant Fluctuations, gate work function and oxide thickness variation [15].

The JL-FinFET has many inherent advantages, but the critical constraint during the fabrication is achieving high uniform doping in the device layer. This complexity is increased even more for non-planar architectures such as FinFET as the fin's doping has to be accomplished in a three-dimensional pattern, resulting in non-uniform doping around the fin region [16]. The generic analytical doping is a Gaussian doping profile from which other doping distributions can be derived by tuning specific parameters of Gaussian distribution as required [17]. The literature review reveals various studies have been done in the performance and device operation of Junctionless concept based FinFETs with heavily doped structures. Recently, Mondal et al. [18] proposed a Gaussian channel doping profile in Junctionless Transistors. We present a Gaussian Channel-based Junctionless FinFET structure simulation in a 14nm technology. The device structure is simulated and analyzed using the TCAD simulation tool, and the IV characteristic is compared with the existing uniformly doped Junctionless FinFET structure. This paper focuses on the comprehensive study on Gaussian doping Junctionless FinFETs and provide a solution to improve the leakage current of the device.

The remnant of this manuscript is organized as follows: Section 2 reports the proposed device structure and simulation, Section 3 describes the performance analysis of the proposed structure. Subsequently, Section 4 summarizes the findings and concludes.

2. Device Structure and Simulation

The 3D schematic view of the proposed n-type Junctionless FinFET architecture used for simulation is shown in Figure 1. The channel length is chosen as gate length of 14nm as per the 7nm technology in ITRS [1]. In addition, all the design parameters and electrical characteristics of the structure were calibrated as per the guidelines of ITRS.

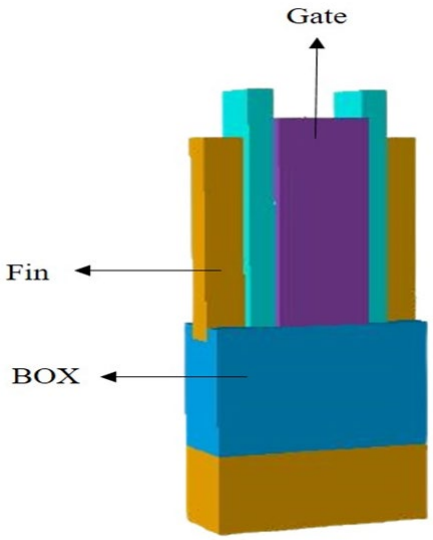


Figure 1. 3D schematic view of the 14nm SOI-based n-type Junctionless FinFET.

Table 1 listed out the device dimensions of the simulated 14nm SOI Gaussian Channel Junctionless FinFET. The source and the drain (S/D region) have the same n-type doping concentration of 4 x 10^{19} cm^{-3} for all the cases. In uniform doping distribution, the channel has the same doping concentration of 4 x 10^{19} $cm^{-3,}$ similar to the S/D regions. However, the S/D regions are highly n-doped, and the channel has non-uniform n-type doping of 4 x 10^{19} cm^{-3} across the thickness of the fin. The non-uniform doping distribution can be defined using a 1D Gaussian distribution function as given in the following equation [19] :

$$N_D(Y) = PEAK.exp\left[-\left(\frac{Y}{Y.CHAR}\right)\right]^2 \quad (1)$$

Where PEAK is the peak doping concentration, Y.CHAR is the Gaussian doping's standard deviation or straggle length. The Gaussian doping profile in the JL-FinFET structure is analyzed with the peak of 4 x 10^{19} cm^{-3} placed at the sidewalls of the fin and gets reduced gradually towards the centre of the fin with the standard deviation of 1 nm/dec. The gate work function of all the configurations of FinFET was adjusted to obtain a 400mV Threshold Voltage for a meaningful comparison. The detailed device parameters list is provided in Table 1 and compared with other work [20] and the gate length is the same which is 14nm according to the reference paper [20].

Table 1. Simulation Device Parameters of the 14nm SOI Gaussian Channel Junctionless FinFET

Device parameters	**This work**	**Other work, Kaundal S [20]**
Gate Length, L_g	14nm	14nm
Fin Width, F_w	5nm	8nm
Fin Height, F_h	42nm	N/A
EOT	1nm	1nm
S/D Doping, N_{sd}	4.0×10^{19} cm^{-3}	2.5×10^{19} cm^{-3}
V_{DS}	0.70V	0.70V
Spacer width	10nm	(2-22) nm

The simulation of the Junctionless FinFETs was performed in the Silvaco TCAD simulation tool. The Atlas simulator of Silvaco was used to obtain the electrical characteristics. The Bohr Quantum Potential model was included for quantization effects in the device to get higher accuracy in the results. In the quantum transport equation, the density gradient model is incorporated. The Band Gap Narrowing (BGN) model is used for highly doped JLFinFETs to precisely model the bipolar current gain. Band-To-Band-Tunneling (BTBT) model and Shockley Read Hall (SRH), along with Auger models, respectively, were included to account for band-to-band tunnelling and recombination effects. Finally, the Lombardi CVT model is introduced in the simulation for carrier mobility.

3. Results and Discussion

For fair validation, the device is carefully calibrated using the experimental results for 14nm Conventional Inversion Mode FinFET structure using the 3D TCAD simulator [21]. The precise calibration can be achieved by implementing the exact device parameters and dimensions and the doping in TCAD simulation to match current-voltage (I-V curves). After which, the mobility models can be varied to achieve the electrical characteristics of the proposed work. The simulated IV characteristics of both n and p-type FinFET exhibit good compliance with the experimental results of work in [21] as depicted in Figure 2 by validating the results of the device simulations. Figure 3 shows the net doping concentration of 14nm Inversion-Mode FinFET, Uniformly Doped Junctionless FinFET and Gaussian Channel Junctionless FinFET.

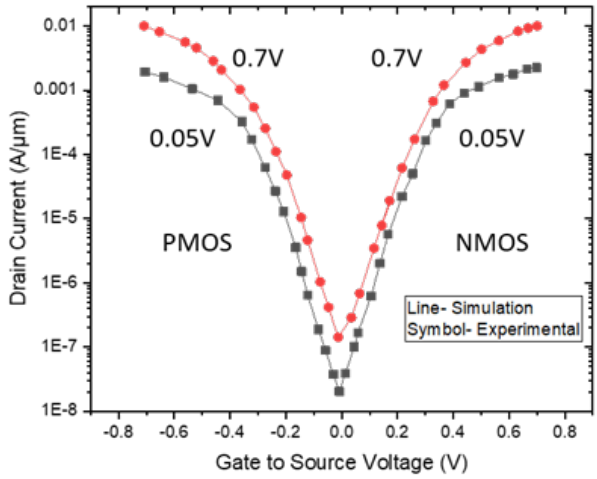


Figure 2. Calibration of the simulation with the experimental data for 14nm IM-FinFET structure [21].

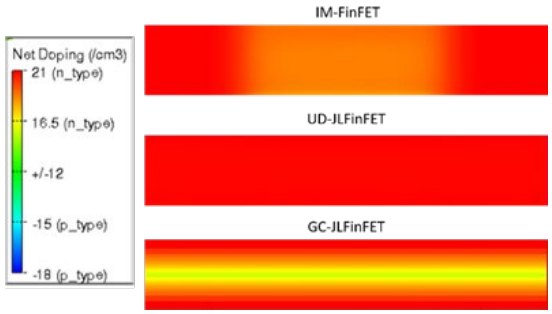


Figure 3. Cross-Sectional view of the channel in Inversion mode FinFET, Uniformly Doped Junctionless FinFET and Gaussian Channel Junctionless FinFET mode at V_{gs}=1V, V_{ds}=0.7V.

In the IM-FinFET, p-n junctions are present; hence, the doping profile is Gaussian with Junction. In Uniformly doped Junctionless FinFET, the doping profile is the same and uniform through the device structure. In contrast, in Gaussian Channel Junctionless FinFET, the doping concentration is a peak at the sidewalls of the fin. It gradually declines towards the centre of the fin. Therefore the declined doping concentration at the centre of the channel makes the electron mobility increase during the ON state (V_{gs}=0.4V, V_{ds}=0.7V). At the same time, the depletion of electrons at the sidewalls of the fin is also reduced simultaneously when the device is in the OFF state (V_{gs}=0V, V_{ds}=0.7V). Moreover, as the doping is spread across the channel, there is a subsequent reduction of electron crowding. The electron crowding is one of the major problems in the FET as it increases the impurity scattering because of Random Dopant Fluctuation in the device [22]. Thus 14nm SOI-based GC-JLFinFET has reduced scattering of impurity caused by the RDF. The above points show that the proposed device has a better electrical and electrostatic performance when compared to the conventional and existing FinFET structures.

3.1. Analysis of electrical characteristics

Figure 4 illustrates the effect of varying the fin height for GC-JLFinFET at L_g=14nm, F_w=5nm and V_{ds}=0.65V. The ON current increases as the fin height is increased due to the larger channel volume. The proposed GC-JLFinFET has a higher I_{on} when the height of the channel is 42nm. As the fin height is varied to 12, 22, and 42nm, enhanced I_{on} is achieved with 26.3% improvement at F_h=42nm. Figure 5(a-b) shows the effect of fin height variation over the DIBL and SS.

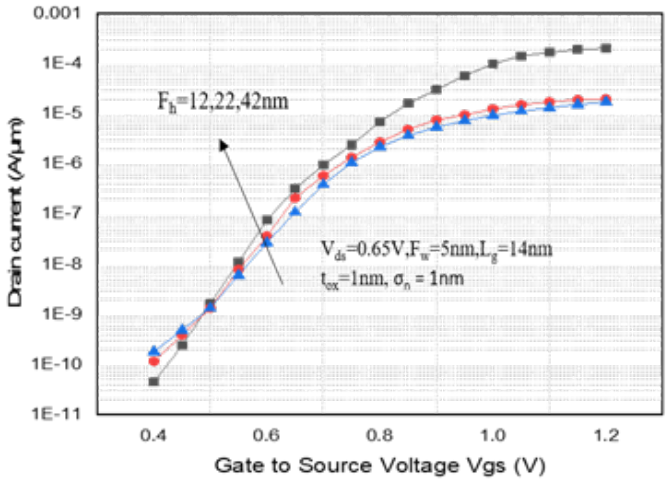
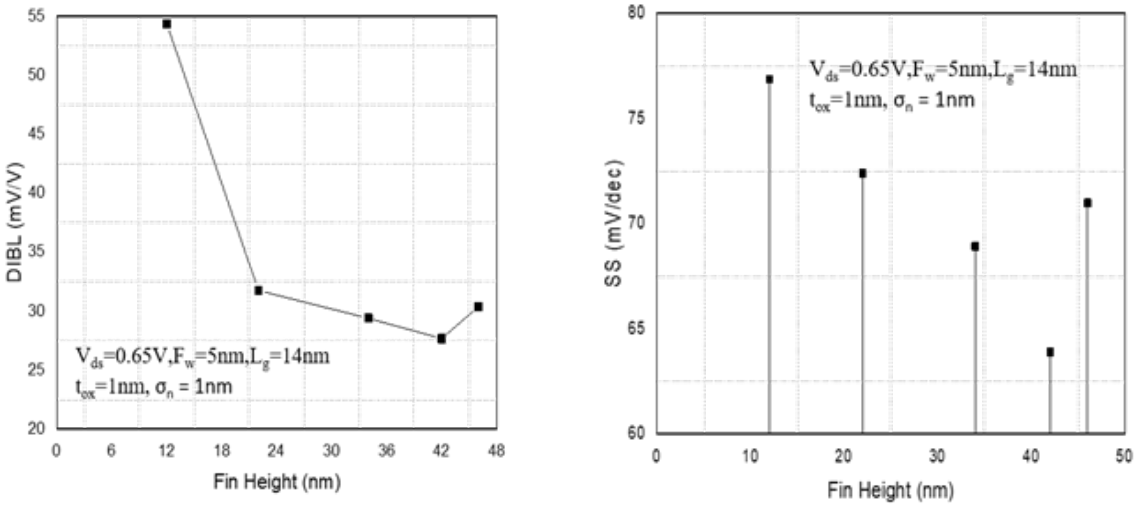


Figure 4. Effect of varying the height of the fin to the drain current for 14nm SOI Gaussian Channel JLFinFET.



(a) (b)

Figure 5. Variation of DIBL and SS for 14nm Gaussian Channel Junctionless FinFET structure for different fin height values.

In the proposed structure of GC-JLFinFET, the peak is located at the sidewall of the fins, and hence the electron density near the surface increases with a gradual decline towards the centre of the fin width. Thus, it is essential to note that the parameters mentioned above, such as peak doping concentration, straggle length and position of the peak, must have optimum values to have less variation on I_{on} and I_{off} concerning the variation in device temperature as well as scaling. Figure 6 depicts the dependence of the spacer dielectric constant on the IV characteristics of GC-JLFinFET. The spacer dielectrics considered for the simulation study are SiO_2, Si_3N_4, $HfSiO_4$ and HfO_2 (k=3.9, 7.5, 11, 25). For a fair comparison, V_{th} of all the spacer materials was tuned to obtain 400mV. It can be clearly noticed that the leakage current is reduced when the k_{sp} is increased. With the increase in the dielectric constant of the spacer material, the off current reduces. As a result, the fringing field lines between the gate electrode and the Source/Drain region increase through the spacer. In turn, it expands the depletion region beyond the edges of the gate in OFF mode, reducing the leakage current of the device due to the decline in the energy barrier to augment the fringe field lines through the spacer, between the Source/Drain extension and gate. This is generally known as Gate Fringe Induced Barrier Lowering.

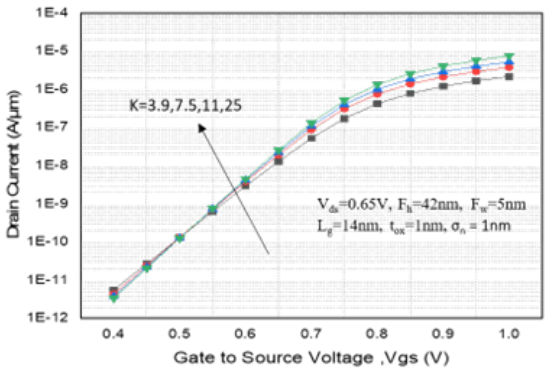


Figure 6. Plot of IV characteristics with spacer dielectric constant on 14nm Gaussian Channel JLFinFET.

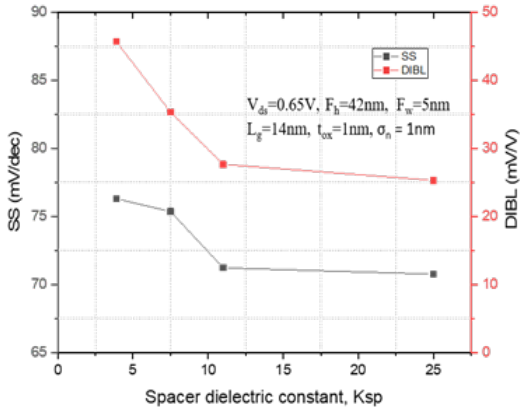


Figure 7. Variation of DIBL and SS with respect to spacer dielectric constant (k_{sp}) of 14nm Gaussian Channel Junctionless FinFET.

Figure 7 explains the variation of DIBL and SS with respect to spacer dielectric (k_{sp}). The data of both DIBL and SS is improved due to the increase in the spacer dielectric constant. Therefore, the proposed GC-JLFinFET structure with a high-k spacer is a promising candidate for enhanced electrical characteristics. It is imperative to study the effectiveness of gate dielectric in the device. The corresponding I_dV_g characteristics of variation of drain current for the gate dielectric is given in Figure 8.

Various dielectric materials with dielectric constant such as k=3.9, 7.5,11 and 22 (SiO_2, Si_3N_4, $HfSiO_4$ and HfO_2) are considered for the analysis by keeping the k_{sp}=22 (HfO_2) as constant. For a fair comparison, V_{th} of all the gate dielectric materials was tuned to obtain 400mV. The effective oxide thickness and gate dielectric material must be chosen correctly for a proper optimizing process during the fabrication. The device architecture with high-k gate dielectric material such as HfO2 (k-=22) has many fringing field lines close to the Source/Drain side, which diminishes the gate's control over the channel. The electric field in the channel and drain region is developed because of the rising fringe field, and hence these results in poor short channel characteristics, as mentioned in Figure 9.

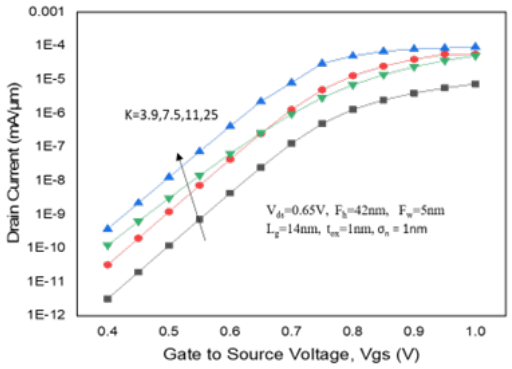


Figure 8. I_dV_g characteristics of variation of drain current with respect to the gate dielectric for 14nm Gaussian Channel JL-FinFET.

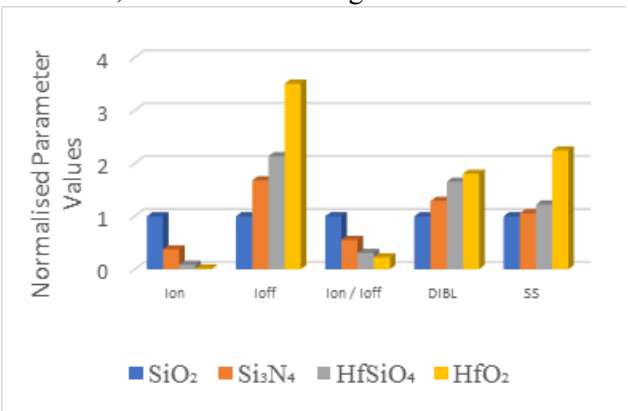


Figure 9. Normalized parameter values for GC-JLFinFETs for different gate dielectric constants.

Thus, the simulated data indicate that the Gaussian Channel JL-FinFET performs better with a lower gate dielectric constant in the Subthreshold. As the Junctionless device operates in bulk conduction

mode, the gate leakage current will not show much effect due to the presence of low-k dielectric material such as SiO_2. The GC-JLFinFET device shows an exemplary gate leakage conduct when it is in OFF condition (i.e., $5.676x10^{-18}$) with Silicon dioxide of k=3.9 as the gate dielectric. Hence, the consolidation of the low-k gate dielectric constant and high-k spacer dielectric in the 14nm GC-JLFinFET will provide a promising performance as tabulated in Table 2 and the electrical characteristics are compared with [20] where the device parameters for both works are stated in Table 1.

Table 2. Performance analysis of different doping configurations of 14nm Junctionless FinFET. The I_{on} extraction is based on V_{gs}=0.4V; V_{ds}=0.65V and I_{off} extraction is based on V_{gs}=0V; V_{ds}=0.65V.

Electrical Characteristics	Gaussian Channel JL-FinFET [20]	Uniformly JL-FinFET simulation	Gaussian Channel JL-FinFET simulation
Ion (A/µm)	4.84×10^{-6}	1.02×10^{-6}	1.78×10^{-5}
Ioff (A/µm)	N/A	4.57×10^{-10}	5.54×10^{-10}
Ion/Ioff	1.1×10^{7}	2.2×10^{5}	3.2×10^{7}
DIBL (mV/V)	53.6	54.52	25.3
SS (mV/dec)	77.7	70.2	63.88
Transconductance, gm (S/µm)	N/A	1.28×10^{5}	3.62×10^{5}

4. Conclusion

This paper investigated the Gaussian doped channel through 3-D simulations. The effects of fin height, gate dielectric, spacer dielectric and temperature variations on the electrical characteristics such as drain current, Drain Induced Barrier Lowering, Subthreshold Swing were examined, and overall performance was shown to be increased by 25.63%. The proposed design showed better efficiency in short channel characteristics, namely DIBL = 25.3 mV/V, SS = 63.88 mV/dec and Transconductance =$3.621x10^5$ S/µm. The simulated results also show that the Gaussian Channel JL-FinFET exhibited enhanced ON current along with the improved Short Channel Characteristics and an overall improvement in the device's performance by 23.8%. We conclude that the presented architecture can be used in low power digital circuit applications with the optimum design parameters. Therefore, the presented GC-JLFinFET structure is optimized for potent device architecture in the sub 20nm regime.

Acknowledgments

Authors would like to acknowledge the financial support of the Research University Grant (UTM Fundamental Research) Project No. Q.J130000.3823.22H52. Also, thanks to the Research Management Center (RMC) of Universiti Teknologi Malaysia (UTM) for providing an excellent research environment in which to complete this work.

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