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Simulation on the Effect of Channel Thickness on the Performance of Multi-Bridge Channel Field-Effect Transistor

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Abstract. A Multi-Bridge Channel Field- Effect Transistor (MBCFET) structure has been designed and simulated to characterize its electrical performance. An MBCFET is a device designed to bridge single-channel FETs, allowing more flexibility with signal routing and power management in complex designs. However, MBCFET suffers from Short Channel Effects which degrade its performance. Channel thickness is another important parameter that affect the performance of MBCFETs. Thus, the impact of channel thickness variation on MBCFET performance is investigated in this project. The electrical characteristic of MBCFET such as its threshold voltage (V_{th}), subthreshold swing (SS), on-state current (I_{on}), and off-state current (I_{off}) were obtained and analyzed by using the TCAD simulation tool. Comparing the simulation results to published results indicated that the difference between the results was less than 5% for various parameters. The second part of the simulation work shows that as the channel thickness of an MBCFET increases, V_{th} decreases, I_{on} increases, and SS decreases. However, when the channel thickness is too thin, SS increases significantly, which leads to the device consuming higher power with lower performance.

1. Introduction

The Multi-Bridge-Channel MOSFET (MBCFET) has multiple channels that are separated by a thin insulating layer [1]. The channels are connected by a bridge structure, which allows for efficient electron transport between them. This design helps to improve the transistor's performance by reducing resistance and increasing current flow. An MBCFET has been proposed to replace the current technology of FinFET which overcomes their performance restrictions by increasing drive current capabilities while simultaneously increasing power efficiency by lowering supply voltage levels [2,3]. Nevertheless, the conventional MBCFET suffers from severe Short Channel Effects (SCE) which can significantly reduce its performance.

The researchers have focused on improving the performance of MBCFETs by experimenting with different device parameters. For example, adjusting the thickness of gate oxide. As the gate oxide thickness is reduced, the gate-channel capacitance increases proportionally [4]. This increase in capacitance causes more carriers to accumulate in the channel region, which leads to the formation of the channel at a lower potential difference. However, with a thinner oxide layer, the dielectric breakdown voltage decreases, which limits the maximum voltage that can be applied to the gate and increases the susceptibility of the device to breakdown under high voltage conditions [4].

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The performance of MBCFET can be improved by varying the channel thickness to ensure it has a lower threshold voltage (V_{th}), steeper subthreshold slope, SS, and higher I_{on} compared to the conventional MBCFET [5]. In general, these studies suggest that varying the channel thickness can significantly affect the device's electrical characteristics.

To optimize the performance of MBCFETs, it is essential to understand the impact of channel thickness variation on their performance levels which can be achieved through simulations. Therefore, the main objectives of this work are to design and simulate the MBCFET by using Atlas Silvaco TCAD software in order to obtain its electrical characteristics. Next, these electrical characteristics are compared with published results to ensure the simulation accuracy. Moreover, this project aims to investigate the impact of channel thickness variation on MBCFET performance.

2. Methodology

2.1 Simulation Setup

At the beginning, the simulation process is started with structures specification which were based on the design proposed in reference [6]. Besides, the MOS model was selected in the simulation, as it is a standard model commonly used for MOSFETs. Next, a numerical method which is NEWTON was selected as it provides quadratic convergence and is well-suited for the simulation of MBCFET. With these requirements in place, the simulation was initiated. The I-V characteristics graph can be obtained by running the simulation. If the result is not expected, then the process will loop back to modify the physical models and numerical methods. Once the simulation results match the expected results, then the design structure will be confirmed and finalized.

Figure 1 shows the structure of the simulated conventional MBCFET while Table 1 displays the device parameters used in this project. MBCFET with gate length of 12 nm, source-drain doping of 3×10^{20} cm^{-3} , channel doping of 1×10^{17} cm^{-3} and drain source voltage of 0.65 V is simulated followed by the reference [6]. The gate is made of Titanium Nitride (TiN) and has a work function of 4.57 eV.

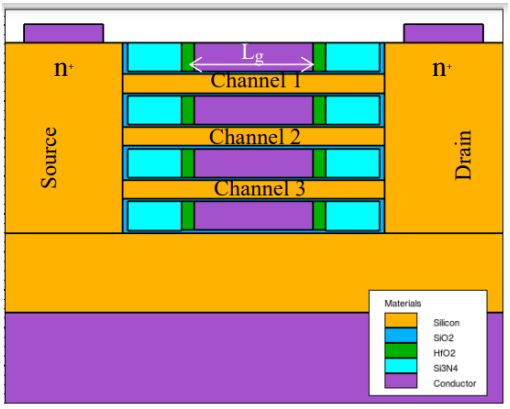


Figure 1. The simulated conventional MBCFET structure [6].

Table 1. Device parameters used in this work.

Device parameters	Published result [5]	This work
Gate length, L_g (nm)	12	12
Source drain doping, N_{sd}(cm^{-3})	3×10^{20}	3×10^{20}
Channel doping (cm^{-3})	1×10^{17}	1×10^{17}
Source Drain Voltage, V_{DS}(V)	0.65	0.65
Work function of the gate (V)	4.57	4.57
Thickness of Silicon Oxide (SiO_2) (nm)	0.5	0.5
Thickness of Hafnium Oxide (HfO_2) (nm)	1.28	1.28
Thickness of each nanosheet, NSHTH (nm)	5	5
Width of each nanosheet, NSHW (nm)	50	50
Thickness of gate (nm)	-	12
Thickness of Substrate (nm)	-	22.5
Source and Drain Length (nm)	-	3

2.2 Measurement of Parameters

2.2.1 Measurement for Threshold Voltage (V_{th})

The threshold voltage is an important parameter of an MBCFET. It is the voltage level at which the FET begins to conduct current. The threshold voltage affects the performance of the FET so it must be taken into consideration when determining the device performance. The threshold voltage can be extracted from the linear extrapolation of the $I_D - V_G$ curve known as the Extrapolation in the Linear Region (ELR) method [7]. This technique involves linearly extrapolating the $I_D - V_G$ curve to obtain an estimate for the device threshold voltage by finding the gate-voltage axis intercept of the linear extrapolation of the $I_D - V_G$ curve at its maximum slope point or the point of maximum transconductance (g_m) [7]. Figure 2 shows the ELG method with the threshold voltage of 0.51V and the maximum slope is at $V_G = 0.72V$.

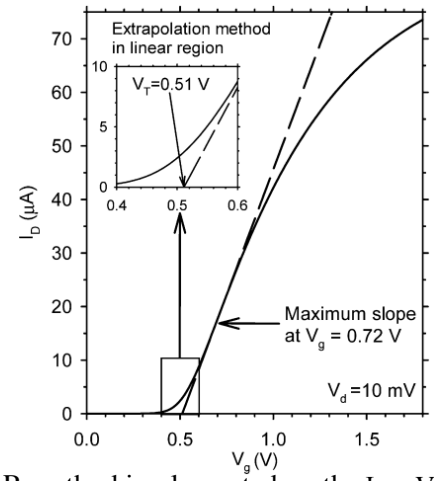


Figure 2. ELR method implemented on the $I_D - V_G$ characteristics [6].

2.2.2 Measurement for Sub-threshold Swing (SS)

The gate to source voltage change required to produce a decade change in the drain current is represented by the subthreshold swing. It can be determined using the subthreshold region's inverse slope of the logarithmic scale of drain current versus gate voltage. Typically, a lower subthreshold swing is preferred

to have a quicker switch from off current to on current. According to studies, a lower subthreshold swing tends to have a greater threshold voltage and less leakage current consumption, which greatly improves the device's performance. The Boltzmann approximation states that the optimum subthreshold swing is roughly 60 mV/Dec. For a FET device, the Subthreshold Swing can be represented in Equation (1) as [7]

$$SS = \frac{dV_{gs}}{d(\log I_{ds})} \tag{1}$$

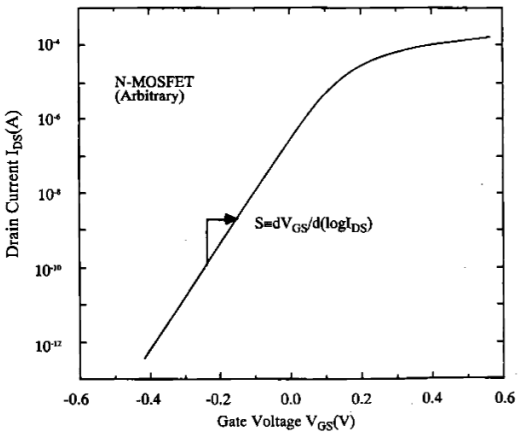


Figure 3. The measurement for Sub-threshold Swing (SS) on the current-voltage (IV) characteristic ($I_D - V_G$) [7].

2.2.3 Measurement for ON & OFF State Current (I_{on} & I_{off})

I_{on} represents the drain to source current when there is a corresponding potential difference applied to the gate and source of the transistor while I_{off} represents the leakage current when there is no bias applied to the gate of a FET. In order to minimize the loss in static power, a low I_{off} is preferred. The gate switching delay is decreased as I_{on} increases. Hence, a high I_{on} / I_{off} ratio denotes an improvement in performance in general. I_{on} can be measured at the maximum V_G while I_{off} can be measured at the minimum V_G [8]. Figure 4 indicates that I_{on} is at V_G of 2 V and I_{off} is at V_G of 0 V when drain voltage is equal to 1 V.

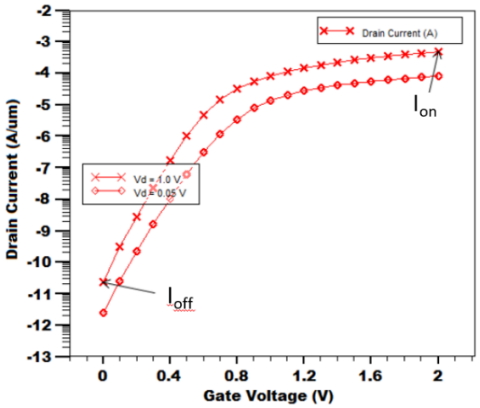
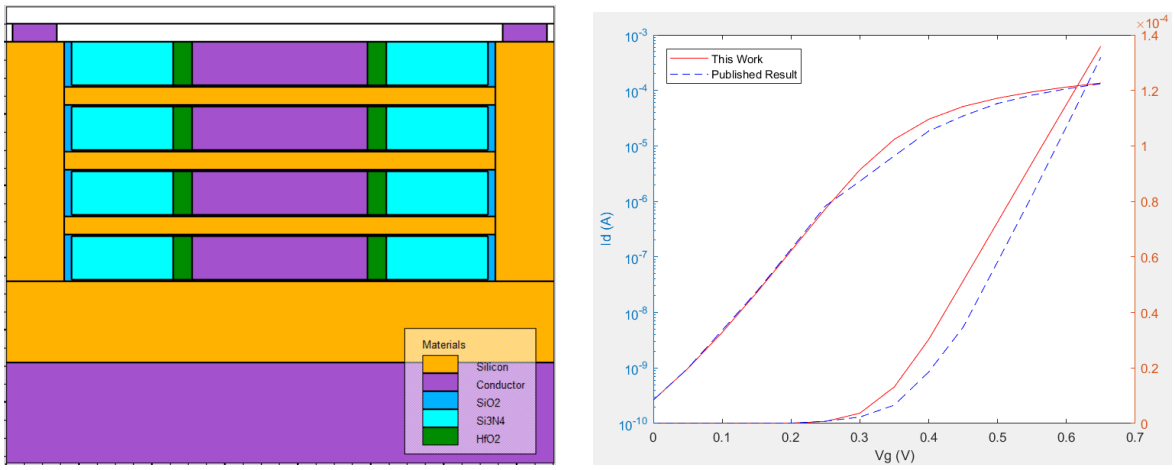


Figure 4. The measurement for ON & OFF State Current (I_{on} & I_{off}) on the $I_D - V_G$ characteristics [8].

3. Results and Discussion

3.1. Simulation Structure for MBCFET

The MBCFET structure has been successfully designed by using Silvaco TCAD tool and the structure and its electrical characteristics are shown in Figure 5. The electrical characteristic such as threshold voltage, subthreshold swing and on-state current were obtained from its I_D- V_G characteristic. The simulated results were compared with the published result in order to verify the validity of the simulated structure.



(a) (b)

Figure 5. (a) The simulated MBCFET structures in this work **(b)** Drain current against gate voltage (I_D-V_G) characteristics of simulated conventional MBCFET in this work.

Based on Figure 5(b), the red line indicates the I_D - V_G characteristics obtained in this work while the blue dotted line indicates the I_D - V_G characteristics from the published result from Ref[4]. The I_D - V_G characteristics show how the current flowing through the device (I_D) changes as the voltage applied to the device (V_G) is varied. From the observation, the I_D - V_G characteristics obtained in the current work are similar to those from a previously published result, for a range of different voltage values (V_G). Hence, we can conclude that the simulated MBCFET in this work has consistent and reliable electrical behaviour.

Table 2. Performance Comparison.

Parameters	Published result [4]	This work	Error (%)
Threshold Voltage ,V_{th} (V)	0.27	0.26	3.70
On current , I_{on} (A)	1.32×10^{-4}	1.36×10^{-4}	3.03
Subthreshold Swing, SS (mV/decade)	70.01	66.75	4.66

Based on Table 2, the difference between the two sets of results is less than 5% for various parameters. Therefore, the proposed structure and methodology for the MBCFET is likely to be accurate and reliable. A low percentage error would indicate that the simulation is reliable and can be used to predict the behaviour of the proposed MBCFET. Hence, the validity of the simulated structure was successfully verified.

3.2. Comparison of different channel thickness

In addition to the initial simulation, second simulation was also performed to compare the behavior of the MBCFET with different channel thicknesses. This is an important aspect to consider in the design of electronic devices, as the thickness of the channel can greatly affect the device's performance. By simulating the MBCFET with different channel thicknesses, we can understand how this parameter affects the device's behavior and optimize the design accordingly. The simulated structure that have verified previously was used to execute the second simulation. Figure 6 shows the I-V characteristics of MBCFET with different channel thickness from 0.5 nm to 7 nm.

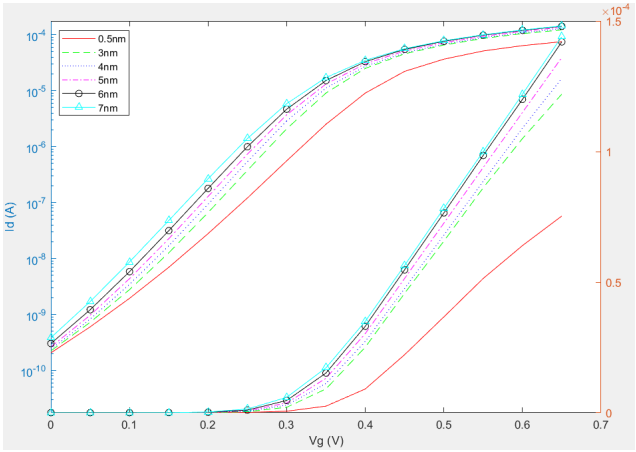


Figure 6. Drain current against gate voltage (I_D - V_G) characteristics of simulated conventional MBCFET with different channel thicknesses.

Table 3. Device performance with different channel thicknesses.

Channel Thickness (nm)	V_{th}	I_{on}	SS
	(V)	(A)	(mV/decade)
0.5	0.32	7.53×10^{-5}	76.03
3	0.28	1.22×10^{-4}	56.69
4	0.27	1.28×10^{-4}	66.57
5	0.26	1.36×10^{-4}	66.75
6	0.25	1.42×10^{-4}	67.24
7	0.24	1.44×10^{-4}	68.52

Based on the results showed in Table 3, as the channel thickness increases, the threshold voltage decreases and the on-state current increases. The threshold voltage is the voltage at which the device starts to conduct current, and a lower threshold voltage means that the device will start to conduct current at a lower voltage, which can be beneficial for some applications. On the other hand, the on-state current is the current flowing through the device when it is in the "on" state, a higher on-state current can be beneficial for some applications. However, as the channel thickness increases, the subthreshold swing decreases, which means that the device will have a less steep slope of the current-voltage characteristics near the threshold voltage. Subthreshold swing is a measure of the device's ability to turn off completely when the voltage is below the threshold voltage.

Additionally, when the channel thickness is too thin, the subthreshold swing increases, which would result in less steep slope of the current-voltage characteristics near the threshold voltage, making it harder to turn off the device completely when the voltage is below the threshold voltage. As a result, the device becomes less sensitive to the voltage applied to the gate as the subthreshold swing increases. This can cause the MBCFET to have a higher power consumption and a lower performance.

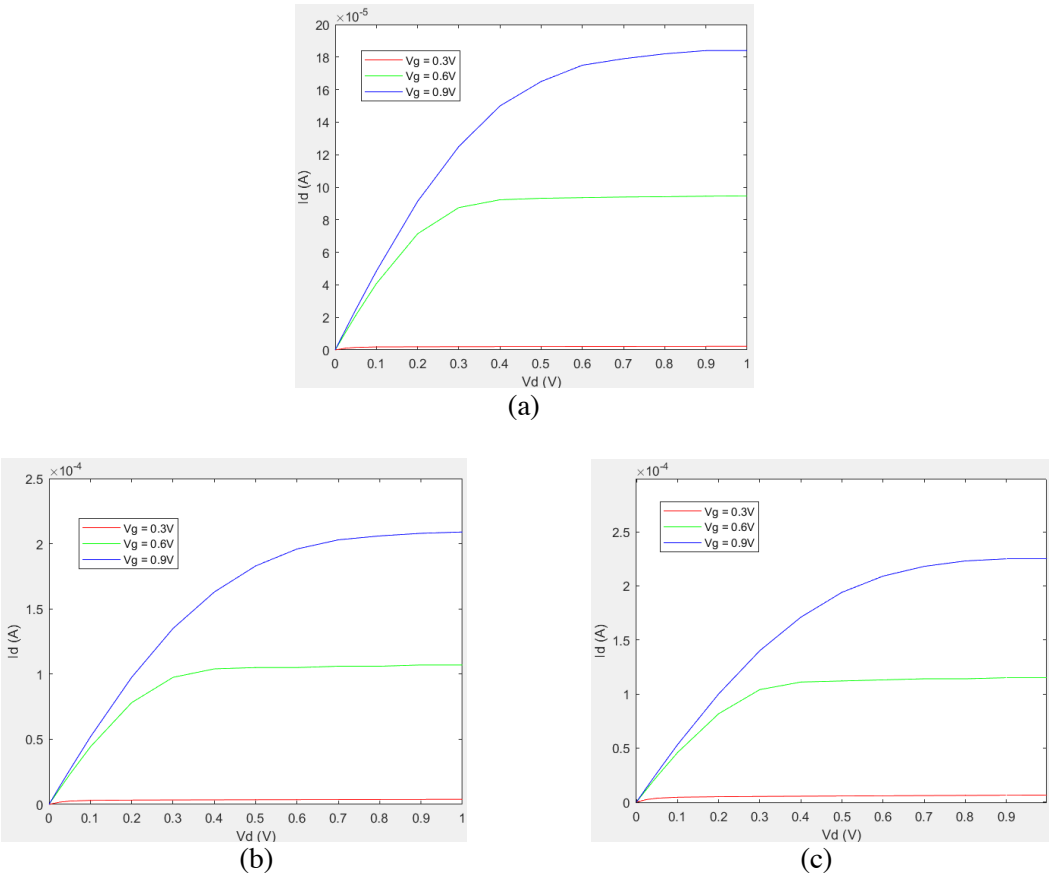


Figure 7. Drain current against drain voltage (I_D - V_D) characteristics of MBCFET with channel thicknesses of (a) 3 nm (b) 5 nm (c) 7 nm.

To plot the I_D - V_D of the MBCFET, a sufficient gate voltage is applied to turn on the device which are 0.3 V, 0.6 V and 0.9 V. When a voltage is applied across the drain and source regions (V_D), a drain current begins to flow. When V_D is small, the MBCFET behaves like a resistor, where the drain current increases linearly with increasing V_D. In this region, the MBCFET is said to be operating in the linear region of the I_D - V_D curve. However, as I_D - V_D is further increased, the channel becomes fully depleted and the MBCFET enters the saturation region. In saturation region, further increases in the drain voltage do not significantly affect the drain current, since the channel is already fully depleted and the drain current is at its maximum value. This behavior is shown in Figure 7(a), (b) and (c) where the drain current is seen to vary linearly at lower drain voltages and becomes constant as the drain voltage increases.

4. Conclusion

An MBCFET structure has been designed and simulated to characterize its electrical performance. Comparing the simulation results to published results indicated that the difference between the results was less than 5% for various parameters. These results suggest that the simulation results agree with the published. Therefore, the proposed structure and methodology for the MBCFET are accurate and reliable. In addition, the second simulation shows that as the channel thickness of an MBCFET increases, V_{th} decreases, I_{on} and SS increase. However, when the channel thickness is too thin, SS increases significantly, which leads to the device consuming higher power with lower performance.

Acknowledments

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