Journal of Physics: Conference Series

PAPER • **OPEN ACCESS**

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To cite this article: Yong Jie Ying and Zaharah Johari 2023 *J. Phys.: Conf. Ser.* **2622** 012023

Simulation and Characterization of Carbon Nanotube-based 2:1 Multiplexer Electrical Properties

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Abstract This paper reports on using simulation to characterize a Carbon Nanotube (CNT) based 2:1 multiplexer (MUX). This study aimed to evaluate the electrical properties, particularly the propagation delay, average power consumption, Power-Delay Product (PDP), and Energy-Delay Product (EDP). Different design approaches namely conventional CMOS, Pass Transistor Logic (PTL) approach, and Gate Diffusion Input (GDI) were adopted. The voltage supply (V_{DD}) and diameter of the CNT are varied to see the effect on the electrical properties. The simulation was carried out using HSPICE. Through simulation, it is found that the GDI approach used the least number of transistors followed by PTL and CMOS. The calculation of the propagation delay exhibits a substantial improvement of more than 95% using the GDI approach. The average power consumption shows a 55.30% and 35.16% reduction when compared to CMOS and PTL respectively. The PDP demonstrates an improvement of more than 95% when compared with conventional CMOS and PTL approaches. The same trend of observation is also achieved for EDP. The variation of the V_{DD} and chirality has a markable effect on the propagation delay and average power consumption. This is a preliminary attempt to evaluate the performance of CNT implementation in MUX. The outcome can become the guideline for engineers working in circuit design using emerging materials for future nanoelectronics applications.

1. Introduction

The scaling down of the transistor to increase its density in an integrated circuit has led to the exploration of emerging materials such as graphene and carbon nanotube (CNT). The use of these emerging materials is expected to sustain the transistor downscaling in the Beyond Moore era, aimed to improve the device performance particularly the power consumption and propagation delay [1]. Moore's Law predicted the number of transistors in an integrated circuit doubled every two years. The miniaturization of the conventional silicon-based transistor performance exhibits a degradation termed short channel effect including threshold voltage rolled–off, leakage current and Drain Induced Barrier Lowering (DIBL) [2]. The implementation of the emerging material is expected that the life span of the device will increase, increasing functionality while reducing the manufacturing cost.

Several studies pertaining to CNT-based material in various applications such as in transistors and sensors have shown promising outcomes. In a study by Zean et al. [3], they showed that CNTFET-based inverters showed a significant decrease in PDP as compared to silicon-based. This is further supported by research conducted by Aara et al. [4] which highlighted the possible reduction in power consumption by 6.30% in a 2:1 MUX application using CNTFET. CNT material used in designing the Analog to Digital Converter (ADC) [5] also has been studied. This study revealed a reduction in the average power consumption by 53.97% when compared with the conventional silicon material. The

need for high-speed devices application may also suit to be implemented using CNT. A study by Newaz et al. [6] has proven a propagation delay enhancement by 45.26% for a full adder circuit. In addition, the priority encoder in [6] implemented with CNT has achieved markable improvement in PDP and EDP.

Although several studies have existed on CNT-based circuit application, additional study is needed to further evaluate its feasible use in other digital circuits such as MUX to further support the previous work. MUX was used in a number of applications such as a communication system as well as the broadcasting of radio and television. The outcome served as the guideline for researchers and experimentalists designing low-power circuits for future electronic device applications. Therefore, this paper simulates and characterizes the CNTFET-based 2:1 MUX application using the established SPICE model simulated in HSPICE extended those from reference [3], [4], and [7]. The electrical performance evaluated is the propagation delay, average power consumption, PDP, and EDP comparing design approaches which are conventional CMOS, PTL, and GDI approaches. The following section describes in detail the methodology.

2. Methodology

The circuit for 2:1 MUX was built using three different approaches namely the conventional CMOS, PTL, and GDI. The constant parameters used for the circuit designing with different design approaches are chirality (n,m) = (19,0) and voltage supply = 0.90V. The voltage supply and chirality are then varied to observe the effects on the propagation delay, average power consumption, PDP and EDP. The simulation to determine the propagation delay, average power consumption, PDP, and EDP was carried out using HSPICE. The CNTFET SPICE Model for 32nm from Stanford University was adopted for this study [8]. The basic 2:1 MUX function is used as a basic building block for the three design approaches. It consists of a selector (S) for selecting the input (D0 or D1) and the output Y. Generally, when S = 0, the output Y will select D0. On the contrary, when S = 1, output Y will select D1.

The propagation delay is measured by taking the average between the high to-low response time, tp_{HL} and low to-high response time, tp_{LH}. tp_{HL} is obtained by taking the response time between the 50% low-to-high at the input and 50% high-to-low at the output while tp_{LH} is obtained by taking the response time between the 50% high-to-low at the input and 50% low-to-high at the output. Equation 1 is used for calculating this propagation delay.

$$t_p = \frac{t_{p_{HL}} + t_{p_{LH}}}{2} \tag{1}$$

PDP is the product between average power consumption and propagation delay. This is calculated using Equation 2 as follows.

$$PDP\ (J) = P_{avg} \times t_p \tag{2}$$

To evaluate the product between PDP and the propagation delay, the EDP is calculated based on Equation 3.

$$EDP\ (Js) = PDP \times t_p \tag{3}$$

3. Design Approaches

The circuit for 2:1 MUX was built using three different approaches namely the conventional CMOS, PTL, and GDI. The constant parameters used for the circuit designing with different design approaches are chirality (n,m) = (19,0) and voltage supply = 0.90V.

3.1. Conventional CMOS 2:1 MUX Design Approach

The conventional CMOS approach uses Pull-Up Network (PUN) and Pull-Down Network (PDN) to produce the output [2]. The PUN is made up of PMOS and the PDN is made of NMOS. The output from PUN is Z while the output from PDN is Z'. In both PUN and PDN, the circuit connected in series represents the 'AND' function and the circuit connected in parallel represents the 'OR' function. A circuit in parallel connection in the PUN will correspond to the circuit connection in series in the PDN and vice versa. For the 2:1 MUX, the circuit is built based on the Boolean equation D0S0' + D1S0. In the PUN, the circuit is connected using PMOS which the inputs are associated with a bar. Therefore, in PUN, the input D0 and S0' will be associated with a bar when connected to PMOS. Thus, D0 and S0' are connected in parallel (D0' OR (S0')'), then series with (AND) the D1 and S0 in parallel (D1' OR S0'). In the PDN, the circuit is connected using NMOS, thus the D0 and S0' are connected in series (D0 AND S0'), then parallel with (OR) the D1 and S0 in series (D1 AND S0). Figure 1 shows the 2:1 MUX and Figure 2 presents the waveform verifying the correct function of the circuits.

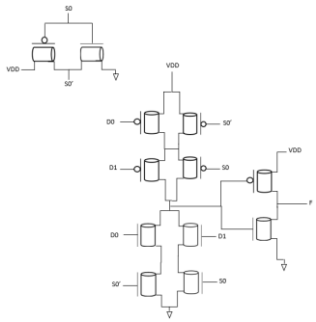

Figure 1. The design of 2:1 MUX using the conventional CMOS approach.

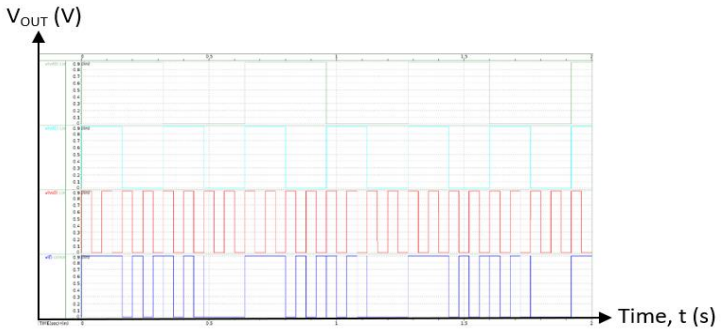

Figure 2. The output waveform of 2:1 MUX using the conventional CMOS approach.

3.2. Pass Transistor Logic 2:1 MUX Design Approach

As opposed to the conventional CMOS approach, the field effect transistor (FET) in PTL is used as the switch to pass the input to the output. PTL uses the NMOS or PMOS to build the circuit. In this study, the NMOS is used in the circuit as the carrier mobility for N–type FET is found to be higher than the PMOS [9]. With the PTL approach, the Source of both NMOS is connected to the D0 and D1 respectively while the Drain of both NMOS is connected to F. The Gate of the upper FET is connected to S0' while the Gate of the bottom FET is connected to S0. Therefore, when S0 = '0', D0 will be passed to the output F through PMOS while when the S0 = '1', D1 will be passed to the output F through NMOS. Figure 3 shows the circuit consisting of a 2:1 MUX connected using only NMOS FET. The waveform is shown in Figure 4.

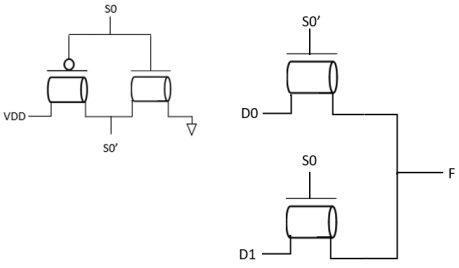

Figure 3. The design of a 2:1 MUX using the PTL approach.

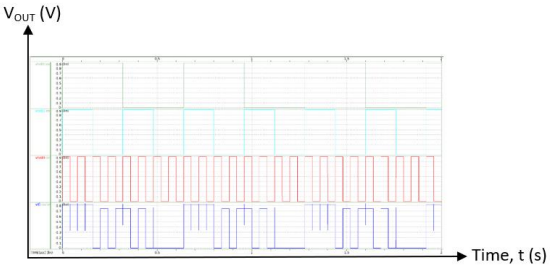

Figure 4. The output waveform of a 2:1 MUX using the PTL approach.

3.3. Gate Diffusion Input 2:1 MUX Design Approach

The GDI technique is aimed to reduce the number of transistors used while providing the same functionality [10]. The GDI technique uses single diffusion input to control the switching of the transistors [11]. A basic GDI cell is made up of a PMOS and a NMOS. There are three input terminals which are G (NMOS and PMOS common gate input), P (PMOS source or drain input), and N (NMOS source or drain input) as well as one output terminal which is OUT [12].

In this study, the GDI approach is implemented to design the 2:1 MUX as shown in Figure 5. GDI is different from PTL as it uses both NMOS and PMOS to design the circuit. With the GDI approach, the Drain of NMOS and the drain of PMOS are connected to output F. The Source of PMOS is connected to D0 while the Source of NMOS is connected to D1. The Gate of both FETs is connected to S0. Therefore, when S0 = '0', PMOS will be activated and the output F will be D0 while when the S0 = '1', the NMOS will be activated, and the output F will be D1 as shown in Figure 6. The circuit was designed using the three approaches, the result is discussed in the following section.

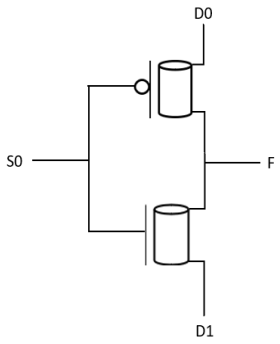

Figure 5. The design of a 2:1 MUX using the GDI approach.

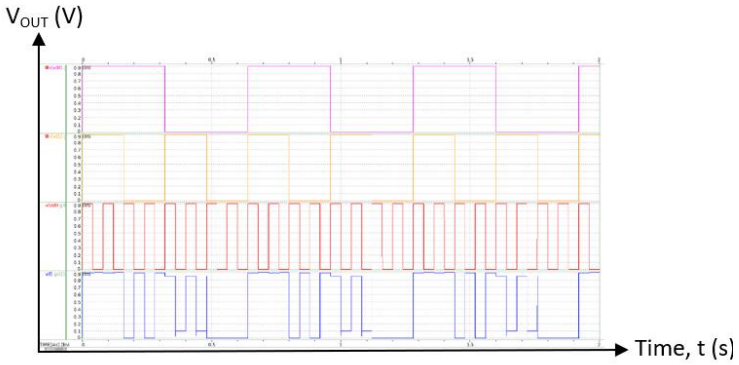

Figure 6. The output waveform of a 2:1 MUX using the GDI approach.

4. Result and Discussion

The 2:1 MUX designed using the three approaches was simulated and characterized. Based on the circuit in Figures 1, 3, and 5, the number of transistors used in conventional CMOS, PTL, and GDI approaches are 12, 4, and 2 respectively. The simulation results obtained in this study indicate the number of transistors in the 2:1 MUX generates a considerable effect on the propagation delay, average power consumption, PDP, and EDP. Based on the simulation, the propagation delay using the GDI approach is significantly lower compared to conventional CMOS and PTL. This can be viewed in Figure 7. The propagation delay for the conventional CMOS approach is less by 42.86% compared to PTL although the number of transistors in PTL is 1/3 of those using conventional CMOS. The same trend of observation was also achieved in [2] where they made a comparison between the conventional CMOS approach and Complementary Pass Transistor Logic (CPL) which the number of transistors in the CPL circuit is lesser than the conventional CMOS approach but still exhibits a longer propagation delay. This outcome can be explained by the voltage drop across the PTL thus resulting in slower signal propagation and hence longer propagation delay than the conventional CMOS approach. According to [13], the PTL approach reduces the number of transistors and reduces the power consumption but sacrifices the propagation delay which causes PTL to have a higher delay than the conventional CMOS approach even if it utilizes a smaller number of transistors.

Table 1. Performance of 2:1 MUX using different design approaches.

Design Approach	Propagation Delay (s)	Average Power Consumption (W)	PDP (J)	EDP (Js)
CMOS	1.40E-1	6.60E-9	9.23E-10	1.29E-10
PTL	2.00E-1	4.55E-9	9.11E-10	1.82E-10
GDI	6.53E-6	2.95E-9	1.93E-14	1.26E-19

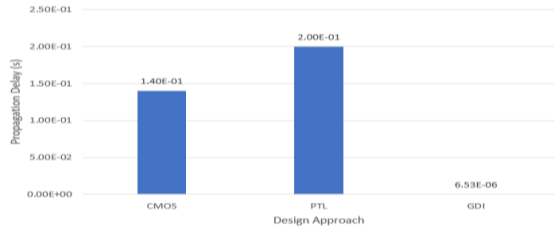

Figure 7. Propagation delay using different design approaches.

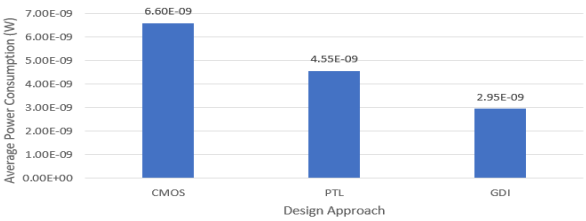

Figure 8. Average power consumption using different design approaches.

Further evaluation of the average power consumption for the 2:1 MUX is shown in Figure 8. It can be observed that the average power consumed using the PTL approach is 31.06% lower compared to conventional CMOS. This is reasonable as the number of transistors used in CMOS is three times more than in PTL. The average power consumption with the PTL approach is approximately 35.16% higher than GDI. The considerably low average power consumption of the GDI approach is due to the lesser number of transistors used in the GDI approach as compared to the PTL approach. This finding supported previous work which also demonstrated that the full adder using a MUX with a GDI approach has lower average power consumption than a conventional CMOS full adder [14].

The propagation delay and the average power consumption directly affect the PDP. Calculations of the PDP for comparing the 2:1 MUX using the three approaches are shown in Table 1. According to Table 1, PDP for conventional CMOS and PTL are close. This is also consistent with the result obtained in [15] where they achieve lower PDP when designing a CNTFET-based comparator using PTL as compared to the CMOS approach. The most striking difference is achieved for 2:1 MUX using the GDI approach. As can be seen, the PDP using the GDI approach has been reduced multiple times. This significant improvement can be due to the simpler topology of the GDI circuit. In the case of EDP, which is the product of PDP and the propagation delay indicates the efficiency of the circuit. It is found from Table 1 that the patterns are essentially the same for PDP for all three design approaches. For example, EDP achieved for the PTL approach is 1.82E-10 Js. This is slightly higher than the conventional CMOS by 41.09%. The multiple decrements of the EDP in the GDI approach are possibly due to the lower power consumption and multiple decrements of the propagation delay of the GDI circuit. Thus, the pro of GDI is able to provide a circuit with lesser energy consumption, lower lag, and smaller area while the cons of GDI is the expensive fabrication cost as it requires a twin-well CMOS or silicon-on-insulator (SOI) process to realize the design [10].

4.1. Effect of Voltage Supply and CNT Diameter

This study also attempts to see the effect when the voltage supplies, V_{DD} and the CNT diameter were varied focusing on the GDI approach as the performance specification outperforms those of PTL and conventional CMOS. It is crucial to investigate the effect of the power supply as it has a direct relation with power consumption. To do this, V_{DD} was varied from 0.90 V to 1.1 V for the GDI approach. The propagation delay and average power consumption are simulated, and the data are presented in Figure 9 and Figure 10.

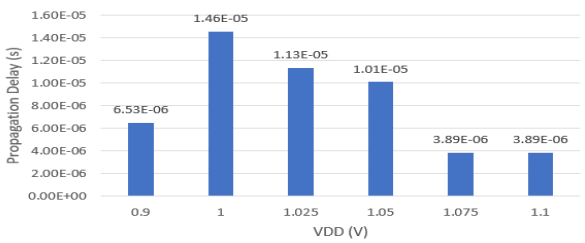

Figure 9. Propagation delay using different voltage supplies for 2:1 MUX.

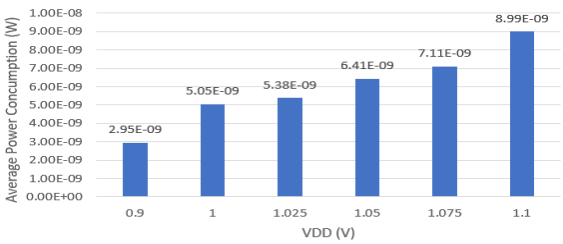

Figure 10. Average power consumption using different voltage supplies for 2:1 MUX.

From Figure 9, it can be seen that there is a variation in the propagation delay when the supply voltage increase. The longest propagation delay achieved is when V_{DD} = 1V which is 123.24% higher than V_{DD} = 0.9 V. However, after V_{DD} = 1V, the propagation delay continues to decrease until V_{DD} = 1.1 V. In fact, at V_{DD} = 1.075 V and 1.1 V the value of the propagation delay changes is close to none. The effect of V_{DD} on the propagation delay has also been studied by Kumar et al. [16] who found that the propagation delay decreases when the V_{DD} increases from 0.80V to 1.00V in CNTFET-based full adder application.

A dramatic increase is achieved in the average power consumption when V_{DD} increases from 0.9V to 1.1V. This simulation result can be viewed in Figure 10. It can be seen that the higher V_{DD} applied consumed more power. There is a significant increase of 71.29% in average power consumption when the VDD increases from 0.90 V to 1.00 V. The same observation is also found in research by Ruhil et al. [17] where they applied V_{DD} from 0.90V to 1.10V and resulting in an upward increase in power consumption. This can be reasoned to power is related to voltage and current, thus increasing voltage indirectly increases power consumption. Table 2 shows the effect on PDP and EDP when supply voltage V_{DD} is varied.

Table 2. Performance of EDP and PDP for different voltage supplies.

V_{DD} (V)	PDP (J)	EDP (Js)
0.900	1.93E-14	1.26E-19
1.000	7.36E-14	1.07E-18
1.025	6.10E-14	6.92E-19
1.050	6.48E-14	6.54E-19
1.075	2.76E-14	1.07E-19
1.100	3.50E-14	1.36E-19

From Table 2, 0.90V is the optimum operating voltage for the 32nm CNTFET, thus increasing the voltage higher than the optimum operating voltage will cause the propagation delay, average power consumption, PDP and EDP to be higher. From Figure 9, it can be concluded that when the V_{DD} increases, the propagation delay will decrease while from Figure 10, it can be observed that the average power consumption will increase when the V_{DD} increases. This result can be benchmarked with the result obtained in [17]. From Table 2, it is shown that the increasing and decreasing of PDP and EDP depend on the value of the propagation delay and average power consumption.

The diameter of the CNT also has a significant effect on the device's performance [18]. To see the effect on the performance specification of the 2:1 MUX with the GDI approach, the chirality n, m is varied. The simulated data for the propagation delay and average power consumption are listed in Table 3.

Table 3. Performance of 2:1 MUX using different diameters of CNT.

Diameter of CNT	Chirality (n,m)	Propagation Delay (s)	Average Power Consumption (W)	PDP (J)	EDP (Js)
0.39nm	(5,0)	1.80E-1	3.69E-12	6.63E-13	1.19E-13
0.78nm	(10,0)	9.20E-6	2.40E-12	2.21E-17	2.03E-22
1.50nm	(19,0)	6.53E-6	2.95E-9	1.93E-14	1.26E-19
2.00nm	(26,0)	1.70E-6	1.60E-8	2.72E-14	4.61E-20

From Table 3, it is obvious that the increment of the CNT diameter greatly affects the propagation delay. For example, the increase of diameter from 0.39nm to double of it which is 0.78nm has shown a multiple times reduction in the propagation delay and the reduction of power. By increasing the diameter from 0.78nm to 1.50nm, it has shown a 29.07% decrement in the propagation delay and a significant increase in power consumption. While the diameter of CNT increases further from 1.50nm to 2.00nm,

the propagation delay decreases further by 73.99% to 1.70E-6 s while the power consumption markedly increases from 2.95E-9 W to 1.60E-8 W. This result is consistent with the result obtained in [18]. From Table 3, it is shown that the increasing and decreasing of PDP and EDP depend on the value of the propagation delay and average power consumption.

5. Conclusion

In conclusion, the GDI approach provides better performance by giving an accurate result while using the least number of transistors as compared to the conventional CMOS approach and PTL approach in terms of propagation delay, average power consumption, PDP, and EDP. GDI gives the least propagation delay, average power consumption, PDP, and EDP which are 6.53E-6 s, 2.95E-9 W, 1.93E-14 J, and 1.26E-19 Js respectively. Besides that, the propagation delay will decrease while the average power consumption will increase when the voltage supply and diameter of the CNT increase. Thus, this research is expected to provide insight into the use of nanomaterials and MUX in designing electronic applications in the future to simplify the circuit while giving a better performance to save cost and area in designing a device using nanomaterial.

Acknowledgments

The authors would like to acknowledge the Ministry of Higher Education for the research grant scheme for financial support under (FRGS/1/2020/STG05/UTM/01/1).

References

[1] Sapan A, Brad A, Hiro A, Otitoaleke A, Mustafa B, Gennadi B and Christian B 2022 Beyond CMOS *IEEE Int. Roadmap for Devices and Systems* pp 1-132

[2] Hussain I, Singh A and Chaudhury S 2018 A review on the effects of technology on CMOS and CPL logic style on performance, speed and power dissipation *IEEE Electron Devices Kolkata Conf. (EDKCON)* pp 332-336 doi: 10.1109/EDKCON.2018.8770506.

[3] Zean M, Aziz A, Islam M, Abir M S M, and Saha S 2017 CNTFET based multiplexers and magnitude comparator *2017 4th Int. Conf. on Advances in Electrical Engineering (ICAEE)* pp 48-53 doi: 10.1109/ICAEE.2017.8255325.

[4] Aara A and Jain S 2019 *Design and implementation of CMOS and CNT based 2:1 multiplexer at 32nm technology*

[5] Sarma A K V V and Choudhary S 2018 A Comparison between MOSFET based and CNTFET based analog to digital converter *2018 Int. Conf. on Recent Innovations in Electrical, Electronics & Communication Engineering (ICRIEECE)* pp 2634-2637 doi: 10.1109/ICRIEECE44171.2018.9008600.

[6] Newaz S, Uddin S M N, Neon M K H and Haque M I 2018 Performance Analysis of Carbon Nanotube Field Effect Transistor Based Digital Circuits *2018 3rd Int. Conf. for Convergence in Technology (I2CT)* pp 1-5 doi: 10.1109/I2CT.2018.8529803.

[7] Agarwal V K, Guduri M and Islam A 2015 Which is the best 2-to-1 line multiplexer for ultralow-power applications? *2015 IEEE Int. Conf. on Computational Intelligence & Communication Technology* pp 655-660 doi: 10.1109/CICT.2015.128.

[8] Stanford CNFET Model - HSPICE | Stanford Nanoelectronics Lab" 2022 *Nano.stanford.edu*

[9] Rajput A, Dua T, Kumawat R, and Srinivasulu 2021 Novel CMOS and PTL based half subtractor designs *IEEE Int. Symposium on Smart Electronic Systems (iSES)* pp 165-168 doi: 10.1109/iSES52644.2021.00047.

[10] Yarlagadda S, Kaza S and N S 2013 Design of low power CMOS logic circuits using gate diffusion input (GDI) technique (*Int. Journal of VLSI Design & Communication Systems* vol 4) pp 89-95 doi: 10.5121/vlsic.2013.4507.

[11] Uma R and Dhavachelvan P 2012 Modified gate diffusion input technique: a new technique for enhancing performance in full adder circuits (*Procedia Technology* vol 6) pp 74-81 doi: https://doi.org/10.1016/j.protcy.2012.10.010.

[12] Kumar B S, Jayanthi S and Rakshgan 2022 Design of 8:1 multiplexer using gate diffusion input (GDI) technique and comparison of delay performance with pass transistor logic *2022 14th*

Int. Conf. on Mathematics, Actuarial Science, Computer Science and Statistics (MACS) pp 1-5 doi: 10.1109/MACS56771.2022.10022682.

[13] Kumar A, Tripathi S L and Subramaniam U 2022 Variability analysis of SBOX with CMOS 45 nm Technology *(Wireless Personal Communications vol 124)* pp 671-682 doi: 10.1007/s11277-021-09377-0.

[14] Mukherjee B and Ghosal A 2015 Design & study of a low power high speed full adder using GDI multiplexer *2015 IEEE 2nd Int. Conf. on Recent Trends in Information Systems (ReTIS)* pp 465-470 doi: 10.1109/ReTIS.2015.7232924.

[15] Lubaba S, Faisal K M, Islam M S and Hasan M 2020 Design of a two-bit magnitude comparator based on pass transistor, transmission gate and conventional static CMOS logic *2020 11th Int. Conf. on Computing, Communication and Networking Technologies (ICCCNT)* pp 1-5 doi: 10.1109/ICCCNT49239.2020.9225501.

[16] Kumar K, Sahithi C, Sahoo R and Sahoo S K 2014 Ultra low power full adder circuit using carbon nanotube field effect transistor *2014 Int. Conf. on Power, Control and Embedded Systems (ICPCES)* pp 1-4 doi: 10.1109/ICPCES.2014.7062796.

[17] Ruhil S, Rohilla K and Sehgal J 2015 *CNTFET Based Energy Efficient Full Adder*

[18] Laribi, A and Bouazza A G 2018 Effect of chirality and oxide thickness on the performance of a ballistic CNTFET *Int. Journal of Electrical and Computer Engineering (IJECE)* doi: https://doi.org/10.11591/IJECE.V8I6.PP4941-4950