

**IMPROVED CHARACTERISTICS OF RADIO FREQUENCY  
INTERDIGITAL CAPACITOR**

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*To My Beloved Family*

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## ABSTRACT

Technology advances in complimentary-metal-oxide-silicon (CMOS) process offer some interesting possibilities for radio frequency (RF) circuit designers. Some circuits that would have to be done with GaAs monolithic microwave integrated circuits (MMICs), for instance, are now possible in CMOS. While the transistor speed has been improving significantly, fuller integration of RF integrated circuits (RFICs) is often retarded by the absence of high quality, high rangeability and efficient on-chip passive components. This thesis presents the possibilities of improving the characteristics of an RF capacitor having interdigital configuration. Modifications in the form of combline structure were introduced into the conventional configuration to improve the capacitor characteristics. Performance in the form of capacitance and Quality, Q, factor were investigated through simulations using electromagnetic simulation software, Ansoft HFSS. The analysis and comparison between conventional and the proposed interdigital capacitor (IDC) with combline structure were discussed in detail. It can be concluded that the proposed IDC with combline structure improves the capacitance of an IDC. The optimum combline configuration which achieved useful capacitance with sufficiently high Q factor is the design with 110 mils effective finger length. It produces 5.48 pF capacitance at first resonance of 2 GHz, with sufficiently high Q factor of 13.88. This is a factor of 1.72 higher than the corresponding conventional IDC having 3.18 pF at first resonance of 3 GHz albeit 10 % slightly higher Q factor of 15.41.

## ABSTRAK

Kecanggihan teknologi pemrosesan silikon-oksida-logam-pelengkap (CMOS) menawarkan peluang menarik kepada perekabentuk litar frekuensi radio. Sesetengah litar yang perlu direkabentuk seperti menggunakan litar bersepadu gelombang mikro monolitik (MMICs), kini boleh dilakukan dengan teknologi CMOS. Sementara kelajuan transistor meningkat dengan pesat, penyepaduan sepenuhnya litar bersepadu RF (RFIC) terbantut oleh ketiadaan komponen pasif atas-cip yang berkualiti tinggi, berkeboleharapan tinggi dan tinggi kecekapan. Tesis ini membentangkan kemungkinan untuk membuat penambahbaikan terhadap ciri kapasitor RF menggunakan konfigurasi interdigital. Modifikasi berbentuk struktur talian komb diperkenalkan pada kapasitor interdigital konvensional untuk memperbaiki ciri prestasinya. Prestasi dalam bentuk kapasitan and faktor kualiti (Q) dikaji menerusi simulasi perisian elektromagnet, Ansoft HFSS. Analisis dan perbandingan antara kapasitor interdigital konvensional dan kapasitor interdigital dengan struktur talian komb dibincang dengan terperinci. Dapat disimpulkan bahawa kapasitor interdigital dengan struktur talian komb meningkatkan kapasitan bagi kapasitor interdigital. Konfigurasi talian komb optimum yang memperoleh kapasitan berguna dan faktor Q yang cukup tinggi adalah rekabentuk dengan panjang jari berkesan bernilai 110 mil. Ia menghasilkan kapasitan 5.48 pF pada resonans pertama 2 GHz dengan faktor Q mencukupi sebesar 13.88. Nilai ini adalah 1.72 lebih tinggi berbanding struktur IDC konvensional dengan 31.8 pF pada resonans pertama 3 GHz, namun dengan faktor Q = 15.41 yang 10 % sahaja lebih tinggi.

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**LIST OF SYMBOLS**

$A$	-	Area
$C$	-	Capacitance
$d$	-	Distance
$f$	-	Frequency
$f_o$	-	Self resonance frequency
$h$	-	Dielectric thickness
$L$	-	Inductance
$l$	-	Fingers length
$l'$	-	Effective fingers length
$M$	-	Number of capacitors connected in a network
$N$	-	Total capacitor fingers
$N'$	-	Total combline fingers per finger
$Q$	-	Electric charges
$R$	-	Resistance
$s$	-	Spacing between fingers
$s'$	-	Spacing between combline fingers
$t$	-	Conductor height
$w$	-	Finger width
$w'$	-	Comblines fingers width
$X_c$	-	Reactance
$\epsilon_r$	-	Dielectric relative permittivity

**LIST OF ABBREVIATIONS**

CMOS	-	Complementary metal oxide semiconductor
ESL	-	Equivalent series inductance
ESR	-	Equivalent series resistance
FDTD	-	Finite-difference time domain
FEM	-	Finite element model
IC	-	Integrated circuit
IDC	-	Interdigital capacitor
MIM	-	Metal-insulator-metal
MOSFET	-	Metal oxide semiconductor effect transistor
PCB	-	Printed circuit board
Q	-	Quality factor
RFIC	-	Radio frequency integrated circuit



## CHAPTER I

### INTRODUCTION

#### 1.1 Background of Study

The growth of smaller, more power-sensitive wireless-communication products has fueled the explosive development of radio frequency integrated circuits (RFICs) [1]. Highly integrated RF components now populate ICs, replacing the hybrid circuits that used discrete semiconductor devices. As a result, RFICs can be found in applications that blanket the wireless space, ranging from cellular to wireless LANs and everything in between. There are many challenges involved in creating RFICs. At the transistor level, various competing technologies (GaAs, Si, SiGe, and CMOS) each provide different benefits and drawbacks. Aside from the transistors, the creation of passive components such as inductors, capacitors, and resistors also pose unique challenges to the IC designer.

Passive components are referred to as “glue components” because they “glue” integrated circuits together to make a system. For the accurate design and fabrication of these compact high performance systems, accurate modeling of on chip passive components is becoming very important. However, designing circuits with these passive components is non-trivial due to electromagnetic interactions that lead to parasitic, and ultimately non-ideal frequency behavior. Passive devices

generally have complex geometries, non-uniform current flow, and correspondingly complex field patterns; therefore, suffer from parasitic effects that influence the electrical behavior of the device at different frequencies. For this reason, accurate models of passive components are crucial for designing and characterizing high performance systems.

Building high-quality on-chip capacitors has attracted tremendous interest from the RFIC design community and semiconductor manufacturers. High-quality on-chip capacitors have been widely demonstrated as a key factor for successfully integrating RF building blocks, such as resonant circuits and filters, voltage-controlled oscillators, coupling between stages and bypassing [1]. Other characteristics by which such capacitors are judged include capacitance density; parasitic capacitance to ground; voltage, temperature and frequency coefficients; and the maximum allowable peak repetitive voltage. As shown in *Figure 1.1*, commercial CMOS or BiCMOS processes the following capacitors are generally available:

**(a) Capacitors that use the MOSFET gate oxide [2]**

The highest capacitance densities are obtained with these capacitors. Capacitance density of  $6 \text{ fF}/\mu\text{m}^2$  has been reported [2]. However, there is a trade-off between the gate oxide thickness and the breakdown voltage. A 50-Angstrom gate oxide capacitor in a  $0.25\mu$  processes can typically withstand a maximum peak repetitive voltage of 2.75V. Depending on the topology and circuit design this may be a limitation. The CV characteristic varies with the particular process technology and is non-linear. This non-linearity may cause distortion in the circuit.

**(b) Metal-insulator-metal (MIM) capacitors [3, 4]**

MIM capacitors are typically built near the top of the metal stack to minimize parasitic capacitance to ground; for example, a bottom-plate using METAL4 and a top-plate using METAL5 separated by a thin insulator layer a few hundred Angstroms thick. The large separation between the bottom plate and substrate ( $\cong 6\mu$ )

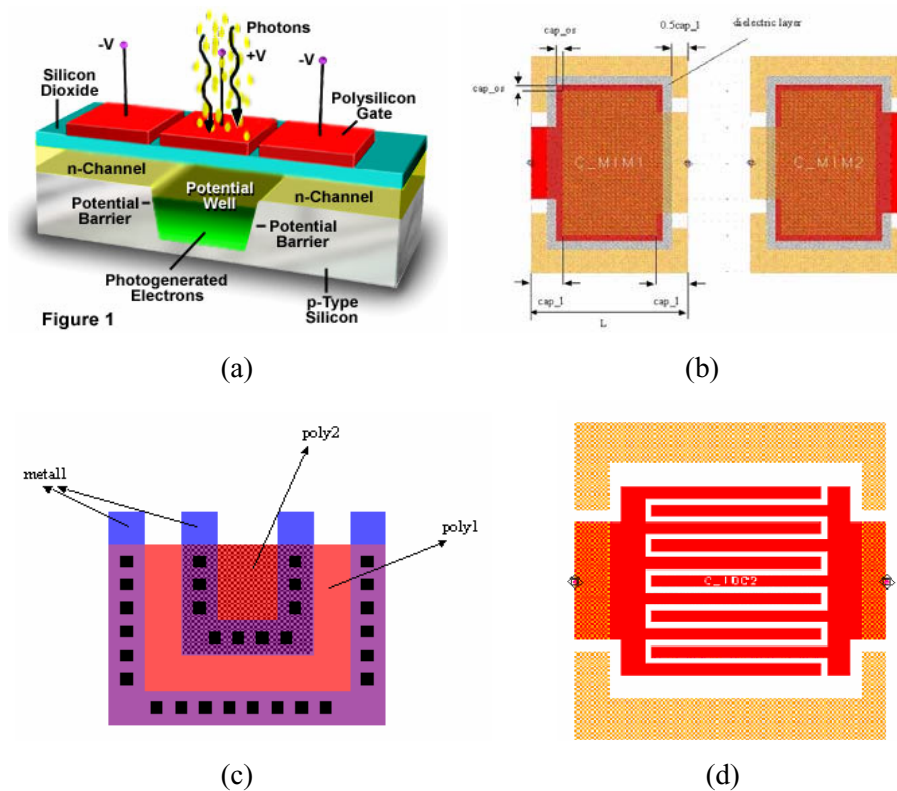
helps in reducing the parasitic capacitance to ground to approximately 2% of the useful inter-metal capacitance (trans-capacitance). MIM capacitors have very good voltage and temperature-coefficient characteristics and a capacitance density of approximately  $0.8\text{fF}/\mu^2$ . MIM capacitors are available in many RF CMOS and BiCMOS processes, however, they require extra masking steps to implement and increase the cost of the IC. Furthermore, these devices do not scale with process technology

**(c) Poly-insulator-gate poly (Double Poly) capacitors [2]**

Double-poly and MOS capacitors also have parasitic capacitance associated with them. Double-poly capacitors have about 18% parasitic capacitance to ground while MOS capacitors can have 2~20% parasitic capacitance to ground depending upon their design. Both MOS and double-poly capacitors have the problem of very high series resistance to one of the two nodes.

**(d) Planar Interdigital capacitor (Planar IDC) [5]**

Planar Interdigital capacitors hold much promise in providing capacitors that continue to improve with succeeding process technologies. Capacitance density increases significantly as the number of metal layers increase and the feature size decreases. Such capacitors can be optimized to minimize parasitic capacitance and to make the parasitic capacitance symmetric, thus reducing noise pickup from the substrate or nearby structures.



**Figure 1.1:** Different types of CMOS or BiCMOS capacitor. (a) MOSFET gate oxide capacitor, (b) MIM Capacitor, (c) Double-poly capacitor, (d) IDC

## 1.2 Goals and Limitations of On-chip Capacitor Design

High-performance on-chip capacitors are required to implement RF integrated circuits [6]. The main requirements for high-performance capacitors are capacitance density, symmetry and high quality factor. Recent literature [6] emphasizes exclusively either high capacitance density or high Q because improvement in Q tends to come at the expense of capacitance density.

For a number of sensitive applications, capacitors with a  $Q > 15-20$  at frequency range of interest are required. However, there is a limitation in obtaining a

high Q factor especially at high frequency range in most of today's applications. These limitations in the poor Q factor are primary due to the resistive losses in the plates and contacts and due to the parasitic capacitance between the passive component and the lossy silicon substrate [7]. Thus, lots of researches and studies are currently on going and some has been carried out focusing on different ways to obtain high Q and high capacitance capacitors. Some researches focus on various capacitors layout and dimensions; some of these studies focus on material science looking for new low loss materials which is suitable for planar capacitor implementation. Accurate capacitor model which gives accurate simulation results for Q factor and series resistance (ESR) is crucial as well for RF circuit design and characterization.

### **1.3 Objectives**

The main objective of this project is to improve the characteristics of a planar interdigital radio frequency capacitor by employing combine structure. The performance in the form of capacitance and Q factor of the modified interdigital capacitor with the conventional configuration interdigital capacitor are compared. It is aimed to obtain a planar combline interdigital capacitor which is able to produce higher capacitance with sufficiently high Q factor of at least 15 in a wider frequency range which suits today's application in various fields. The basic and combline configurations are depicted in *Figure 1.2*.

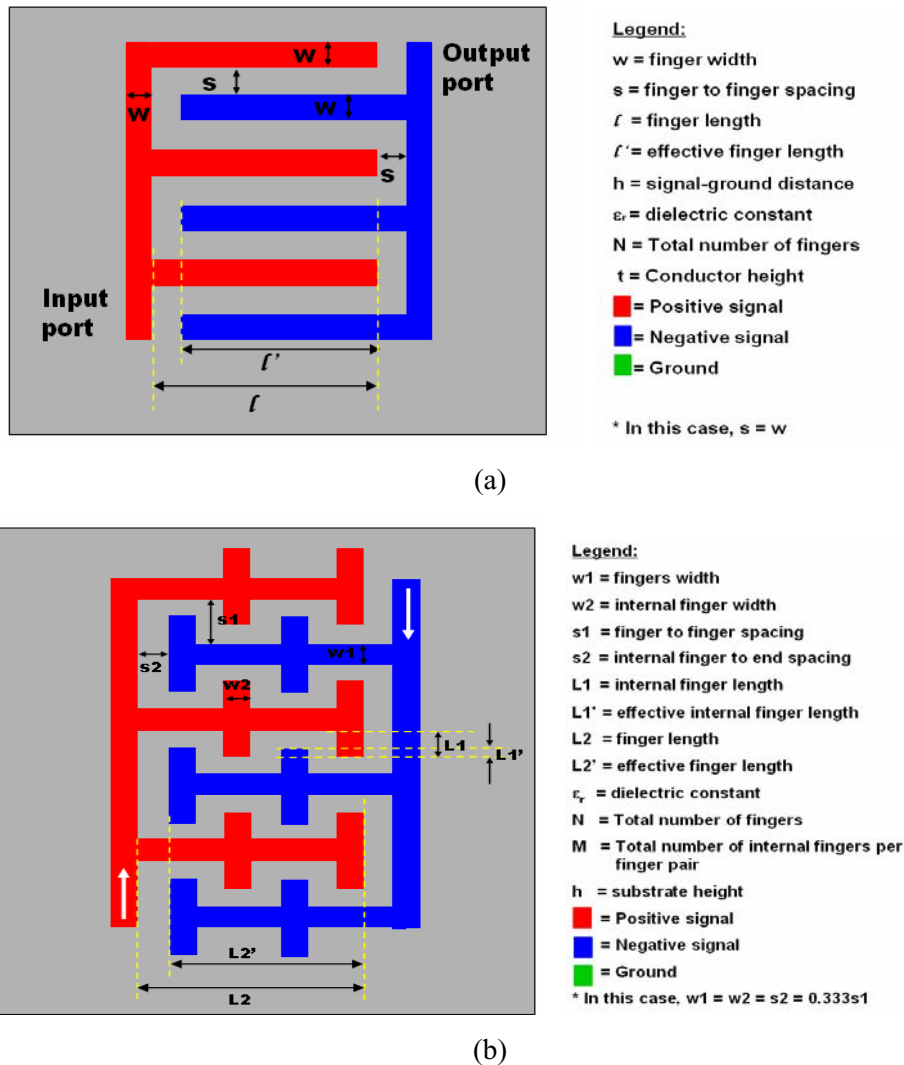


Figure 1.2: IDC configurations (a) basic, (b) six fingers.

## 1.4 Scope of Project

The project is focused on developing an interdigital capacitor configuration that will exhibit a high capacitance density as well as high Q-factor. The scope of the project covers the following areas:

- **Study of the theory and fundamentals of RF interdigital capacitor.**

This includes basic design of lumped elements, basic capacitor theories, parameters that affect capacitor performance, parameters that used for capacitor performance evaluation, electrical representation of capacitors, interdigital capacitor design and performance improvement techniques.
  
- **Modification of the conventional interdigital configuration with combline structure for performance improvement.**

Based on the theories and work done by other researchers, the study further explore and investigate the possibility of improving the interdigital capacitor performance by varying different layout options with combline structure.
  
- **Electromagnetic simulations.**

Simulations of the conventional and modified interdigital configurations were performed using Ansoft HFSS electromagnetic simulation software.
  
- **Analysis of the results.**

Performance comparison of the modified and conventional configuration interdigital capacitor in terms of Q factor and capacitance density.

## **1.5 Outline of Thesis**

Chapter one discusses the objectives and scope of the project and gives a general introduction to RFICs and functions of on chip capacitors in RFIC. This chapter also clearly discusses the motivation behind the study and the limitations in order to achieve the project objectives.

In Chapter two, relevant literature and previous work regarding planar interdigital capacitor characterization are reviewed. This chapter also elaborates on the principles of capacitor and the factors that must be taken into consideration to obtain a good capacitor for RFIC usage.

The design and analysis approach used in this project are elaborated in Chapter three. The overall activities of this study are discussed in this chapter. Besides, this chapter also discusses in detail the capacitor modification flow of the proposed interdigital capacitor with combline structure and simulation flow of the designed capacitors using Ansoft HFSS simulation software.

In Chapter four, the final results are presented and analyzed in detail. This includes the modifications from the basic configuration to various combline configurations.

The final chapter concludes the thesis. Suggestions for further improvement are also presented.



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