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Performance Analysis of Cross-Connected Sources Multilevel Inverter (CCSMLI) based on NLM and SHE Switching Schemes

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Abstract: A power inverter is an important device in present technologies since the usage of renewable energy sources has increased rapidly throughout the world. The main focus of research in the power inverter field is to produce a high-efficiency power inverter to maximize the energy harvested from renewable energy sources. In a power inverter, selecting an appropriate switching scheme is imperative. In this paper, two different switching schemes, namely the Nearest Level Modulation (NLM) and the Selective Harmonics Elimination (SHE) are implemented on the Cross-Connected Sources Multilevel Inverter (CCSMLI) circuit. The switching schemes are implemented on 11 and 13-level CCSMLI circuits with two types of loads (R load and RL load). The simulation results show that when applied to CCSMLI, both switching techniques' output voltage THD performances are comparable, but the NLM is paramount for high-level MLI topologies due to its simplicity.

Keywords: Cross-Connected Sources Multilevel Inverter, Nearest Level Modulation, Selective Harmonics Elimination, Total Harmonics Distortion.

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1. INTRODUCTION

The demand for renewable energy sources in power generation has shown an increasing trend in recent years due to the growing problem of global warming. The power conversion of these sources from direct current (DC) to alternating current (AC) requires an inverter circuit. Solar and wind energy are examples of renewable energy sources extensively used for this purpose.

Over the past few years, Multilevel Inverters (MLI) have been a center of attraction as they possess various advantages over conventional inverters. Some advantages are high power quality, high voltage capability, low switching losses, and low electromagnetic interference (EMI). These devices are widely used in induction motor drives, renewable energy applications, and medium and high voltage applications [1].

In general, MLIs are built using several DC sources and switching devices. Based on the magnitude of DC sources, the multilevel inverters can be divided into two types, which are symmetrical and asymmetrical. The symmetrical type uses DC sources with equal magnitude, while an asymmetrical type uses DC sources with different magnitudes [2]. The advantage of asymmetrical over the symmetrical configuration is that the output level generation will be higher. However, the voltage and current stress across the switches are not equal, leading to reliability issues.

The switching techniques can be classified into low switching frequency (LSF) and high switching frequency (HSF). These switching techniques play a crucial part in the inverter since they are directly related to the overall efficiency of the entire system. LSF offers many advantages over HSF, such as lower switching losses [3], reduced switching stress, lower cooling requirements, lower operating cost, better efficiency, and many more [1]. Hence, it is more favorable to operate the MLIs under LSF switching techniques such as Nearest Level Modulation (NLM), Selective Harmonics Elimination (SHE), and Space Vector Control (SVC) [1] – [3].

This paper presents a comparative analysis of two different switching techniques, namely the NLM and the SHE. The analysis will be mainly on the voltage output THD. Both techniques will be applied to control the switching of a reduced component MLI topology, namely the Cross-Connected Source MLI (CCSMLI). The model will be developed through the Matlab-Simulink software, and several simulation tests will be carried out. Performance analysis will be conducted on the output voltage THD parameter.

2. CONVENTIONAL MULTILEVEL INVERTER TOPOLOGIES

The multilevel inverter was introduced in 1975 by Baker and Banister [4], where at its initial development, the multi-step output voltage was produced from several DC sources. Later, a new topology called Neutral Point Clamped (NPC) was developed by Nabae et al. in 1981 [4]. In 1992, Flying Capacitor (FC) topology was developed by Meynard and Fosch [4][5]. Peng and Lai also contributed to the development of MLI topologies by developing the Cascaded H-Bridge (CHB) topology [4]. Table 1 shows the summary for the conventional MLI. The details of each topology are presented in the following sub-sections.

Table 1. Conventional multilevel inverter topologies summary

MLI topology	NPC	FC	CHB
No. of DC sources	1	1	$\frac{m-1}{2}$
DC link capacitor	$m-1$	$m-1$	-
No. of switches	$2(m-1)$	$2(m-1)$	$\frac{4(m-1)}{2}$
Clamping capacitor	-	$\frac{(m-1)(m-2)}{2}$	-
Clamping diodes	$(m-1)$ $\times(m-2)$	-	-

2.1 Neutral Point Clamped

A 3-level Neutral Point Clamped Multilevel Inverter (NPC-MLI) topology is illustrated in Figure 1. The 3-level output voltage generated by this topology is 0.5Vdc, 0, and –0.5Vdc. Switching on the T1 and T2 will generate output voltage with positive polarity, while switching on T3 and T4 will generate output voltage with negative polarity. Switch T2 and T3 must be turned on to generate zero output voltage.

This NPC-MLI topology has advantages, such as only one DC source is required to generate any desired output voltage level, 3-level and 5-level structures have simple control logic, are highly reliable, and work more efficiently under fundamental switching frequency [4]. However, lack of modularity, a high number of clamping diodes, unbalanced power distribution [6], and uneven voltage balancing [7] are some drawbacks of this topology.

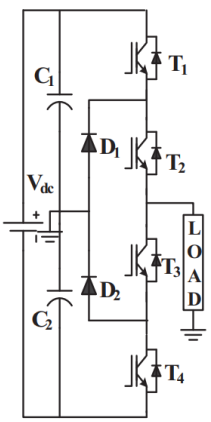


Figure 1. Three-level NPC-MLI topology

2.2 Flying Capacitor

The Flying Capacitor Multilevel Inverter (FC-MLI) topology has an identical structure and working principle to the NPC-MLI topology. A little bit different in its structure is that the clamping diodes are now replaced with floating capacitors. Meanwhile, its working principle is different in generating zero output voltage. The FC-MLI topology has two options for generating the zero output voltage: turning on T1 and T3 switches or T2 and T4 switches. Figure 2 shows the 3-level FC-MLI topology, which generates 3-level output voltage (0.5Vdc, 0, and –0.5Vdc).

Some of the advantages listed in [4] for this topology are that it is more flexible in synthesizing voltage as compared to NPC-MLI, uneven voltage balancing problems can be eliminated by properly selecting the switching combination for structure with more than 5-level output voltage and active power as well as reactive power can be controlled. Despite its advantages, this topology also has certain limitations, such as a higher number of switching devices and capacitors are required when the number of output voltage levels increases [6][7]. Besides that, the capacitors' charges needed to be balanced at a low switching frequency [6].

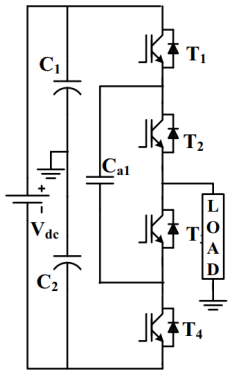


Figure 2. Three-level FC-MLI topology

2.3 Cascaded H-Bridge

Cascaded H-Bridge Multilevel Inverter (CHB-MLI) topology to generate a 3-level output voltage, which are Vdc, 0, and –Vdc is shown in Figure 3 below. The topology generated output voltage with positive polarity when T1 and T4 switches are turned on. On the other hand, output voltage with negative polarity can be generated by turning on T2 and T3 switches. Meanwhile, turning on either T1 and T3 switches or T2 and T4 switches will generate zero output voltage.

When compared with previously discussed topologies, NPC-MLI and FC-MLI, this CHB-MLI topology requires lesser components since no clamping diodes and clamping capacitors are utilized by this topology [4]. As a result, the uneven voltage balancing problem caused by the existence of capacitors does not occur in this topology [4]. Nevertheless, this topology also gives a higher degree of freedom, multiple switching state redundancy, and increases the effectiveness of the power and voltage capability, as listed in [8]. Moreover, it has a modular

structure and can implement simple control [7].

Similar to other topologies, CHB-MLI also possesses several limitations. Every module of H-Bridge required a separate DC source, resulting in a higher cost to develop this topology [6]. Another drawback is that low-frequency transformers are usually utilized to generate the desired output voltage level [4], reducing overall efficiency.

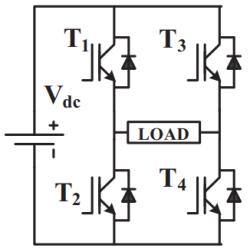


Figure 3. Three-level CHB-MLI topology

3. CROSS – CONNECTED SOURCES MULTILEVEL INVERTER TOPOLOGY

This section explains the working principle of the Cross-Connected Sources Multilevel Inverter (CCSMLI) topology operating under a symmetrical configuration. Figure 4 shows the circuit diagram for the CCSMLI topology, which utilizes three DC sources and eight switches. The sources are connected to allow the addition of the voltages from different sources [1] to generate the desired output voltage level. All DC sources are cross-connected through the switching devices in such a way that the lower potential terminal of the preceding source is connected to the higher potential terminal of the succeeding source and vice versa [2].

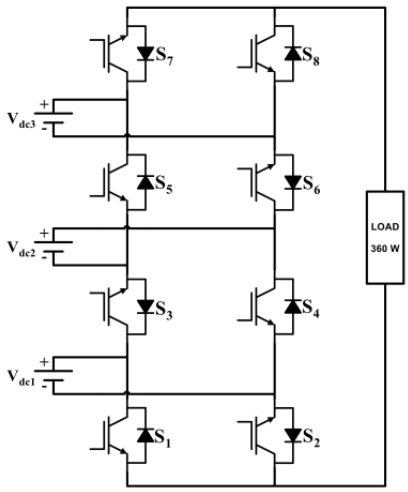


Figure 4. CCSMLI topology

In this CCSMLI topology, the switching stress is equally distributed between the switches with the help of a balanced switching approach. Table 2 shows the switching patterns for the 13-level CCSMLI topology. The table shows that different switches' status enables balanced switching stress for a respective level in the positive and negative cycle [1]. Operating the S1, S4, S5, S8, S9, S12, and S13 switches will add the voltage of DC sources and result in positive polarity in output voltage, whereas operating the other four switches (S2, S3, S6, S7, S10, S11, and S14) will also add the voltage of DC sources but resulting in negative polarity in output voltage.

The CCSMLI topology with symmetrical configuration can be extended to any desired level by following the below equations [2][9]. Since the symmetrical configuration is being utilized in this topology, the value for each DC source can be denoted by Equation (1),

$$V_{dc,j} = V_{dc}\ for\ j = 1,2,3,\ldots \quad (1)$$

where j is the number of DC sources.

Table 2. Switching pattern for 13-level CCSMLI topology

Level	Switch													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
0		■		■		■		■		■		■		■
Vdc		■	■		■		■		■		■		■	
2Vdc		■	■			■		■		■		■		■
3Vdc		■	■			■	■		■		■		■	
4Vdc		■	■			■	■			■		■		■
5Vdc		■	■			■	■			■	■		■	
6Vdc		■	■			■	■			■	■			■
5Vdc		■	■			■	■			■	■		■	
4Vdc		■	■			■	■			■		■	■	■
3Vdc		■	■			■	■		■		■		■	
2Vdc		■	■			■		■		■		■		■
Vdc		■		■	■		■		■		■		■	
0		■		■		■		■		■		■		■
0	■		■		■		■		■		■		■	
-Vdc	■			■		■		■		■		■		■
-2Vdc	■			■	■		■		■		■		■	
-3Vdc	■			■	■			■		■		■		■
-4Vdc	■			■	■			■	■		■		■	
-5Vdc	■			■	■			■	■			■		■
-6Vdc	■			■	■			■	■			■	■	
-5Vdc	■			■	■			■	■			■		■
-4Vdc	■			■	■			■		■		■	■	
-3Vdc	■			■	■			■	■		■		■	
-2Vdc	■			■	■		■		■		■		■	
-Vdc	■			■		■		■		■		■		■
0	■		■		■		■		■		■		■	

ON OFF

The total number of DC sources and the number of switches needed to generate N-level output voltage is given by Equation (2) and Equation (3), respectively.

$$N_{dc} = 0.5\ (N_{level} - 1) \quad (2)$$

$$N_{switch} = 2\ (N_{dc} + 1) \quad (3)$$

Hence, the maximum voltage can be obtained by summing all the voltage of DC sources as given by Equation (4).

$$V_{max} = V_1 + V_2 + V_3 + \ldots + V_j \quad (4)$$

By utilizing the mathematical expressions above, the

CCSMLI topology with any level can be developed by adding or removing DC sources and switches.

4. LOW SWITCHING FREQUENCY TECHNIQUES

The Low switching frequency (LSF) offers many advantages over the high switching frequency (HSF) techniques. The apparent benefit is low switching frequency losses. In this section, the fundamental of two LSF techniques, the NLM and the SHE, will be briefly described.

4.1 Nearest Level Modulation

The Nearest Level Modulation (NLM) switching technique has gained tremendous attention due to its advantages. The major advantage is that the switching angles can be calculated using a simple mathematical equation [3]. Besides that, it also offers a lower Total Harmonic Distortion (THD) value since the produced waveform follows the sinusoidal nature of AC waveforms [1]. The graphical representation of NLM can be seen in Figure 5.

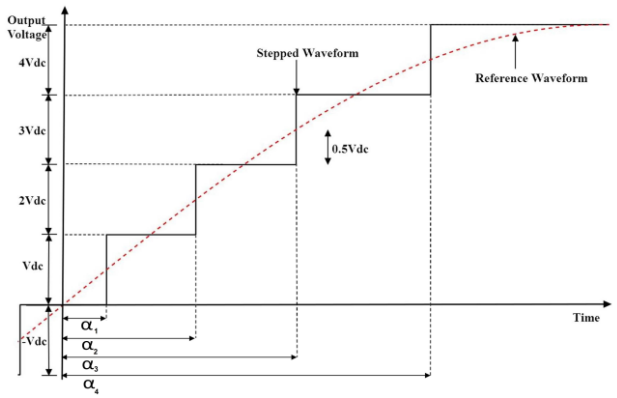


Figure 5. NLM switching technique [2]

Figure 5 above shows that this NLM switching technique helps generate a stepped waveform that synchronizes with the reference sine waveform [2]. At every switching angle, the sine wave will cut the rising edge of the stepped waveform exactly at half its magnitude [1] – [3]. The nearest voltage level is selected by comparing the reference sine waveform with the output voltage level [4]. The switching angle for NLM can be calculated using Equation (5), while the value of THD can be determined using Equation (6) [1] – [3],

$$\alpha_i = \sin^{-1}\left(\frac{i-0.5}{n}\right) \; for \; i = 1, 2, 3, \ldots, n \tag{5}$$

$$THD = \frac{\sqrt{\frac{\pi^2 n^2}{8} - \frac{\pi}{4}\sum_{i=0}^{n-1}(2i+1)\alpha_{i+1} - (\sum_{i=1}^{n}\cos(\alpha_i))^2}}{\sum_{i=1}^{n}\cos(\alpha_i)} \tag{6}$$

Where n is the number of the desired output voltage levels, and i is the number of angles.

4.2 Selective Harmonics Elimination

Selective Harmonics Elimination (SHE) switching technique works on the same frequency as the NLM, i.e., low switching frequency (LSF). It helps in reducing the unwanted odd harmonics relying on the number of pulses in the output voltage waveform. The undesired odd harmonics can be completely removed from the output voltage waveform by determining the placements and duration of the notches' switching angles. The SHE is a mathematical approach for removing lower-order odd harmonics such as the 3rd, 5th, 7th, etc. from the output voltage waveform [10]. Because lower-order harmonics contribute to a larger proportion of total harmonics, eliminating them is a great idea. Consequently, there will be an increase in higher-order harmonics [2] [11].

One needs to solve a group of nonlinear transcendental equations to obtain the most suitable switching angles for eliminating the lower-order odd harmonics. This is considered the main challenge in utilizing SHE switching techniques [4] [12], and choosing the appropriate numerical method is very helpful in solving these equations. This paper uses the Newton-Raphson method to solve the equations. The transcendental equations for the 13-level inverter are given in Equation (7).

$$\begin{aligned}
&\cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_6) = 6M \\
&\cos(3\alpha_1) + \cos(3\alpha_2) + \cdots + \cos(3\alpha_6) = 0 \\
&\cos(5\alpha_1) + \cos(5\alpha_2) + \cdots + \cos(5\alpha_6) = 0 \\
&\cos(7\alpha_1) + \cos(7\alpha_2) + \cdots + \cos(7\alpha_6) = 0 \\
&\cos(9\alpha_1) + \cos(9\alpha_2) + \cdots + \cos(9\alpha_6) = 0 \\
&\cos(11\alpha_1) + \cos(11\alpha_2) + \cdots + \cos(11\alpha_6) = 0
\end{aligned} \tag{7}$$

Where M is the modulation index with values ranging from 0 to 1, these equations are then written in matrices. The switching angles matrix and the harmonic amplitude matrix are shown in Equation (8) and Equation (9), respectively.

$$\alpha^j = \left[\alpha_1^j \;\; \alpha_2^j \;\; \alpha_3^j \;\; \alpha_4^j \;\; \alpha_5^j \;\; \alpha_6^j\right]^T \tag{8}$$

$$T = [6M \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 0]^T \tag{9}$$

The nonlinear system matrices are given below in Equation (10) and Equation (11).

$$F(\alpha) = \begin{bmatrix} \cos(\alpha_1) & \cdots & \cos(\alpha_6) \\ \vdots & \ddots & \vdots \\ \cos(11\alpha_1) & \cdots & \cos(11\alpha_6) \end{bmatrix} \tag{10}$$

$$\left[\frac{\partial F}{\partial \alpha}\right]^j = -\begin{bmatrix} \sin(\alpha_1^j) & \cdots & \sin(\alpha_6^j) \\ \vdots & \ddots & \vdots \\ \sin(11\alpha_1^j) & \cdots & \sin(11\alpha_6^j) \end{bmatrix} \tag{11}$$

In general, Equation (7) can be written as:

$$F(\alpha) = T \tag{12}$$

By using Equation (8) to Equation (12), the Newton Raphson method can be done in the following steps [13] [14].

- Guess the initial value of α^j for j = 0;

$$\alpha^0 = [\alpha_1^0 \ \alpha_2^0 \ \alpha_3^0 \ \alpha_4^0 \ \alpha_5^0 \ \alpha_6^0]^T \quad (13)$$

- Calculate the value of F^0 using the assumption value of α^0;

$$F^0 = F(\alpha^0) \quad (14)$$

- Linearize Equation (10) about α^0;

$$F^0 + \left[\frac{\partial F}{\partial \alpha}\right]^0 \times d\alpha^0 = T \quad (15)$$

where,

$$d\alpha^0 = [d\alpha_1^0 \ d\alpha_2^0 \ d\alpha_3^0 \ d\alpha_4^0 \ d\alpha_5^0 \ d\alpha_6^0]^T \quad (16)$$

- Solve for $d\alpha^0$;

$$d\alpha^0 = INV \left[\frac{\partial F}{\partial \alpha}\right]^0 (T - F^0) \quad (17)$$

- Update the initial value of α;
-

$$\alpha^{j+1} = \alpha^j + d\alpha^j \quad (18)$$

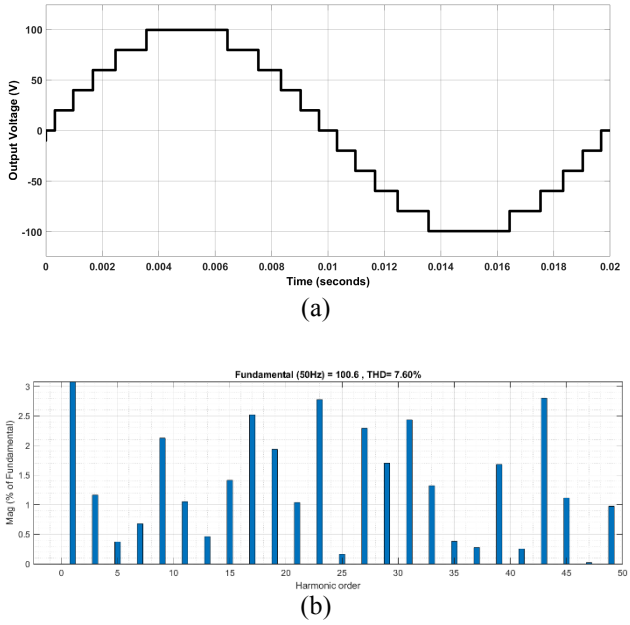
- Repeat the process until $d\alpha^j$ satisfies the desired degree of accuracy, and the solutions obtained to satisfy the following condition;

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \frac{\pi}{2} \quad (19)$$

5. RESULTS AND DISCUSSIONS

This section presents the simulation results for Cross-Connected Sources Multilevel Inverter (CCSMLI) of two levels, 11-level and 13-level are presented. The circuits were simulated with MATLAB/Simulink R2021a package. The CCSMLIs were operated to generate a fundamental voltage of 100V and 120V, respectively, at the frequency of 50Hz. The purely resistive load was rated at 100 ohms, while the resistive-inductive load was rated at 100 ohms and 50 mH. Two low switching frequency (LSF) switching techniques, as discussed in section 4, which are Nearest Level Modulation (NLM) and Selective Harmonics Elimination (SHE), were implemented in the simulation to compare the performance of the CCSMLI.

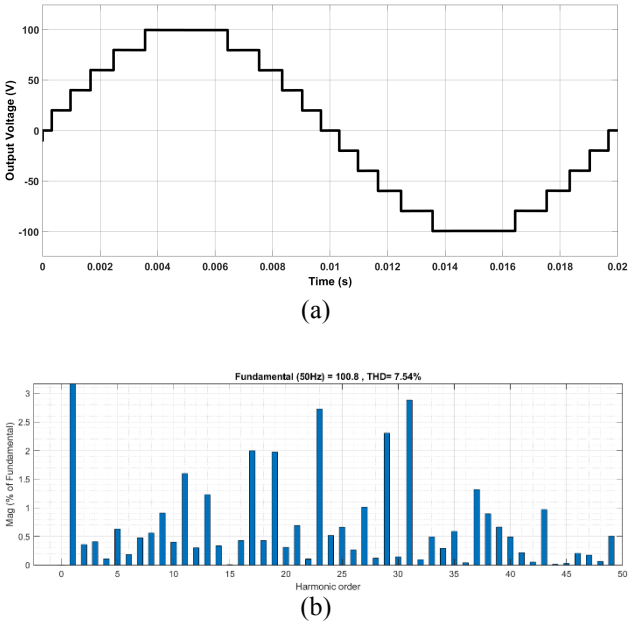
Figure 6 and Figure 7 show the simulation results for 11-level CCSMLI for R load and RL load, respectively, when operated with NLM switching technique. It was observed that the CCSMLI generated an 11-level output voltage with a fundamental voltage equal to 100.6V and 100.8V, respectively, for R load and RL load. Regarding voltage THD, the R load generated 7.60% while the RL load generated 7.54%.



(a)

(b)

Figure 6. Simulation results for 11-level CCSMLI with R load using NLM (a) Output voltage waveform (b) Voltage THD

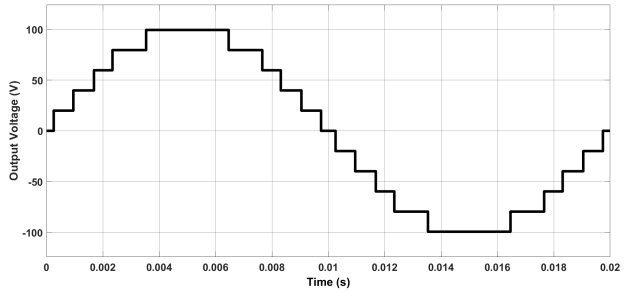


(a)

(b)

Figure 7. Simulation results for 11-level CCSMLI with RL load using NLM (a) Output voltage waveform (b) Voltage THD

When the 11-level CCSMLI circuit is simulated with the SHE switching technique for both R load and RL load, the results are as shown in Figure 8 and Figure 9, respectively. The circuit with R load produced 100.5V fundamental voltage with voltage THD of 7.85%. On the other hand, the circuit with RL load generated 101.1V fundamental voltage with voltage THD of 7.73%.



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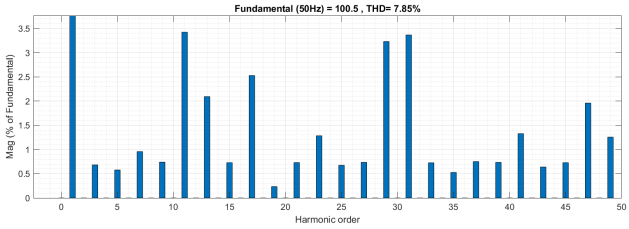
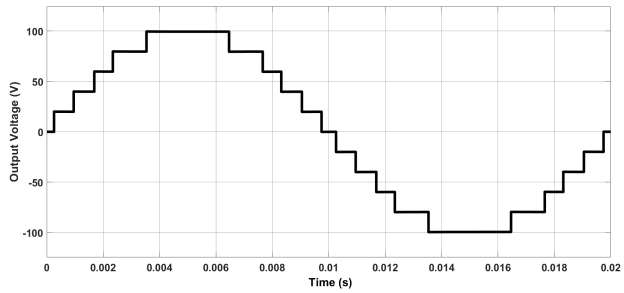


(b)

Figure 8. Simulation results for 11-level CCSMLI with R load using SHE (m=0.8001) (a) Output voltage waveform (b) Voltage THD



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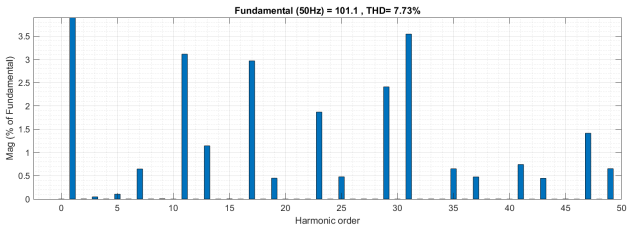
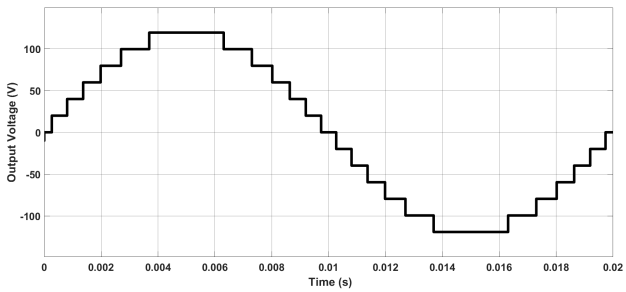


(b)

Figure 9. Simulation results for 11-level CCSMLI with RL load using SHE (m=0.8001) (a) Output voltage waveform (b) Voltage THD

As for the simulation of the 13-level CCSMLI circuit, similar procedures were repeated as in the simulation of the 11-level CCSMLI circuit. The simulation results for this circuit with R load, when implemented with the NLM switching technique, are given in Figure 10. From this figure, it can be seen that the fundamental voltage and voltage THD produced were 119.7V and 6.43%, respectively. Meanwhile, Figure 11 illustrates the simulation results for the circuit with RL load for a similar switching technique. The fundamental voltage obtained from the simulation was 120.2V with 6.39% voltage THD.



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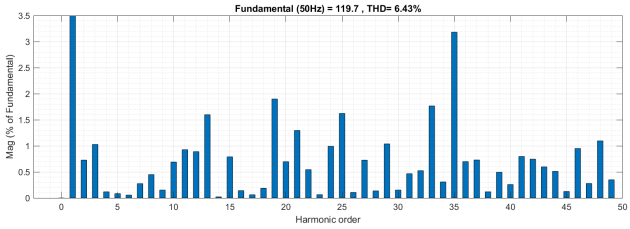
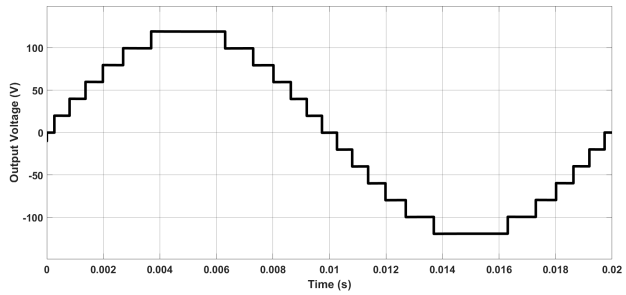


(b)

Figure 10. Simulation results for 13-level CCSMLI with R load using NLM (a) Output voltage waveform (b) Voltage THD



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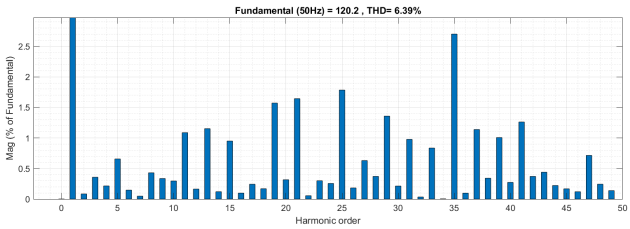
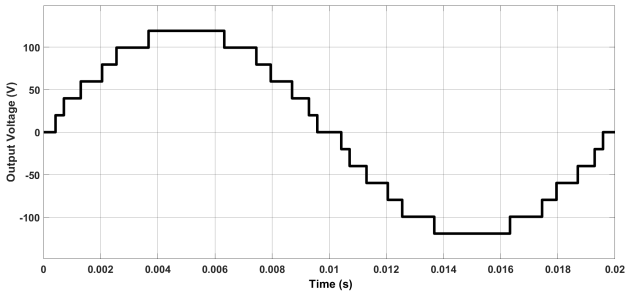


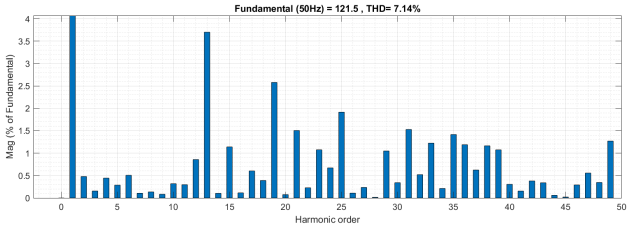
(b)

Figure 11. Simulation results for 13-level CCSMLI with RL load using NLM (a) Output voltage waveform (b) Voltage THD

For SHE switching technique implemented on 13-level CCSMLI circuit, the results obtained from the simulations of both R load and RL load are presented in Figure 12 and Figure 13 respectively. From these two figures, the fundamental voltage produced were 121.5V and 120.9V respectively for the circuit with R load and RL load. As for the voltage THD, the two circuits produced 7.14% and 7.04% respectively.

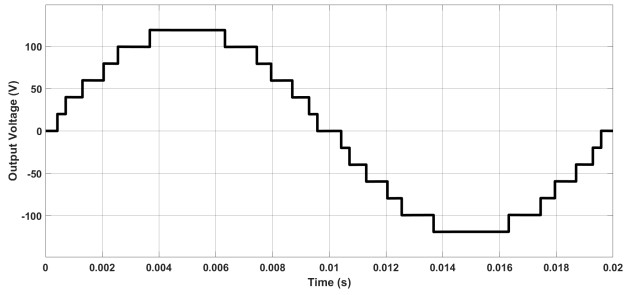


(a)

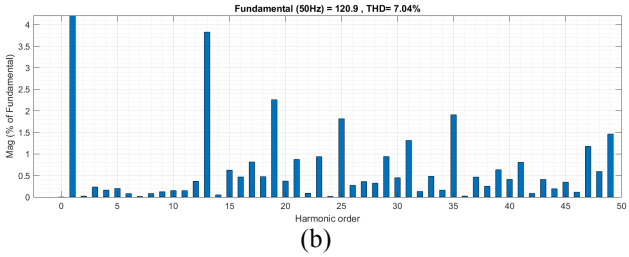


(b)

Figure 12. Simulation results for 13-level CCSMLI with R load using SHE (m=0.7972) (a) Output voltage waveform (b) Voltage THD



(a)



(b)

Figure 13. Simulation results for 13-level CCSMLI with RL load using SHE (m=0.7972) (a) Output voltage waveform (b) Voltage THD

Table 3 summarizes all the simulation results for different output voltage levels, different load types, and different switching techniques used.

From Table 3, it can be seen that the 13-level CCSMLI circuit give better THD results than the 11-level CCSMLI circuit. This is because the output voltage waveforms obtained from this circuit resembled the shape of the sine waveform. Regarding load type, the circuit with RL load had lower voltage THD than the circuit with R load. However, this type of load produced a higher fundamental voltage. Besides that, it can be summarized that the voltage THD obtained when using NLM switching technique was improved significantly instead of when using the SHE switching technique. As for the fundamental voltage, it was impossible to obtain the exact voltage as desired. All fundamental voltages differed in the range of -0.3V to +1.5V. The best result was obtained when a 13-level CCSMLI circuit with RL load was implemented with NLM switching technique since it gave the lowest voltage THD (6.39%) and the nearest fundamental voltage (120.2V).

Table 3. Summary of all simulation results

Circuit	Load type	Switching technique used	Fundamental voltage (V)	Voltage THD (%)
11-level CCSMLI	R load	NLM	100.6	7.60
		SHE	100.5	7.85
	RL load	NLM	100.8	7.54
		SHE	101.1	7.73
13-level CCSMLI	R load	NLM	119.7	6.43
		SHE	121.5	7.14
	RL load	NLM	120.2	6.39
		SHE	120.9	7.04

6. CONCLUSION

In this paper, two low switching frequency (LSF) switching techniques, namely the nearest level modulation (NLM) and the selective harmonics elimination (SHE) are simulated for a cross-connected sources multilevel inverter (CCSMLI) topology. The CCSMLI topology is designed to operate under a symmetrical configuration and generate a voltage output of eleven and thirteen levels. The simulation is carried out using MATLAB/Simulink R2021a software. It can be concluded that both switching techniques produce comparable voltage THD performance. However, the NLM design is easier than the SHE. The NLM should be the most suitable candidate for the switching technique for high-level MLI.

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