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An improved seven-level switched-capacitor-based neutral-point clamped inverter

Saifullah Kakar[1], M. Saad Bin Arif[1,2]*, Shahrin Md. Ayob[1]*, Norjulia B. M. Nordin[1], Saad Mekhilef[3,4,5], Mehdi Seyedmahmoudian[3] and Alex Stojcevski[3]

[1]School of Electrical Engineering, Faculty of Engineering, Universiti Teknologi Malaysia, Johor Bahru, Malaysia, [2]Department of Electrical Engineering, Faculty of Engineering and Technology, Aligarh Muslim University, Aligarh, India, [3]School of Software and Electrical Engineering, Swinburne University of Technology, Melbourne, VIC, Australia, [4]Center of Research Excellence in Renewable Energy and Power Systems, King Abdulaziz University, Jeddah, Saudi Arabia, [5]Department of Electrical Engineering, College of Engineering, Universiti Tenaga Nasional, Kajang, Malaysia

Multilevel inverters (MLIs) have seen significant growth in a variety of medium- to high-power industrial applications and have become a mature and viable solution for renewable energy systems over the past decade. The major concerns of MLIs are the high component count and the buck-type feature of the ac output voltage when used for grid-connected renewable-energy-based sources such as solar photovoltaic (PV) panels. As another option, a switched-capacitor (SC)-based inverter possessing the feature of boost ability is a prime solution to meet the requirements of ac power applications. Integrating an SC network with a neutral-point clamped (NPC) structure makes leakage current alleviation viable for transformerless PV grid-connected systems. In this article, an improved SCMLI based on the NPC structure is proposed to reduce the number of active switches and the number of switches in the charging loop, significantly reducing the power loss. It can generate seven voltage levels with voltage boosting and self-balancing of capacitors within a single-stage power conversion. The working principle of the proposed topology, circuit description, and control technique are presented. Further, the proposed inverter was compared with other recent SC topologies to show its superiority. In the end, a laboratory prototype was developed and tested for the seven-level module under steady-state and dynamic conditions to validate the practical viability of the proposed configuration. The proposed inverter's maximum efficiency was 97.5% at 1.2 kW rated power.

Introduction

Multilevel inverters (MLIs) have attracted increasing attention in renewable energy generation systems over the past decade (Iqbal et al., 2020). Among all renewable energy sources, the use of photovoltaic (PV) systems in power generation has regularly increased worldwide. MLIs play a vital role in power conversion suitable for different applications owing to their promising features such as high efficiency and power density. In contrast to the classical two-level inverter, their main features are higher modularity and scalability, excellent output waveform quality, appropriate power density, and suitable cost (Kakar et al., 2021a; Kakar et al., 2021b; Iqbal et al., 2021). However, the major concerns of MLIs are the high component count and the buck-type feature of the ac output voltage when used for grid-connected renewable energy-based sources such as solar PV panels. Therefore, a separate boost dc–dc converter or transformer is imperative to boost the input dc voltage to an acceptable range, increasing the systems' size, cost, weight, and losses.

Therefore, the switched-capacitor (SC) concept integrated into MLIs is an effective solution to boost the low input voltage obtained from renewable energy sources such as PV and fuel cells with multistepped voltage levels. The concept of a SC inverter was introduced first by Mak and Ioinovici in 1998 (Hussan et al., 2021). In general, SC-based MLIs require a single dc source and capacitors in place of dc sources and take advantage of the series–parallel technique to boost the low input voltage near the sinusoidal output voltage waveform. SCMLI is one of the popular MLI structures that can inherently balance the capacitor voltage and boost the input voltage simultaneously. Therefore, the need for sensors, complex control techniques, and auxiliary circuits for balancing the capacitor voltage is completely avoided. However, SCMLIs require a large number of power switches and capacitors with high voltage stress. Thus, the overall system becomes complex and costly, and efficiency is reduced when high voltage levels are required. Therefore, several SCMLI topologies have been introduced over the years to reduce the number of circuit components (Taghvaie et al., 2017; Ali and Krishnasamy, 2018; Peng et al., 2019; Roy et al., 2019; Saeedian et al., 2019; Khan et al., 2020; Roy and Sadhu, 2020; Chen et al., 2021; Lin et al., 2021; Roy et al., 2021). However, these topologies share a common drawback of high common-mode voltage (CMV) that induces leakage risk, making these topologies less viable for transformerless PV grid-tied systems. An alternative solution is to employ neutral-point clamped (NPC) inverters that maintain the CMV constant; thus, mitigating the leakage current to an acceptable range. In addition, power quality increases by enhancing the number of output voltage levels. In this category, inverter structures like active neutral-point clamped (ANPC) (Wang et al., 2017), T-type (Saeedifard et al., 2011), and flying capacitor (FC)-based (Siwakoti et al., 2019a) are the most developed and efficient topologies. In addition, other two of

the main issues involving the ANPC and NPC topologies discussed above are the lack of voltage-boosting capability and the capacitor's voltage unbalancing.

On this line, several attempts have been made in literature by integrating SCs into an NPC structure to achieve voltage boosting, which successfully solved the voltage unbalancing and boosting issues in ANPC topologies and the CMV in other topologies discussed above. In recent years, two 5-level boost T-type ANPC inverters were developed by Rech (2019) and Siwakoti et al. (2019b) to generate voltage levels of 0, $\pm0.5\ V_{in}$, and $\pm1\ V_{in}$. The one by Rech (2019) had a similar structural layout to the classical five-level ANPC, but both switches (S_5 and S_6) were connected in reverse. Because of this, the capacitor implemented in this topology was actually an SC rather than a FC. The second topology by Siwakoti et al. (2019b) was also constructed on the SC concept, and two switches were less used than the first one. However, their main drawback was that two switches (S_3 and S_6) in each topology needed to block a bipolar voltage so that active and reactive powers could not conduct through them simultaneously for some levels. Hence, a special control strategy was necessary for nonunity power factor (FP) operation, as analyzed by Siwakoti et al. (2019b). In addition, the switch count was high in these topologies for the five-level inverter. To resolve the drawbacks of the topologies in the study by Rech (2019) and Siwakoti et al. (2019b), Ye et al. (2021) developed a new five-level inverter by inserting an SC unit into the classical three-level NPC inverter phase leg. The SC unit comprised two SCs and one bidirectional switch. However, it had no boost capability. The topology presented by Lee et al. (2019a) could produce up to seven voltage levels, with a gain factor of 1.5.

To further improve voltage boosting, a dual T-type seven-level topology (Lee and Lee, 2019) was attempted. The achieved boosting gain of this topology was 1.5 at the cost of incorporating more power switches and floating capacitors. Another topology (Lee et al., 2019b) preserved the two advantages of the high voltage-boosting gain of 1.5 and the seven voltage level generation in the study by Lee and Lee (2019) while achieving low switch count and guaranteeing low voltage stress on the switching devices. The topology by Sathik et al. (2019) was developed with the intent to reduce the voltage stress on switches and the number of capacitors while offering the same benefits of 1.5 boosting gain. Another attempt was made by Sandeep et al. (2020) to improve the topology presented by Lee and Lee (2019) in terms of switch count and voltage stress reduction. Similar features could also be noticed from the seven-level SC topology by Zeng et al. (2019). The inverter by Siwakoti (2018) was a first attempt that enhanced the boosting gain to unity. Inspired by the ANPC topology presented by Siwakoti (2018), two new enhanced ANPC topologies were derived by Lee et al. (2019c), where a higher voltage gain and switch reduction were achieved.
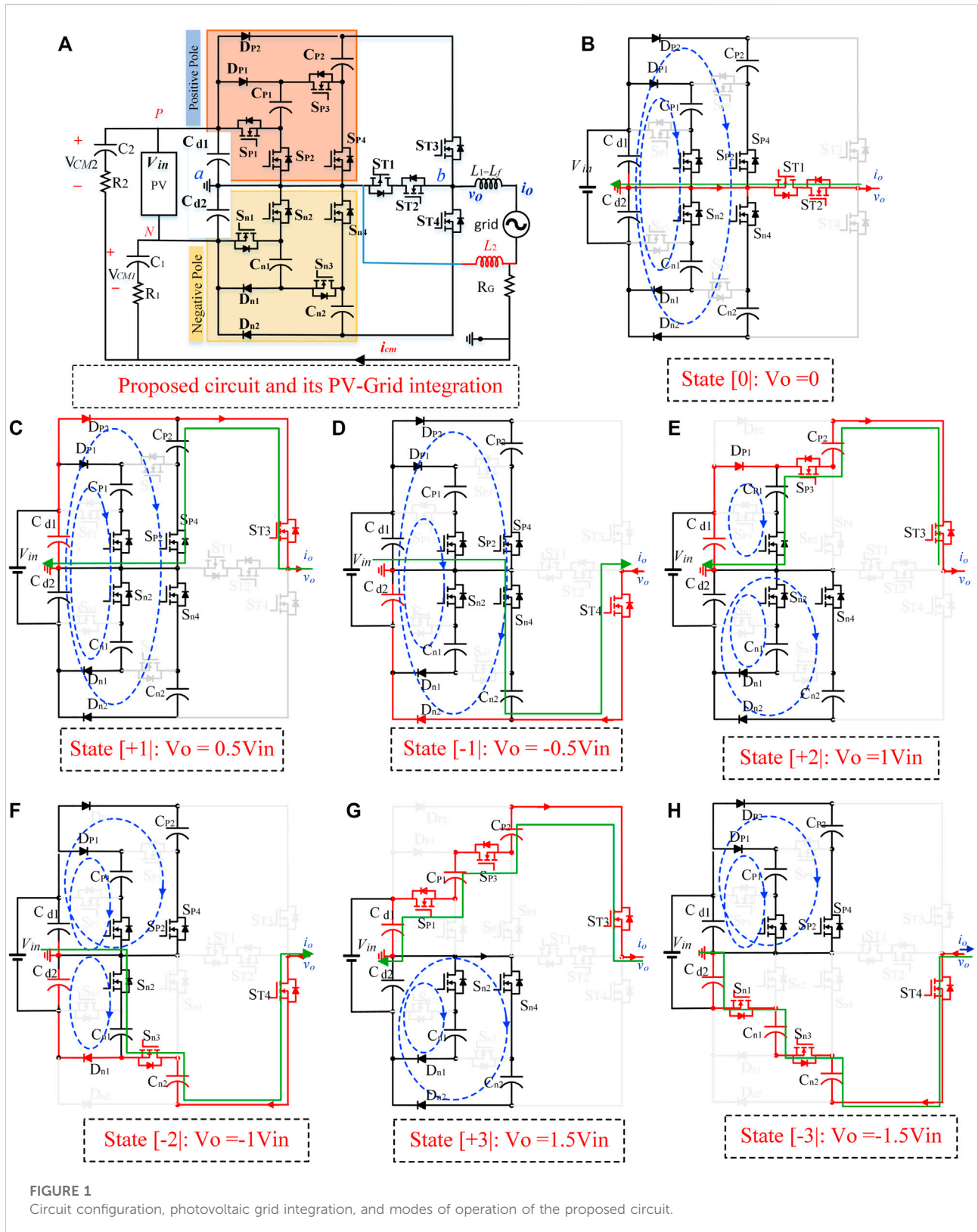
FIGURE 1
Circuit configuration, photovoltaic grid integration, and modes of operation of the proposed circuit.

TABLE 1 Switching states for the proposed seven-level inverter.

State	Voltage levels	On-state switches	Capacitors			
			C_{p1}	C_{p2}	C_{n1}	C_{n2}
[+1]	$0.5V_{in}$	S_{p2}, S_{p4}, S_{n2}, S_{n4}, S_{T3}	C	C	C	C
[+2]	$1V_{in}$	S_{p2}, S_{p3}, S_{n2}, S_{n4}, S_{T3}	D	C	C	C
[+3]	$1.5V_{in}$	S_{p1}, S_{p3}, S_{n2}, S_{n4}, S_{T3}	D	D	C	C
[0]	$0V_{in}$	S_{p2}, S_{p4}, S_{n2}, S_{n4}, S_{T1}, S_{T2}	C	C	C	C
[-1]	$-0.5V_{in}$	S_{p2}, S_{p4}, S_{n2}, S_{n4}, S_{T4}	C	C	C	C
[-2]	$-1V_{in}$	S_{p2}, S_{p4}, S_{n2}, S_{n3}, S_{T4}	C	C	C	D
[-3]	$-1.5V_{in}$	S_{p2}, S_{p4}, S_{n1}, S_{n3}, S_{T4}	C	C	D	D

However, NPC-type topologies suffer from drawbacks such as a significantly large number of switches in the load current path (N_{path}) and the number of switches in the charging loop ($N_{path, C}$). In recent years, a new topology proposed by Lee and Lee (2020) resolved these issues by extending the charging duration of SCs. The topology is termed switched-capacitor-based modular T-type inverter (SC-MTI). This significantly reduced the capacitor voltage ripples but at the expense of a high switch count. This article proposes an improved seven-level SCMLI that retains the main features of SC-MTI with additional improvements such as the following:

- Reduced the number of active power switches by four for seven-level voltage waveform generation.
- Only a single switch and a diode are utilized to charge each capacitor during all states of inverter operation.
- A lower number of switches in load current conduction and SC charging paths.
- The current flow among SCs is restricted. This is a benefit because the charging current only flows from the dc-link capacitor to the SCs.

Methodology

Figure 1A shows the seven-level bipolar circuit configuration of the proposed NPC topology. It comprises 12 switches with antiparallel diodes, four diodes, and four switched capacitors to generate seven equal voltage levels of the following amplitudes: $+0.5\ V_{in}$, $+1\ V_{in}$, $+1.5\ V_{in}$, $-0.5\ V_{in}$, $-1\ V_{in}$, $-1.5\ V_{in}$, and $0\ V_{in}$. It is a combination of an SC module and a T-type inverter. The SC module comprises basic SC units between the dc-link network and a T-type unit. In the proposed topology, the positive pole generates positive voltage levels and the negative pole is responsible for generating the negative voltage levels at

the load. Each pole uses separate paths for the charging process. It is noteworthy that the capacitors can be charged for at least the half-cycle of the operation, and the capacitors will remain in a charging state when not delivering power to the load. The operation of the seven-level inverter is shown in Figures 1B–H. Here, the path for carrying load current is indicated by red, blue dotted lines indicate the charging paths for switched capacitors, and the green line indicates freewheeled current in reactive mode. In this analysis, all power switches and diodes are assumed to be ideal, neglecting their on-state resistance and forward voltage drop. In addition, the SC voltage ripples are neglected by assuming large capacitors. Further, the generation of seven voltage levels based on the switching states of the proposed inverter is listed in Table 1. Here, "1" and "0" represent a switch's "ON" and "OFF" states, respectively. In contrast, "C" and "D" represent the charging and discharging of the SCs.

As detailed in Figure 1 and Table 1, both the inverter structure and operation of the proposed SCMLI are symmetrical. The capacitors in the positive pole are responsible for the positive half-cycle and the capacitors in the negative pole are responsible for the negative half-cycle of the output waveforms. For both unity power factor and nonunity power factors, the functions and operations of the involved capacitors are the same and are able to handle the same amount of power. Hence, all capacitor voltages in the circuit are naturally balanced at their rated values. Moreover, the upper SCs and lower SCs are connected in parallel with the dc-link capacitors for the positive and negative half-cycle levels, respectively. Therefore, their voltages can be self-balanced to the same magnitude as the dc-link voltage of $0.5\ V_{in}$.

To find the value of the capacitors, their longest discharging periods in a complete cycle must be evaluated for a permissible voltage ripple.

Therefore, by integrating the load current from t_{on} to t_{off}, the maximum amount of electric charge (ΔQ_C) discharged by each capacitor to the load can be expressed as follows.

$$\Delta Q_C = \int_{t_{on}}^{t_{off}} I_o \sin(2\pi f_o t - \varnothing) dt \qquad (1)$$

where I_o represents the load current, f_o is the output frequency, φ is the phase angle, and $[t_{on} - t_{off}]$ are the start and end instants of the capacitor discharging duration.

Therefore, considering the minimum voltage ripple (ΔV), the optimum capacitance of the capacitors can be obtained as

$$C = \frac{\Delta Q_C}{\Delta V_C} = \frac{\int_{t_{on}}^{t_{off}} I_o \sin(2\pi f_o t - \varnothing) dt}{\Delta V_C} \qquad (2)$$

where $V_C = 0.5\ V_{in}$ is the rated voltage of all employed capacitors in the proposed inverter and ΔV_C and V_C are the voltage ripple and the rated voltage of C, respectively. Eq. 2 shows that the voltage ripple can be controlled within a reasonable range by selecting a suitable capacitance.

Common-mode voltage

A detailed CMV and leakage current analysis of the proposed seven-level circuit configuration has been conducted in this section (Xiao, 2020). The equivalent circuit is drawn in Figure 1A. While, P and N represents input terminals of the input dc source (i.e., PV arrays), respectively. Whereas Va,N and Vb,N are the output voltages of the proposed inverter relative to the N terminal of the PV. Here, a and b are the output terminals of the differential mode voltage (V_{DM}), and C_1 and C_2 are photovoltaic (PV) parasitic capacitors against the ground. Considering parasitic C_1 for analysis, it is clear from Figure 1A that $V_{b,\ N} = 0.5\ V_C$ and $V_{a,\ N}$ for all switching states can be derived using Kirchhoff's voltage law according to the operating modes of the seven-level inverter and operating state of the switches tabulated in Table 1.

Taking point N as the reference, CMV (V_{CM}) and differential mode voltage (V_{DM}) are expressed as follows:

$$V_{CM} = \frac{V_{a,N} + V_{b,N}}{2} \qquad (3)$$

$$V_{DM} = V_{a,b} = V_{a,N} - V_{b,N} \qquad (4)$$

$$V_{a,N} = V_{CM} + \frac{V_{DM}}{2} \qquad (5)$$

$$V_{b,N} = V_{CM} - \frac{V_{DM}}{2} \qquad (6)$$

Both the CMV and DMV that contribute to the total CMV ($V_{CM,\ T}$) can be expressed using the equation below

$$V_{CM,T} = \frac{V_{a,N} + V_{b,N}}{2} + (V_{a,N} + V_{b,N}) \cdot \frac{L_2 - L_1}{2(L_2 - L_1)} \qquad (7)$$

where L_1 and L_2 are the filter inductors at the ac side.

While the leakage current (i_{CM}) is mainly induced by the fluctuation of CMV as expressed in Eq. 8.

$$i_{CM} = C \frac{dV_{CM}}{dt} \qquad (8)$$

It shows that the flow of the ground leakage current through the parasitic capacitance (C) is dependent on the behavior of CMV. In case CMV transitions occur at high frequency, it will introduce a large leakage current. Therefore, to minimize or eliminate the common-mode leakage current, it is necessary for CMV to be kept constant.

Assuming that the $L_1 = L_f$ and $L_2 = 0$, then

$$V_{CM,T} = \frac{V_{a,N} + V_{b,N}}{2} - \frac{V_{a,N} - V_{b,N}}{2} = V_{b,N} \qquad (9)$$

By putting the values obtained from Eq. 3 to Eq. 6 in Eq. 9, the total CMV values for different switching states can be obtained. From this analysis, it is clear that the variation of the CMV remains constant at 0.5 V_C at each switching for the proposed seven-level circuit topology. Therefore, the proposed topology naturally maintains the total CMV constant at 0.5 V_C because of the dc-link capacitor bridge arm. A similar procedure can be applied when considering parasitic capacitors (C_2) and V_{CM2}. The equivalent CM circuits can be derived, but here, $V_{b,\ N} = -0.5$, and the variation of the total CMV ($V_{CM,T}$) remains constant at $-0.5V_C$ and does not contain any high-frequency component, which practically eliminates the leakage current.

Comparison

This study conducts a comparative investigation with the SC-MTI (Lee and Lee, 2020) chosen as the benchmark reference and other state-of-the-art topologies for comparison. To evaluate the implementation cost-per-level for each inverter, the cost function (CF) is calculated using Eq. 10. Here, β is the weight coefficient and is set to 0.5 for all topologies. Here, N_S is equal to 1 for all inverters as single-source topologies are selected for comparison. Whereas $\mathbf{N_{Sw}}$ is the number of active power switches, $\mathbf{N_G}$ is the number of gate-drivers, $\mathbf{N_D}$ is the number of diodes, $\mathbf{N_C}$ is the number of SCs required, $\mathbf{TSV_{pu}}$ is the total standing voltage per unit, and $\mathbf{N_s}$ is the number of dc sources.

$$CF = \frac{(N_{Sw} + N_G + N_D + N_C + \beta TSV_{pu}) \times N_s}{7} \qquad (10)$$

Compared to SC-MTI, the proposed inverter reduced the number of required active switches by four for seven-level generation. In addition, only a single active switch and a diode are utilized to charge any switched capacitor in the proposed topology, and there is no charge flow among the capacitors. Overall, the cost is minimized, and the efficiency of the proposed inverter topology is significantly improved. A comprehensive comparison analysis among state-of-the-art SCMLIs and the proposed SCMLI is illustrated in Table 2. The numbers of switches employed in the proposed topology

TABLE 2 Performance comparison with existing switched-capacitor-based multilevel inverters.

T	Ref	[A]	[B]	[C]	[D]	[E]	[F]	[G]	[H]	[I]	[J] $\beta = 1$	[J] $\beta = 0.5$	[K]	[L]	[M]
Non-NPC SCMLIs	Khan et al. (2020)	7	11	1	1	1:3	3	1	20	2	4.37	3.9	×	×	93
	Saeedian et al. (2019)	9	8	4	2	1:4	4	2	16	2	3	2.66			96
	Roy et al. (2019)	7	9	2	2	1:3	3	1	17	4	4	3.56			92
	Ali and Krishnasamy, (2018)	9	11	0	2	1:2	1	0.5	11	4	3	2.97			NA
	Taghvaie et al. (2017)	7	9	0	1	1:1	1	1	9	3	4	3.35			91.7
	Roy and Sadhu, (2020)	13	14	2	4	1:3	3	1	34	2	3.3	3			91
NPC SCMLIs	Das et al. (2021)	5	8	6	4	1:1	1	1	12	2	7.6	6.4	√	×	95
	Rech, (2019)	5	8	0	3	1:1	1	0.5	5	4	4.4	4.3			NA
	Siwakoti et al. (2019b)	5	6	2	3	1:1	0.5	0.5	3.5	4	3.9	3.75			97
	Ye et al. (2021)	5	6	2	4	1:0.5	0.5	0.25	6	2	4.8	4.2			97
	Lee et al. (2019a)	7	10	0	4	1:1.5	1	0.5	9	4	4	3.8			97
	Lee and Lee, (2019)	7	10	0	4	1:1.5	2	1	10	2	4.7	3.96			97
	Lee et al. (2019b)	7	9	0	3	1:1.5	1	1	8	4	3.7	3.37			96
	Sathik et al. (2019)	7	10	0	3	1:1.5	1	1	9	4	4.75	3.71			98
	Sandeep et al. (2020)	7	9	0	4	1:1.5	1	0.5	8	4	3.77	3.45			96
	Zeng et al. (2019)	7	9	0	3	1:1.5	1	1	8	4	3.6	3.31			95
	Lee et al. (2019c)	7	9	0	1	1:1.5	1	1	9	4	3.58	3			96
		9	12	0	2	1:1	1	0.5	11	6	4.11	3.5			96
		11	12	0	2	1:2.5	2	1	33	6	3.56	2.8			96
	Lee and Lee, (2020)	7	16	0	4	1:1.5	2	0.5	14	3	6.64	5.8	√	√	NA
	PT	7	12	4	4	1:1.5	2	0.5	14	2	5.90	5.2			97.5

Parameters: [A] number of voltage levels, [B] number of active power switches, [C] number of diodes, [D] number of SCs, [E] gain, [F] maximum switch's voltage, [G] maximum capacitor's voltage, [H] total standing voltage, [I] number of power switches in charging loop (Nc, path), [J] CF, [K] CMV elimination ability, [L] SC charging duration exceeds half-cycle, [M] conversion efficiency (%) @ 50 Hz.

are similar to those of the topologies presented by Khan et al. (2020), Barzegarkhoo et al. (2021), and He et al. (2021). Unlike many SCMLIs, however, owing to the reduction in the number of active switches, the reverse-power flow is not restricted by the proposed SCMLI, making it suitable for grid-connected renewable energy sources.

Although the gain of the proposed inverter is low (i.e., only 1.5 V_{in} for seven levels) compared to some other topologies, it provides other benefits such as lower voltage ripple, leakage current minimization, and single-source utilization. In addition, it uses a single switch and diode to charge each switched capacitor, and the switches in the charging path are more in SC-MTI. Also, the current flow among SCs is restricted because of its unique structure. In addition, it has the same ripple as the latest topology (Barzegarkhoo et al., 2021) while reducing the component count and conduction loss. In the topologies by Ali and Krishnasamy (2018), Peng et al. (2019), Roy et al. (2019),

Saeedian et al. (2019), Khan et al. (2020), Chen et al. (2021), He et al. (2021), and Roy et al. (2021), because the neutral of the ac output is connected to a half-bridge or full-bridge, CMV is introduced. Therefore, their topological structures induce the risk of leakage current, making these SCMLIs less viable for photovoltaic (PV) applications. The lack of reactive power capability in nonunity reactive power mode is the main drawback of the topology (Saeedian et al., 2019). Hence, it is unsuitable for grid-connected renewable energy sources. As can be observed from Table 2, the inverter structures (Ali and Krishnasamy, 2018; Peng et al., 2019; Roy et al., 2019; Saeedian et al., 2019; Khan et al., 2020; Chen et al., 2021; He et al., 2021; Roy et al., 2021) require three dc sources for three-phase applications, unlike the proposed topology that needs only one dc source. To minimize power loss in SCMLIs, it is necessary to use a low number of switches in the different levels (N_{path}) and charging paths of SCs ($N_{path, c}$). For example, four and three switches are conducted in SC's

FIGURE 2
Experimental validation and power-loss analysis of the proposed topology.
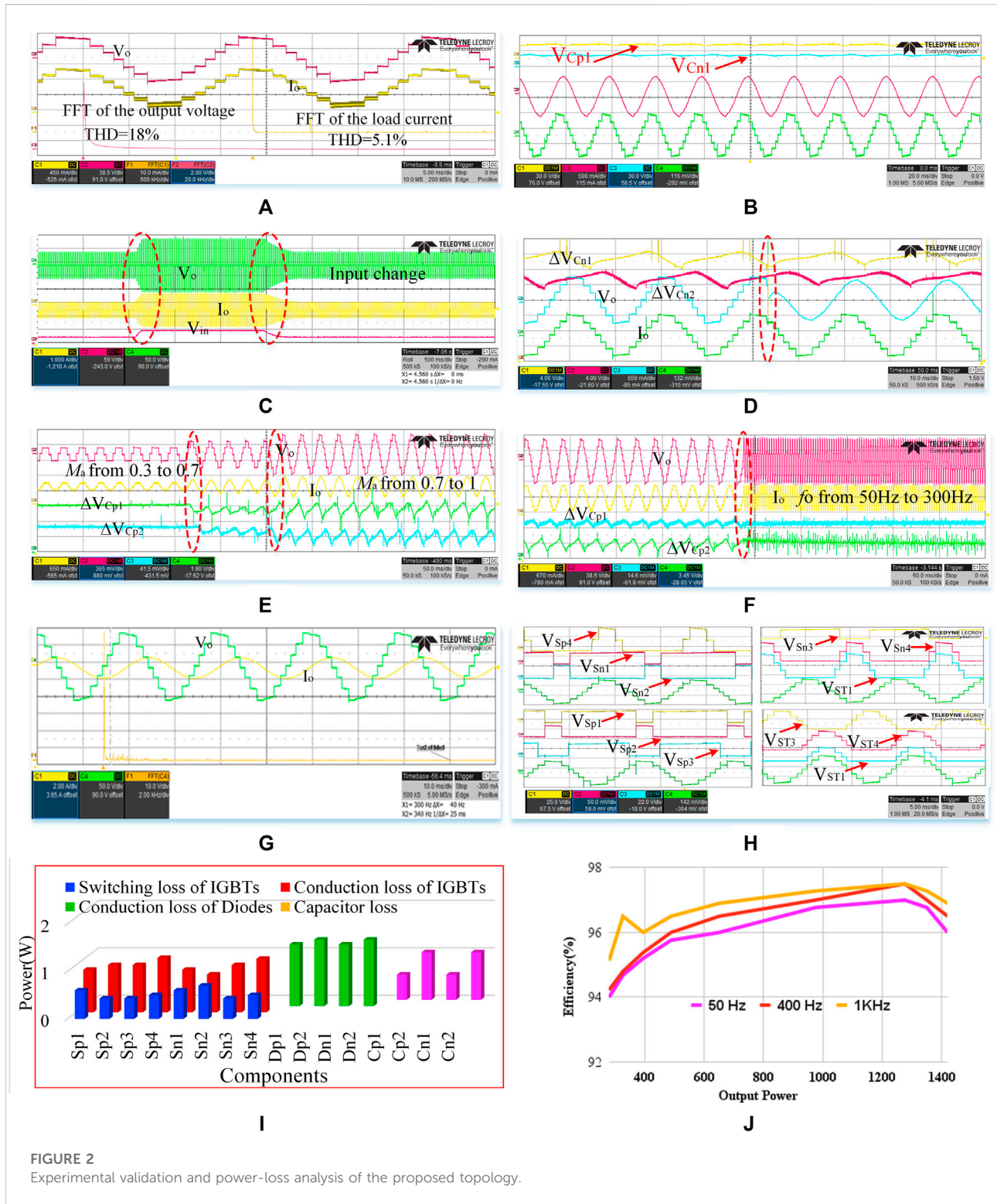
charging path for the SCMLIs proposed by Lee et al. (2019b), Sathik et al. (2019), Zeng et al. (2019), Sandeep et al. (2020), and Lin et al. (2021) and by Taghvaie et al. (2017) and Lee and Lee (2020), respectively. At the same time, only two switches are conducted in SC's charging path for each SC in the study by Das et al. (2021) and Lee and Lee (2019). However, these inverters require more switches, and the discharging duration is higher than the charging duration.

Results

In the laboratory, a seven-level inverter prototype was developed to verify the performance evaluation of the proposed topology. The input dc source voltage was set to 60 V, and 1200 μF capacitors were selected. To test the proposed topology operating at a low switching frequency, the nearest level control (NLC) modulation technique with dSPACE 1104 controller was used to generate gate signals for the power switches. The NLC method, also called the round modulation method or the half-integer method, can be easily performed by round function (Sathik et al., 2021; Mustafa et al., 2022; Siddique et al., 2022). This technique can produce the closest voltage level by comparing the inverter output voltage with the reference sinusoidal voltage to produce proper switching signals.

The experimental results obtained in the steady state of the inverter operation are presented in Figures 2A and B. Figure 2A shows the voltage and current frequency spectra of the output voltage considering pure resistant load ($R = 200\,\Omega$). Here, the output voltage and current seven-level staircase waveforms were obtained without using output filters. Meanwhile, its peak of fundamental output voltage reached nearly 90 V, which was 1.5 times that of the input voltage. The THD values of the output voltage and load current without filters were 16.5 and 16.1%, respectively. The corresponding output voltage waveform for the nonunity power factor with $R = 100\,\Omega$ and $L = 200$ mH, is shown in Figure 2B, as it can be observed that the SCs (C_{p1} and C_{n1}) were balanced at approximately 30 V in the steady state.

Similar tests were conducted to investigate the feasibility of the inverter in dynamic modes of operation. It was tested for load, input voltage, modulation index, and output frequency variations. The experimental waveforms under the input voltage and load variations are shown in Figures 2C and D. It is clear from Figure 2C that the operation of the inverter is very stable for transient changes in input voltage from 30 to 60 V and vice versa. The experimental waveforms are shown in Figure 2D to verify the performance of the inverter for a step change in load from an R-load ($R = 100\,\Omega$) to an RL-load ($R = 100\,\Omega$, $L = 100$ mH). While the voltage across the capacitors remains balanced during transient variation in load. It can be observed that the peak magnitude of the voltage ripples of C_{p1} and C_{n1} was about 3.5 V; as for C_{p2} and C_{n2}, they were approximately 4.1 V.

In the end, the inverter was tested with a step change in modulation index (M_a) and output frequency. The results are captured in Figures 2E and F. When M_a was suddenly changed from 0.3 to 0.7 and then to 1, seven, five, and three voltage levels were achieved in the output, respectively, and the load current also increased accordingly. The load current affects the magnitude of discharging current of the SCs, and therefore, it influences the discharge amount of the SCs, which will, in turn, influence the ripples of the capacitor voltage. The results under the condition of a step change of the output frequency (f_o) are shown in Figure 2F. It can be observed that the output voltage waveforms were unaffected

during either the modulation index or frequency transient. The results confirmed that the proposed inverter was able to adapt to sudden variations in modulation index and load. Figure 2G shows the experimental results at an RL-load (R = 10 Ω, 200 mH) to show the validity of the proposed inverter at low power factors. The blocking voltage experimental waveforms for different switches are captured in Figure 2H. The maximum blocking voltage of the switches in $S_{u1,\,1}$, $S_{u1,\,2}$, $S_{l1,\,1}$, $S_{l1,\,2}$, $S_{u2,\,1}$, and $S_{l2,\,1}$ was within 30 V. The maximum blocking voltage for $S_{u2,\,2}$ and $S_{l2,\,2}$ was 60 V. The maximum blocking voltage for S_{T1} and S_{T2} was within 90 V. In a similar way, the maximum blocking voltage for switches S_{T3} and S_{T4} was within 120 V.

The power-loss analysis of the seven-level topology has been carried out in this section. At 158 W measured output power of the inverter, the total loss of the topology observed from the circuit was 16.26 W (input power = 175 W). At this power, the efficiency of 90.28% was reported with a high switching technique (10 kHz). Then, a detailed power-loss analysis was carried out for the proposed seven-level inverter using PLECS simulation software. Here, the inverter efficiency, loss distribution among power components, and temperature profile of switches in steady-state conditions for the proposed SC inverter were analyzed over a wide range of output power.

In the following analysis, the parameters taken into consideration at steady-state conditions are the following: (a) IGBT loss (both switching loss and conduction loss), (b) diode conduction loss, and (c) capacitor equivalent series resistance loss or ripple loss. In this case, the input voltage source was set to 300 V. With the parameters used for experimental testing, the proposed seven-level inverter was modeled and implemented in PLECS. The thermal modeling of the semiconductor devices was developed from the datasheet of the IKY75N120CH3 module manufactured by Infineon Technologies AG. The parasitic resistances of the capacitors (1200 μF) were set at 0.1Ω. The loss distribution among power components in steady-state conditions for the proposed SC inverter is given in Figure 2I.

The measured efficiencies for different operation frequencies with a unity power factor at various power loads such as 0.3, 0.4, 0.5, 0.6, 0.9, 1.2, and 1.4 kW are plotted in Figure 2I. It can be observed that the proposed seven-level SCMLI gave maximum efficiency of 97.5% at 1276 W for 400 Hz and 1 kHz. Overall, the observed effects of the output current and frequency on the conversion efficiency coincided with the theoretical analysis. The ripple losses were not dominating at light load, and the simulated efficiencies at operating frequencies (50 Hz, 400 Hz, and 1 kHz) were very close to each other. The simulated efficiency for the seven-level inverter was about 97.5%. When the output power was gradually increased, the conversion efficiency became significantly improved at 1 kHz over 50 Hz, along with the reduction in the voltage ripples of SCs. By increasing the frequency at 350 Ω load, the efficiency increased from 94 to 96%. However, the efficiency variation measured between 400 Hz

and 50 kHz was insignificant because of the large *RC*-time constant of the SCs selected in the prototype.

Conclusion

In this article, a new SC-based inverter with a low switch count was suggested. Also, the CMV was significantly minimized by connecting the neutral of the output terminal to the midpoint of dc-link capacitors. In addition, SCs were charged beyond half-cycle, which minimized the capacitor's voltage ripples and current spikes during the SC charging process. Moreover, the proposed structure featured main advantages such as a low number of conducting switches in current flow paths and SC charging paths. Moreover, the current flow among SCs was restricted. This is a benefit because the charging current only flows from the dc-link capacitor to the SCs. The comparative analysis and cost comparison against its benchmarked topology (SC-MTI) and recently introduced SCMLIs confirmed the superiority of the proposed SCMLI. Further, the performance of the proposed inverter was verified by conducting experimental tests at steady- and dynamic-state conditions. The tests were performed at different loadings and modulation indices. The additional feature of the proposed inverter was its capability to integrate inductive loads. In the end, a PLECS power-loss modeling and conversion efficiency evaluation was provided for the proposed topology.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material. Further inquiries can be directed to the corresponding authors.

Author contributions

SK contributed to the conception and methodology and performed the analysis. SK wrote the first draft of the manuscript. SK and MA wrote sections of the manuscript. SA and NN supervised this work. SM, MS, and AS arranged the funding acquisition. All authors contributed to the manuscript, read, and approved the submitted version.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

The handling editor NP is currently organizing a research topic with the author SM.

Publisher's note

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