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Device performances analysis of p-type doped silicene-based field effect transistor using SPICE-compatible model

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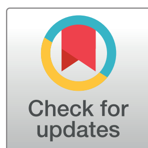

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Abstract

Moore's Law is approaching its end as transistors are scaled down to tens or few atoms per device, researchers are actively seeking for alternative approaches to leverage more-than-Moore nanoelectronics. Substituting the channel material of a field-effect transistors (FET) with silicene is foreseen as a viable approach for future transistor applications. In this study, we proposed a SPICE-compatible model for p-type (Aluminium) uniformly doped silicene FET for digital switching applications. The performance of the proposed device is bench-marked with various low-dimensional FETs in terms of their on-to-off current ratio, sub-threshold swing and drain-induced barrier lowering. The results show that the proposed p-type silicene FET is comparable to most of the selected low-dimensional FET models. With its decent performance, the proposed SPICE-compatible model should be extended to the circuit-level simulation and beyond in future work.

1. Introduction

In the modern lives, the computing power of digital devices has been improved by the technology innovations in the miniaturisation of semiconductor transistors [1]. The famous Moore's Law will soon experience its fundamental limit because of various constraints in bulk silicon (Si) technology, especially in the sub-10-nm atomic scales [2–4]. Therefore, the more-than-Moore development of the alternative field-effect transistors (FETs) has attracted much attention in the nanoelectronic research communities. Numerous industrial and public funds and programmes were initiated globally to overcome these "roadblocks" for long-terms advances in computing technology beyond Moore's Law [5].

Among the options in the more-than-Moore race, two-dimensional (2D) materials have emerged as the prospective contenders owing to their atomically thin structure. Following the success of graphene since 2004 [6], research activities regarding 2D materials are intensely stimulated. Until now, more than 1800 exfoliable 2D candidates are theoretically predicted based on density-functional theory (DFT) [7], among which silicene could play a major role in future transistors owing to its outstanding carrier mobility [8] and compatibility with the

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cutting-edge Si wafer technology [9]. Silicene was also shortlisted as a potential material for transistor miniaturisation in the International Roadmap for Devices and Systems (IRDS) [10].

In 2015, Tao *et al*. [9] fabricated the first silicene-based transistor operating at room temperature. Moreover, silicene nanosheets have successfully been fabricated on various substrates in their buckled [11–13] and planar [14] forms. However, the deposition of silicene monolayers on metals substrates is less practical viable for transistor applications, as compared to the direct growth on insulating layers, such as dielectrics or oxides [15]. This shortcoming can be addressed by using computational modelling and simulation while waiting for the breakthrough in silicene-based fabrication techniques.

Concerning the computational models of silicene-based transistors [16, 17], rigorous efforts were invested by many groups of researchers. The absence of bandgap in pristine silicene did not halt its exploration for nanotransistor applications. In spite of the challenges, various bandgap engineering techniques have been explored, and such examples include confinement through silicene nanoribbons (SiNRs) [18–20], co-decoration [21], and doping [22–24]. Among the aforementioned techniques, doping is the most commonly employed technique in the semiconductor industry to alter the electronic properties [25]. Furthermore, the performance of SiNR FETs are sensitive to their device dimensions [20, 26]; and it is still a major challenge to precisely control the widths of nanoribbons even for the established graphene monolayers [27]. Therefore, a uniformly aluminium (Al) doped silicene monolayer was proposed to engineer the bandgap of silicene, producing the $AlSi_3$ monolayer. In addition, a SPICE-compatible model was created to facilitate studies beyond the device-level simulation [28], such as the gate and logic levels.

Fig 1 shows the schematic diagrams of the proposed $AlSi_3$ FET and the simplified top-of-the-barrier (ToB) nanotransistor circuit model. In this study, we developed of a SPICE-compatible model for the proposed $AlSi_3$ FET from the ToB nanotransistor model and benchmarked its device performance metrics with other published low-dimensional transistor models. **Section 2** describes the modelling procedures to obtain the current-voltage (I-V) characteristics and the respective model evaluation methodology. **Section 3** discusses the device performance of $AlSi_3$ FET with respect to its close low-dimensional contenders. Finally, **Section 4** includes the conclusion of this work and future work recommendation.

2. Methodology

This section describes the overall modelling procedures employed in this study, where the overall flowchart is shown in **Fig 2**.

2.1. ToB nanotransistor and SPICE models

The atomic structure of the $AlSi_3$ monolayer (as shown in **Fig 1**) was adapted from published DFT study [29]. By using the derivation from time-independent Schrödinger equation [30], the electronic transport effective mass was then obtained by using nearest neighbour tight-binding (NNTB) model and parabolic band assumptions as $m_e^* = 0.235m_0$ and $m_h^* = 0.255m_0$ for electrons and holes, respectively. The material-level modelling was shown in details in our previous work [22].

Table 1 summarises the device parameters of the $AlSi_3$ FETs. In the ToB nanotransistor model [31], net induced mobile charge can be obtained by $\Delta P = (P_S + P_D) - P_0$ where P_S and P_D are the non-equilibrium charge densities at the source and drain terminals, respectively, and P_0 is the equilibrium charge density. The self-consistent potential U_{SCF} at the ToB is obtained

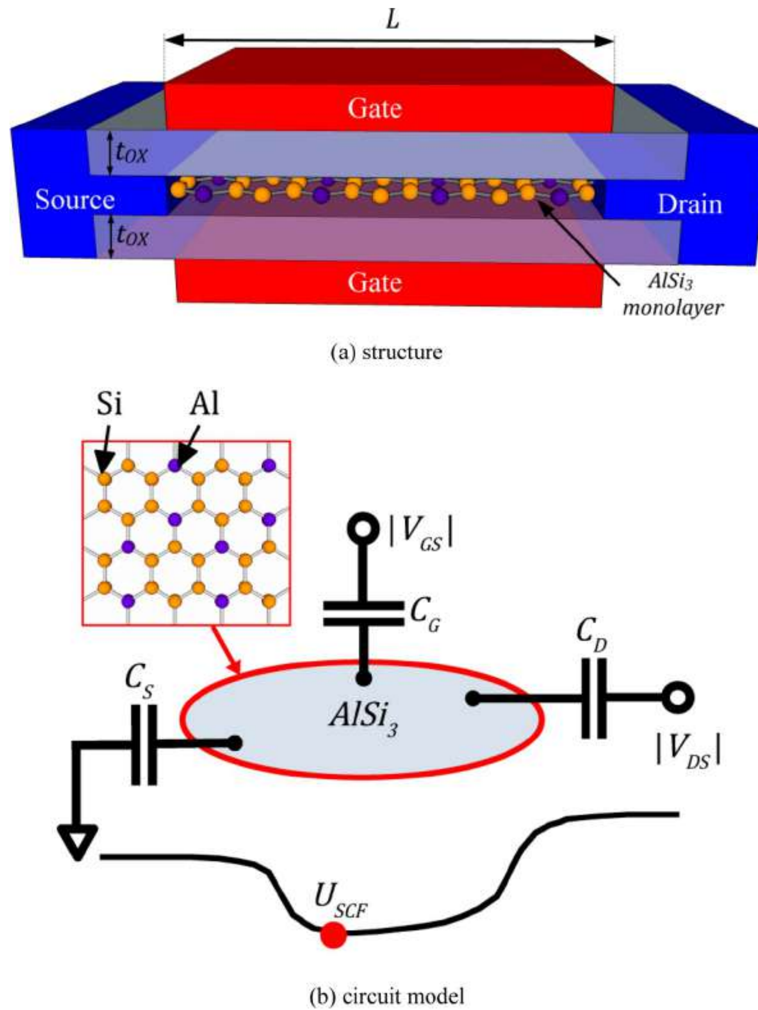

Fig 1. Schematic diagrams of $AlSi_3$ FET: (a) the structure and (b) the ToB nanotransistor circuit model. The gate, drain and source terminal capacitances are denoted as C_G, C_D, and C_S, respectively.

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by using

$$U_{SCF} = -q\left(\alpha_G|V_{GS}| + \alpha_D|V_{DS}| + \alpha_S V_S - q\frac{\Delta P}{C_\Sigma}\right), \quad (1)$$

where q is the constant for electric charge and the total terminal capacitances is expressed as $C_\Sigma = C_G+C_D+C_S$. Because the source terminal is always set to be zero, α_S can be ignored. In an ideal FET, the perfect gate and drain control parameters $\alpha_G = 1$ and $\alpha_D = 0$ [18] are used to mimic the ideal I-V characteristics. However, the default gate and drain control parameters $\alpha_G = 0.880$ and $\alpha_D = 0.035$ [31] were used in this work.

Subsequently, the current-voltage (I-V) characteristics of p-type $AlSi_3$ FET can be obtained in terms of V_{DS} and V_{GS}, by employing Landauer-Büttiker ballistic transport equation [31] along with Fermi-Dirac integral solutions [32], given as

$$|I_{DS}(|V_{GS}|,|V_{DS}|)| = \frac{gW}{\hbar^2}\sqrt{\frac{m_h^* q^2 (k_B T)^3}{2\pi^3}}\left\{\log[1+e^{\eta_S(|V_{GS}|,|V_{DS}|)}] - \log[1+e^{\eta_D(|V_{GS}|,|V_{DS}|)}]\right\}, \quad (2)$$

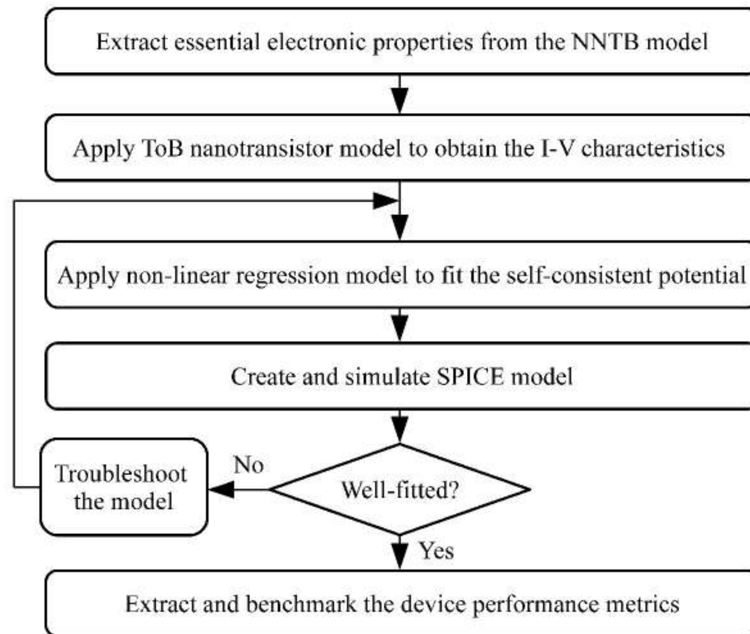

Fig 2. Overall flowchart of this study.

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with the normalised energies of

$$\eta_S(|V_{GS}|,|V_{DS}|) = \frac{E_F - U_{SCF}(|V_{GS}|,|V_{DS}|)}{k_B T}, \tag{3}$$

$$\eta_D(|V_{GS}|,|V_{DS}|) = \frac{E_F - U_{SCF}(|V_{GS}|,|V_{DS}|) - q|V_{DS}|}{k_B T}, \tag{4}$$

for source and drain, respectively. In the equations, g is the degeneracy factor (set as 2 to include up and down spins); $\hbar$ is the Planck's constant; and k_B is the Boltzmann constant. **Fig 3(A)** shows the I-V characteristics for $AlSi_3$ FET produced by the ToB nanotransistor model.

Following that, the results from ToB nanotransistor were further used to create the SPICE model to allow cross-platform and non-iterative simulation. Moreover, SPICE models are one of the essential tools in the IC design industry for simulation [28]. Before creating the SPICE model, a non-linear regression model [33] was employed to fit the self-consistent potential

Table 1. The device parameters of $AlSi_3$ FETs.

Parameters	Values
Band structures	NNTB
Hole effective mass, m_h^*	$0.255m_0$
Bandgap, E_g	0.78 eV
Oxide material	SiO_2
Oxide thickness, t_{OX}	1.5 nm
Temperature, T	300 K

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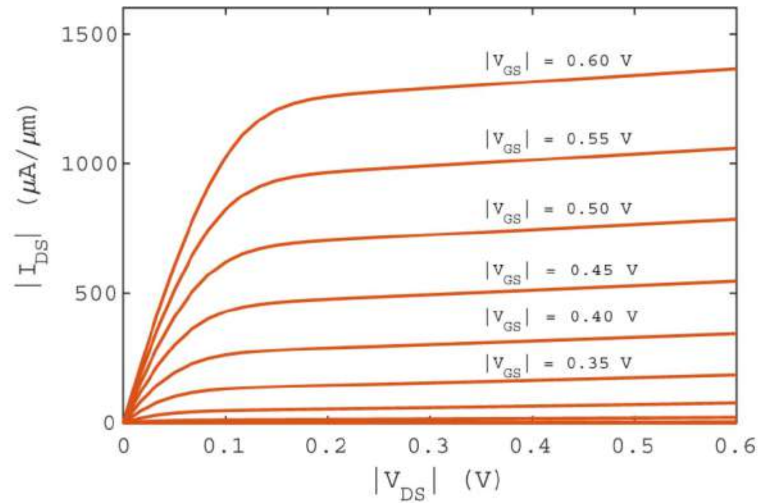
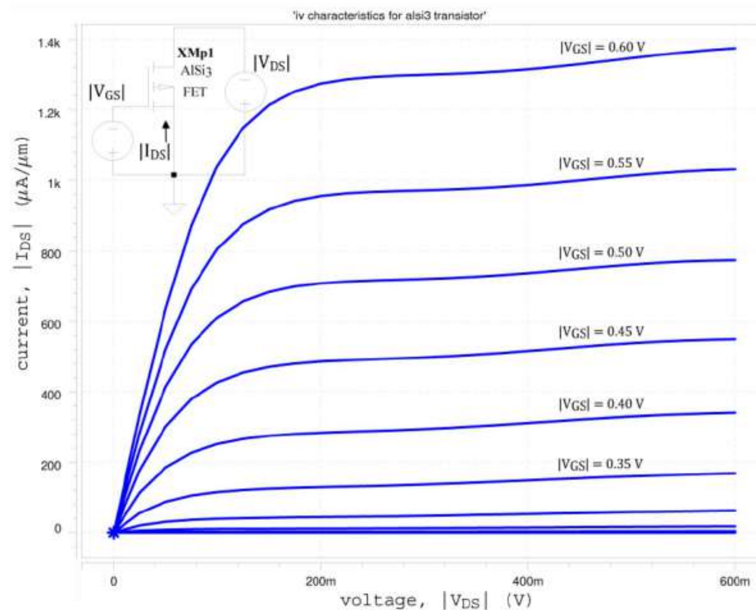


(a) ToB nanotransistor model



(b) SPICE model

Fig 3. I-V characteristics of $AlSi_3$ FET simulated using (a) ToB nanotransistor model and (b) SPICE model.

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U_{SCF}, given as

$$U_{SCF}(|V_{GS}|, |V_{DS}|) = \sum_{k=0\ to\ 5}^{j=0\ to\ k} P_{\{j\}\{k-j\}}(|V_{GS}|^j + |V_{DS}|^{k-j}), \tag{5}$$

where the coefficients $P_{\{j\}\{k-j\}}$ for each respective $|V_{GS}|^j|V_{DS}|^{k-j}$ term were computed and optimised using MATLAB curve fitting tool. By using the MATLAB Curve Fitting tool, it was found that the lower orders of polynomial equations fail to fit the USCF well and, as a result, are unable to reproduce accurate I-V characteristics. Therefore, the fifth-order polynomial equation (highest number of order available in the MATLAB Curve Fitting tool) is chosen

although the resulting equation is slightly long. The expansion of **Eq (5)** and the respective coefficients $P_{\{j\}\{k-j\}}$ are attached along with the SPICE model library files in the S1 File. **Fig 3(B)** shows the I-V characteristics for $AlSi_3$ FET produced by the SPICE model.

2.2. Model evaluation

In this subsection, a statistical method is employed to evaluate the accuracy of the SPICE model with respect to the ToB nanotransistor model for the proposed $AlSi_3$ FET. The models were evaluated by using the normalised root-mean-square-deviations (RMSD) [29], given as

$$RMSD = \frac{\sqrt{\sum_{i=1}^{N} (p_i - q_i)^2 / N}}{\max(p_i, q_i) - \min(p_i, q_i)} \times 100\%, \tag{6}$$

where N denotes the total number of data, p_i and q_i are the values of ith data for the ToB nanotransistor model and the SPICE model, respectively. **Fig 4(A)** shows the I-V characteristics

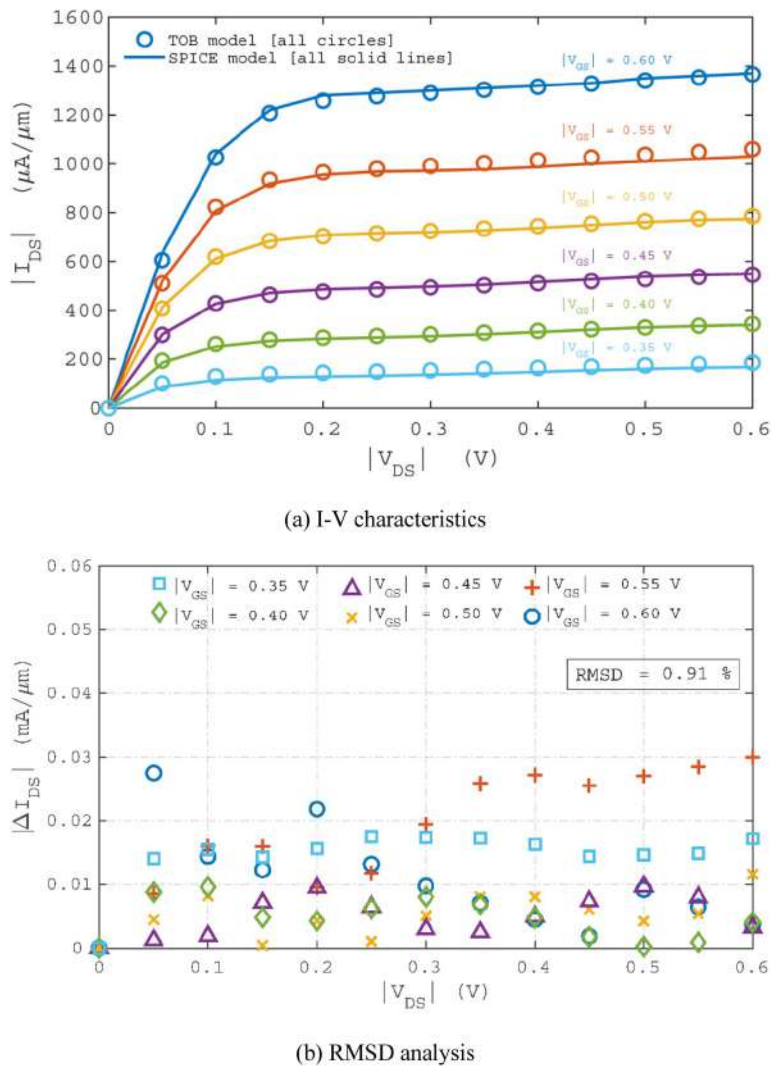

Fig 4. Comparison between the ToB nanotransistor model and SPICE model of the $AlSi_3$ FET. The empty dots in (a) represent the results of the ToB nanotransistor model while the solid lines in (a) represent the results of the SPICE model.

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combining the results of the ToB nanotransistor model and the SPICE model. The point-by-point differences to compute RMSD are plotted in **Fig 4(B)**. Overall, 0.91% of RMSD is produced by the SPICE model when it is benchmarked with the results from the ToB nanotransistor model, indicating that the model has produced a decent fit.

3. Performances analysis and discussion

We can analyse the device performances by extracting the device metrics from the proposed p-type $AlSi_3$ FET model. **Fig 5** shows the graphical extraction approach to obtain on-to-off current (I_{on}/I_{off}) ratio, subthreshold swing (SS), and drain-induced barrier lowering (DIBL). The proposed $AlSi_3$ FET produces an I_{on}/I_{off} ratio of 2.6×10^5, a SS of 67.8 mV/dec, and a DIBL of 48.2 mV/V.

In this work, we compared our proposed p-type $AlSi_3$ FET with respect to other low-dimensional FETs. We have selected other published works on low-dimensional FETs to fairly assess the device performance of the proposed $AlSi_3$ FET. The selected published models include co-decorated SiNR FET [21], 27-ASiNR FET [20], Si nanowire (SiNW) FET [34], Si thin sheet FET [35], carbon nanotube (CNT) FET [36], graphene nanoribbon (GNR) FET [37], black phosphorene (BP) FET [38], and monolayer molybdenum disulfide (MoS_2) FET [39]. To concisely compare the device performance metrics, the comparisons are presented as bar graphs as shown in **Fig 6**. Regarding the I_{on}/I_{off} ratio, the performance of $AlSi_3$ FET model is slightly inferior to 27-ASiNR FET [20] and MoS_2 FET [39]. Regarding the SS, $AlSi_3$ FET model is also

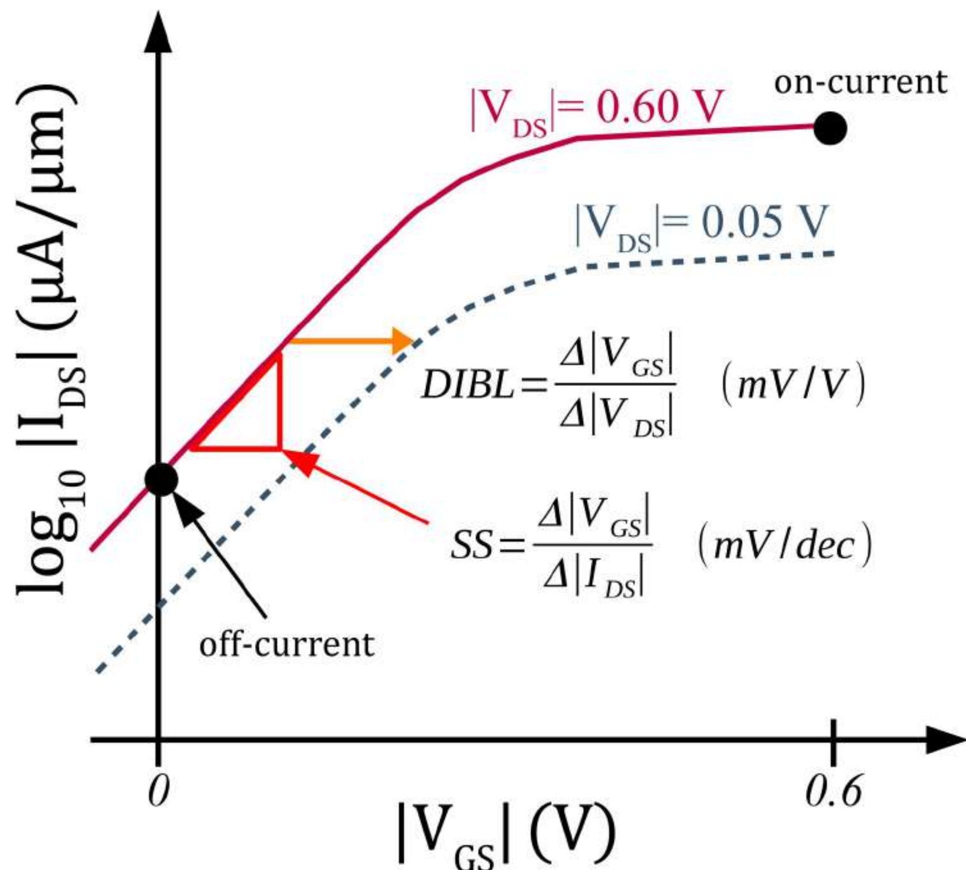

Fig 5. Definitions of the device performance metrics of a FET.

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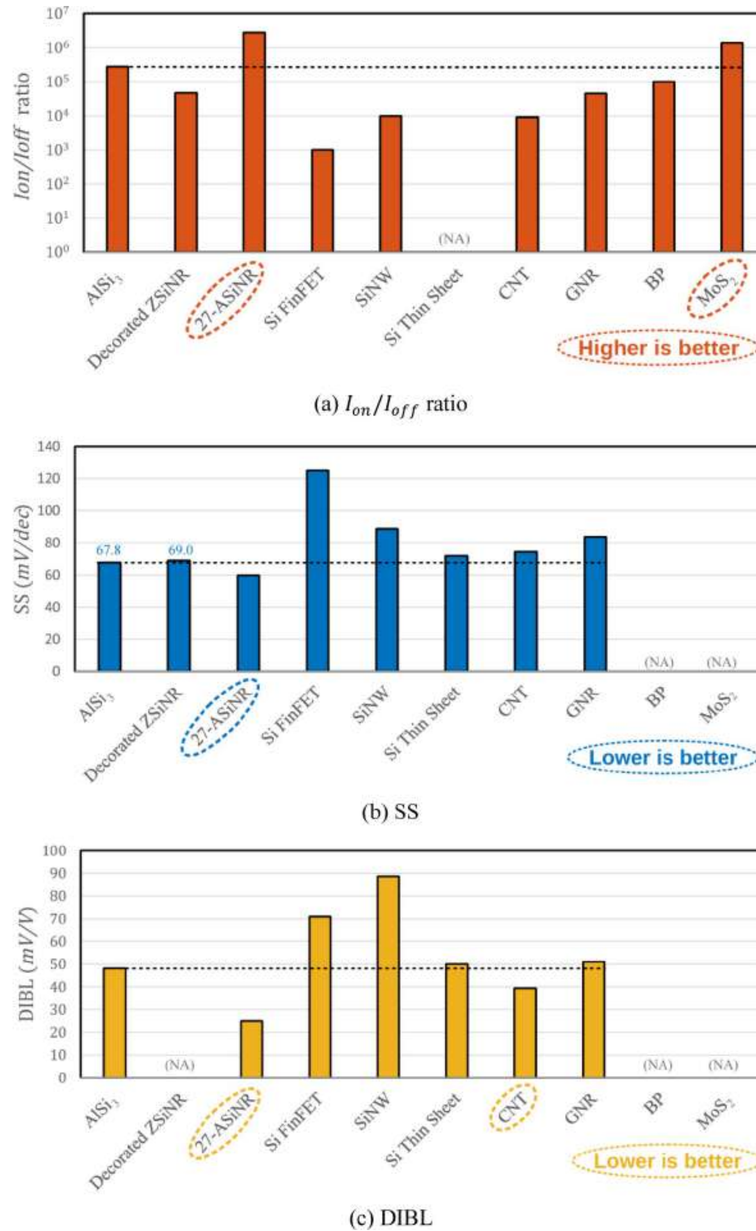

Fig 6. Device performances analysis between the proposed $AlSi_3$ FET model with published transistor models based on various low-dimensional materials. NA (not available) in the bar graphs denotes the unavailable data.

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slightly higher than the 27-ASiNR FET [20]. Concerning the DIBL, $AlSi_3$ FET model is also outperformed by 27-ASiNR FET [20] and CNT FET [36]. However, the challenges remain owing to the fabrication compatibility of non-Si-based materials and the difficulty to precisely control the widths of nanoribbons [27, 40]. Therefore, the proposed $AlSi_3$ FET model is still a prospective alternative for future nanotransistor applications.

4. Conclusion

In this paper, we have investigated a SPICE-compatible model for p-type uniformly Al-doped silicene FET. Following that, the device performance of the proposed model is compared with

other published low-dimensional nanotransistors. Although the proposed silicene FET is slightly inferior to a few competitors, silicene-based FETs are still one of the potential ways for more-than-Moore nanoelectronic applications owing to its Si-based nature. This work can be extended by performing further circuit-level simulation beyond the transistor device level by using the proposed SPICE model.

Supporting information

S1 File. SPICE model.
(DOCX)

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Author Contributions

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Formal analysis: Mu Wen Chuan, Afiq Hamzah.

Funding acquisition: Munawar Agus Riyadi, Michael Loong Peng Tan.

Investigation: Munawar Agus Riyadi.

Methodology: Mu Wen Chuan.

Project administration: Nurul Ezaila Alias, Michael Loong Peng Tan.

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Software: Afiq Hamzah, Cheng Siong Lim.

Supervision: Nurul Ezaila Alias, Michael Loong Peng Tan.

Validation: Munawar Agus Riyadi, Afiq Hamzah.

Visualization: Suhana Mohamed Sultan.

Writing – original draft: Mu Wen Chuan.

Writing – review & editing: Mu Wen Chuan, Munawar Agus Riyadi.

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