ENHANCED ADAPTIVE THERMAL-AWARE ROUTING ALGORITHM FOR NETWORK-ON-CHIP

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ABSTRACT

Routers in 3D NoC are responsible for generating more heat than other components putting an extra strain on the chip cooling cost. Various methods have been suggested to balance temperature distribution, including thermal-aware routing. Thermal-aware adaptive routing is a viable remedy to reduce thermal hotspots by migrating load to the cooler areas of the chip, hence adopting longer and extended paths and suffering from traffic congestion in the network. Furthermore, routing algorithms fetch parameters from neighbouring nodes each time, causing an extra strain on the network. The objective of this study was to have a balance between path length and temperature, reduce the workload on thermally unstable paths and reduce control traffic overhead. This work presented an efficient thermal-aware adaptive routing. The proposed work could adaptively choose the next neighbour at each intermediate node, leading the packet closer to the destination. An effective thermal-aware dynamic weighted adaptive routing was also proposed in this study. The dynamic weighted model had considered parameters related to congestion and thermal issues and provided a suitable balanced approach according to the current situation at each node. Furthermore, an interval-based record-keeping mechanism was proposed to record parameters of previously accessed nodes. Therefore, better, efficient and rapid routing decisions could be made. Results obtained from the simulations showed that the proposed routing algorithms had performed a 12-49% improvement in terms of global average delay under various synthetic traffic conditions compared to the state-of-the-art ATAR. The proposed techniques had observed 24-30% lower hop counts and considerable reduction in thermal profiling, along with up to 35-60% more valid records found from the history table compared to existing techniques. Overall, the proposed routing techniques have contributed to finding progressive routing paths and reducing control traffic overhead within the network.

ABSTRAK

Penghala dalam 3D NoC bertanggungjawab untuk menghasilkan lebih banyak haba daripada komponen lain yang memberi tekanan tambahan pada kos penyejukan cip. Pelbagai kaedah telah dicadangkan untuk mengimbangi taburan suhu, termasuk penghalaan sedar haba. Penghalaan adaptif sedar haba adalah salah satu penyelesaian untuk mengurangkan titik panas haba dengan memindahkan beban ke kawasan cip yang lebih sejuk, dengan itu menggunakan laluan yang lebih panjang dan lanjutan serta mengalami kesesakan lalu lintas dalam rangkaian. Tambahan pula, algoritma penghalaan mengambil parameter dari nod jiran setiap kali, menyebabkan ketegangan tambahan pada rangkaian. Objektif kajian ini adalah untuk mengimbangi antara panjang laluan dan suhu, mengurangkan beban kerja pada laluan yang tidak stabil secara haba dan mengurangkan overhed trafik kawalan. Kerja ini membentangkan penghalaan adaptif sedar haba yang cekap. Kerja yang dicadangkan secara adaptif mampu memilih jiran seterusnya pada setiap nod perantaraan, membawa paket lebih dekat ke destinasi. Penghalaan adaptif berwajaran dinamik sedar haba yang berkesan turut dicadangkan dalam kajian ini. Model berwajaran dinamik telah mempertimbangkan parameter yang berkaitan dengan isu kesesakan dan haba dan menyediakan pendekatan seimbang yang sesuai mengikut situasi semasa pada setiap nod. Tambahan pula, mekanisme penyimpanan rekod berasaskan selang waktu telah dicadangkan untuk merekodkan parameter nod yang diakses sebelum ini. Oleh itu, keputusan penghalaan yang lebih baik, cekap dan pantas boleh dibuat. Hasil kajian yang diperoleh daripada simulasi menunjukkan bahawa algoritma penghalaan yang dicadangkan telah melakukan peningkatan 12-49% dari segi purata lengah keseluruhan di bawah pelbagai keadaan trafik sintetik berbanding dengan ATAR yang canggih. Teknik yang dicadangkan juga memerhatikan 24-30% kiraan hop yang lebih rendah dan pengurangan ketara dalam pemprofilan haba, sehingga 35-60% lebih rekod sah yang ditemui daripada jadual sejarah berbanding teknik sedia ada. Secara keseluruhan, teknik penghalaan yang dicadangkan telah menyumbang kepada pencarian laluan penghalaan progresif dan mengurangkan overhed trafik kawalan dalam rangkaian.

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LIST OF ABBREVIATIONS

2D	-	2-Dimentional
3D	-	3-Dimentional
3DIC	-	3D Integrated Circuit
ACO	-	Ant Colony Optimization
ANN	-	Artificial Neural Networks
ATAR	-	Adaptive Thermal-Aware Routing
BO	-	buffer occupancy
BTI	-	Bias Temperature Instability
CMP	-	Chip Multi-Processors
CPU	-	Central Processing Unit
CTTAR	-	Collaborative Thermal- and Traffic-Aware Adaptive Routing
DCAT	-	Distributed-Centralized Ageing Table
DFS	-	Dynamic Frequency Scaling
DFSB	-	Dynamic Frequency Scaling
DPRA	-	Deterministic Path Routing Algorithm
DST	-	Destination
DTM	-	Dynamic Thermal Management
DVFS	-	Dynamic Voltage And Frequency Scaling
DVS	-	Dynamic Voltage Scaling
DyAD	-	Deterministic and Adaptive Routing
EBL	-	Effective Buffer Length
EFuNN	-	Evolving Fuzzy Neural Network
ETW	-	East Then West
FAAR	-	Frequency-Aware Adaptive Routing
FMoTAR	-	Fast Multi-Object Thermal-Aware Adaptive Routing Algorithm
FS	-	Flit Serialization
FTRA	-	Fault Tolerant Routing Algorithm
GCAR	-	Game based congestion-aware adaptive routing
GTDAR	-	Game theory based thermal-aware adaptive routing
HRA	-	Heuristic Routing Algorithm

IBRKM	-	Interval Based Record Keeping Mechanism
ILP	-	Integer Linear Programming
INT	-	Immediate Neighbour Temperature
IP	-	Intellectual Property
LAXY	-	Location based Age Resilient
LEAD	-	Longitudinal Exclusively Adaptive or
LMS	-	Least Mean Square
MPSoC	-	Multi-Processor System-on-Chip
MTTF	-	Mean Time To Failure
NBTI	-	Negative Bias Temperature Instability
NI	-	Network Interface
NoC	-	Network-on-Chip
OE	-	Odd-Even
PD	-	Path Diversity
PDA-FTR	-	Path-Diversity-Aware Fault-Tolerant Routing
PDN	-	Power Delivery Network
PDTM	-	Proactive Dynamic Thermal Management
PE	-	Processing Elements
PG	-	Power Gating
PIR	-	Packet Injection Rate
PSO	-	Particle Swarm Optimization
QoS	-	Quality of Service
RTM	-	Repetitive turn Model
RX	-	Receivers
S&F	-	Store & Forward
SAR	-	Systematic Ageing Routing
SoC	-	System-on-Chip
SRC	-	Source
TADAR	-	Thermal-Aware Directional And Adaptive Routing
TADWR	-	Thermal-Aware Dynamic Weighted Routing
TDDB	-	Time Dependent Dielectric Breakdown
TFSP	-	Thermal-Aware Frequency Scaling Policy
TSV	-	Through Silicon Via

TTAR	-	Traffic- and Throttling-Awareness Routing
TTDR	-	Traffic-and Thermal-Aware Routing
TX	-	Transmitters
UPF	-	Unpaired Function
VCT	-	Virtual Cut Through
VLSI	-	Vary Large Scale Integrated
WB	-	Weight Bucket
WF	-	Weight Fraction

LIST OF SYMBOLS

a	-	Respective Weight
β	-	Change in Weight
C	-	Number of all Parameters
α	-	New weight
ɣ	-	Validity difference
τ	-	Number of packets in queue
λ	-	Packet arrival rate
P_i	-	Packet
L_i	-	Latency
L_{avg}	-	Average Latency
F	-	Flits
i	-	Input buffer
r	-	Router

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CHAPTER 1

INTRODUCTION

1.1 Overview

The increasing packing density of transistors on a chip and the demand for processing for future applications compelled designers to enhance the number of processing elements (PEs) on a chip. Ever increasing number of PE brings an intercommunication problem due to common resources. To reduce interconnection communication delay among PEs, network-on-chip (NoC) was introduced. NoC is flexible and scalable (Wasif *et al.*, 2021). To reduce the end-to-end distance for communication recently, 3D NoC (Three-Dimensional Network-on-Chip) technologies are capable of reducing the interconnection delays by die stacking. 3D NoC-based chip multiprocessors (CMP) are estimated to have higher performance with lower data transmission, power consumption and connection cost (Kunthara *et al.*, 2021).

On the other hand, some factors involved in the degradation of NoC performance include congestion, temporary and permanent faults, ageing, high power density and thermal aggravation. Routers are responsible for generating more heat than memory and processing elements (Taheri *et al.*, 2020). Due to the tier architecture of 3D NoC, it is challenging to reduce the thermal hotspot within the chip as a cooling mechanism that lies on only one side of a chip (Said *et al.*, 2019).

A thermal issue reduces system reliability and puts an extra strain on the on-chip cooling mechanisms. Thermal-aware routing algorithm allows balancing the workload traversing across the on-chip network. In these circumstances, thermal-aware routing algorithms become more substantial to deal with thermal difficulties and diffusion of heat into cooler areas (Taheri *et al.*, 2019). Thermal-aware routing can

reduce thermal hotspots by migrating load to the cooler areas of the chip to achieve thermal optimisation.

The objective of this work is to propose a routing technique that can balance between neighbor temperature and path length, to calculate better paths and reduce the number of path options to choose and an interval-based record keeping mechanism to reduce frequency of control messages transfer for frequently communicating nodes.

1.2 Problem Background

Number of transistors in a single chip is increasing rapidly, this trend will continue in the coming future according to Moore's law. A transistor is a basic element of any computational logic circuit in a microprocessor. Hence increase in number of transistors result in increase in on-chip processing elements. Such rapid growth allows hundreds and thousands of microprocessors to exist on the same chip. This has emerged as a technology consisting of multi-processors on a single chip known as System-on-Chip (SoC). SoC has its own limitations and challenges such as communication, synchronization, delay, routing etc. A new paradigm that helps to facilitate SoC limitations is Network-on-chip (NoC). NoC is communication infrastructure for these hundreds and thousands of microprocessors (E. G. Satish and Ramachandra, 2022).

Recently, 3D-IC (Three-Dimensional Integrated Circuit) technologies are capable of reducing the interconnection delays in die stacking. 3D NoC based chip multiprocessors (CMP) are estimated to have higher performance with lower data transmission power consumption and connection cost (Kunthara *et al.*, 2021). In conventional NoC architecture, each core comprises a processing element (PE), network interface (NI) and a router. NoC concepts and techniques are similar to the well-known and well established domain of computer networks, but are practically impossible to directly reuse all features of traditional computer networks (Hassan and Khaleel, 2018).

Benefits of using NoC paradigm are dedicated communication lines, decentralized controller for communication, support system testing, can operate at different voltage and frequency domain, short wires, arbitrary number of terminals, scalability, guarantees for transfer (Joseph *et al.*, 2019). Along with benefits, NoC has some issues. Researchers are currently focusing on NoC architecture, routing protocol, application mapping, flow control, quality of service, error correction, routing, switching, control schemes etc. (A. Alimi *et al.*, 2021).

The high performance along with balancing load, deadlock-free and livelock-free, as well as fault-tolerant, are the desirable properties of a routing algorithm for NoC. The routing algorithm can be static or dynamic (Li *et al.*, 2018), distributed or source routing and minimal or non-minimal (Safari *et al.*, 2022). Along with packet delivery, researchers have been using routing algorithms to deal with and handle issues like ageing (Wang *et al.*, 2019), temporary and permanent faults (Gabis *et al.*, 2018) and power density (Kumar *et al.*, 2017) to enhance NoC resilience (Charif *et al.*, 2020) and thermal (Salamat *et al.*, 2018) issues.

As the technology scales, temperature effects become more significant, while the designing for performance becomes more difficult. Hence, designers must understand the impact of thermal variations on these systems to reduce hotspots and maintain performance (Lee *et al.*, 2019). Thermal issues are an increasing concern in microelectronics due to increased power density as well as the increasing vulnerability of the system to temperature effects (delay, leakage, reliability) (Lee *et al.*, 2018). To balance temperature distribution, various methods of floor-plan optimisation (Zou *et al.*, 2017), thermal-aware application mapping (Liu *et al.*, 2018) and thermal-aware routing (Ye *et al.*, 2020) have been proposed.

Routers are responsible for being a source of thermal hotspots due to high switching activity. Owing to the tier architecture of 3D NoC, it is challenging to reduce the thermal hotspot within the chip as a cooling mechanism that lies only on one side of a chip. High power density in 3D NoC is responsible for reliability degradation and thermal difficulties. The chip cooling mechanism, also known as a heat sink, is utilised only at one side of the chip in multiple layer 3D NoC; hence, some of the layers away

from the sink have a long heat dissipation path. Therefore, the possibility of thermal hot spots increases especially in layers subsequently further away from the heat sink (Zou *et al.*, 2019).

Cooling mechanisms also known as heat sinks usually exist only on one side of the chip in multi-layer 3D NoC. Hence, layers further away from the heat sink have a higher possibility of thermal hotspots (Shen *et al.*, 2021). These thermal hotspot difficulties and aggravation of the failure mechanism put an extra strain on the cooling cost of the chip and reliability reduction in 3D NoC. Designers need to maintain the performance of the system while reducing thermal hotspots (Lee *et al.*, 2019). To balance temperature distribution, various methods of thermal-aware application mapping (Liu *et al.*, 2018; Abdollahi *et al.*, 2021), floor-plan optimisation (Balakrishnan and Venkatesan, 2021) and thermal-aware routing (Kumar *et al.*, 2017; Dang *et al.*, 2022; Shirmohammadi *et al.*, 2022) have been proposed. Thermal-aware routing algorithms are generally classified into temporal and spatial routing algorithms. Temporal DTM (Dynamic Thermal Management) can dynamically adjust frequencies, voltages or clock cycles to reduce on-chip temperatures (Lee *et al.*, 2018). Temporal DTM results in reduced overall system performance but can regulate system temperatures within a short cooling time. Spatial routing algorithms reduce thermal hotspots by diffusing traffic away from the heated regions (Hsin *et al.*, 2014). Meanwhile, Spatial DTM can manage thermal situations without reducing the speed of the node in terms of frequencies, voltages and clock cycles, hence having a tiny impact on the performance of the system.

Due to the lack of heat sink among the layers and poor traffic distribution, it becomes a challenge to tackle the heat dissipation problem in 3D NoC since the centre of the top layer is more susceptible to thermal problems. One of the effective solutions is to divert traffic away from the centre of the network or to the layers closer to the heat sink. Detoured traffic results in cooler routes yet increased path length. Taking longer routes can raise issues like congestion, power leakage that leads to thermal instability and temporary faults; for instance, ATAR (Dash *et al.*, 2018) has the destination address but does not have the proximity of the location of the destination. Hence, a balance between temperature and path length is required.

Heavy intermediate traffic results in more delays, causes congestion and induces thermal issues. Due to diverse thermal conductance between the intra-layer and inter-layer of the 3D NoC, the relationship between temperature and traffic behaviour among NoC nodes becomes divergent. It is difficult to solve thermal issues without considering traffic conditions in the network. Heavy traffic introduces congestion in the network with low outflows, leading to packets stuck at router buffers waiting for their turn, dissipating heat and causing thermal difficulties. Hence, the design goal is to blend temperature and traffic information along with other routing parameters to make better routing decisions.

It is challenging to reduce traffic in NoC, and it is even harder in the presence of communication overhead for the transfer of vital stats from neighbouring nodes, which is supposed to help and improve routing algorithms. Keeping a record of all successful transactions not only reduces communication overhead for the transfer of vital stats from neighbouring nodes in future but also helps to take better decisions under specified supervision. As multiple paths exit between source and destination, choosing a next neighbour is even more critical.

1.3 Problem Statement

Thermal-aware routing gives an opportunity to balance the workload traversing across the on-chip network. Thermal-aware routing can reduce thermal hotspots by migrating load to the cooler areas of the chip to achieve thermal optimization. In the case of 3D NoC, multiple paths can be taken to reach from source to destination. To moderate the temperatures in the chip and to reduce the power density, available coolest paths or regions can be taken to avoid thermally hotspot paths. To sense temperatures and other vital stats of nodes, enhancing on-chip control traffic is essential. Nevertheless, it is challenging to reduce traffic in NoC and it is even harder in the presence of control traffic overhead, which is supposed to help and improve routing algorithms.

1.4 Research Aim

The aim of this research is to propose a thermal-aware mechanism to distribute temperature evenly throughout the chip, optimise the number of paths between source and destination and maintain an interval-based record mechanism for future decision making.

1.4.1 Research Questions

The research questions of the research are:

1. How to reduce the number of hops considering neighboring temperature?
2. How to reduce the number of throttling routers on thermally unstable paths?
3. How to enhance NoC routing to behave according to network status?

1.4.2 Research Objectives

The objectives of the research are:

1. To propose an adaptive NoC routing algorithm that can balance between neighbour temperature and path length.
2. To decrease the number of throttling routers by proposing optimizing the number of paths options to choose, will reduce network workload on thermally unstable paths.
3. To reduce traffic overhead by proposing an interval-based record keeping mechanism for node cost of NoC.

1.5 Research Scope

This work focuses on routing algorithms under thermal and congestion conditions for 3D fully connected regular mesh network-on-chip. Faults in packets during the transmission, purpose of data transmission as well as temporary and permanent faults in topology are beyond the scope of this work.

1.6 Significance of the Study

Routers provide communication mechanisms for communication among tiles using communication paths. During high traffic situations, packets have to reside in the router's buffers waiting for its turn to cause congestion in the network. Routers are a source of thermal hotspot due to high switching activity and congestion resulting in higher power density. Power density of the router area is higher than power density in intellectual property IP. It is also the fact, higher power consumption of the chip elements results in deteriorating into heat. Routers are responsible for providing communication between IP at a cost of high heat dissipation. Higher heat dissipation for a long period of time may cause throttling in the network. Due to the lack of heat sink among the layers and poor traffic distribution, tackling the heat dissipation problem in 3D NoC is difficult. Since the centre of the top layer in 3D NoC is more susceptible to thermal problems. One of the effective solutions is to divert traffic away from the centre of the network or to the layers closer to the heat sink. Detoured traffic results in cooler routes yet increasing the path length. Heavy intermediate traffic results in more delays, causing congestion and induces thermal issues.

Due to diverse thermal conductance between the intra layer and inter layer of the 3D NoC, the relationship between temperature and traffic behaviour among NoC nodes is divergent. It is difficult to solve thermal issues without considering traffic conditions in the network. Heavy traffic can cause congestion in the network with low outflows, leading to packets stuck at route buffers waiting for its turn, dissipating heat and causing thermal difficulties. The goal of this work is to blend temperature and traffic information along with other routing parameters during the thermal control

period in order to take better routing decisions and also reduce traffic. In 3D NoC, it is challenging to reduce traffic in NoC and it is even harder in the presence of control traffic overhead which is supposed to help and improve routing algorithms. Keeping record of all successful transactions not only reduces communication overhead for transfer of vital stats from neighbouring nodes in future but it also helps to take better decisions under specified supervision. As multiple paths exist between source and destination choosing a next neighbour is even more critical.

1.7 Research Contribution

This study delivers the following contributions.

i) Developed a technique that works well for uniform distribution of heat in the 3D NoC. It also strives for finding the best possible neighbour to reach near to the proximity of destination. It is highly adaptive in the beginning and becomes deterministic just before reaching its destination. Developed technique has performed better in terms of global average delay, total hop counts reduction and thermal profiling under various traffic conditions

ii) A novel thermal-aware dynamic weighted routing technique is developed for dynamic distribution of traffic and heat in the 3D NoC. It allows packets to adaptively select their next neighbour by dynamically adjusting weights of the cost model. Developed technique designed to regulate new weights among the parameters to work according to network situation and need of time. It has performed better in terms of global average delay and thermal profiling under various synthetic traffic conditions.

iii) Developed a novel interval-based record keeping mechanism to reduce communication overhead for transfer of vital stats from neighbour nodes. It works on the history table record of previous transactions carried in the node under validity conditions. Keeping record of all successful transactions not only reduces communication overhead for transfer of vital stats from neighbouring nodes in future but it also helps to take better decisions under

specified supervision. Developed technique has performed better in terms of global average delay; average number of hits vs. misses.

1.8 Organization of Thesis

This thesis is organized as follows:

Chapter 2: This chapter provides an intensive literature review on the study domain and detailed background work on the study domain is discussed.

Chapter 3: Provides the research methodology comprising the overview of the research framework, research plan, and detailed explanation of each of the phases that make up the research activities.

Chapter 4: This chapter provides a strategy for uniform distribution of heat in the 3D NoC. It also strives for finding the best possible neighbour to reach near to the proximity of destination. Moreover, it presents experimental evaluations and performance comparisons under different synthetic traffic patterns, focusing on global average delay, thermal profiling and total hop counts.

Chapter 5: This chapter provides a mechanism for dynamic weight management designed to regulate new weights among the parameters to work according to network situation and need of time. Furthermore, it presents experimental evaluations and performance comparisons under different synthetic traffic patterns, focusing on global average delay and thermal profiling.

Chapter 6: This chapter developed a technique mechanism to reduce communication overhead for transfer of vital stats from neighbour nodes by introducing history based record keeping mechanism. It also presents experimental evaluations and performance comparisons under different synthetic traffic patterns focusing on global average delay and average number of hits vs. misses.

Chapter 7: This chapter provides a detailed analysis of this study. It provides a detailed comparison with all the presented techniques in chapter 4, 5 and 6.

Chapter 8: This chapter discusses the outcome of the current work and possible guidelines for future work.

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LIST OF PUBLICATIONS

Following are the published papers based on the results obtained from the work done in this thesis.

1. Kaleem, M. and Isnin, I. F. Bin (2021) 'A Survey on Network on Chip Routing Algorithms Criteria', in Advances in Intelligent Systems and Computing, pp. 455–466.

2. Kaleem, M. and Isnin, I. F. Bin (2021) 'Thermal-aware Dynamic Weighted Adaptive Routing Algorithm for 3D Network-on-Chip', International Journal of Advanced Computer Science and Applications, 12(11), pp. 342–348.

3. Kaleem, M. and Isnin, I. F. Bin (2022) 'Thermal-aware directional and adaptive routing algorithm for 3D network-on-chip', Indonesian Journal of Electrical Engineering and Computer Science, 27(2), pp. 1051–1061.

4. Kaleem, M. and Isnin, I. F. Bin (2022) 'Interval Based Transaction Record Keeping Mechanism for Adaptive 3D Network-on-Chip Routing', International Journal of Intelligent Engineering and Systems, 15(4), pp. 509-519.