IMPROVED SWITCHED-CAPACITOR-BASED MODULAR T-TYPE INVERTER TOPOLOGY

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DEDICATION

This thesis is dedicated to my parents, teachers, guardians, other family members, and friends for their support throughout my life.

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ABSTRACT

Switched-capacitor (SC) based multilevel inverters (MLIs) have gained great attention in renewable energy applications owing to their self-balancing of the capacitor's voltage and ac voltage boosting. In most existing SCMLIs, the unequal charging and discharging duration of the SCs increase the capacitor's voltage ripple problem**.** Recently, the switched-capacitor-based modular t-type inverter (SCMTI) topology resolved the problem by extending the charging period of all SCs to at least half of the fundamental switching period. However, the SCMTI topology suffers from two main drawbacks: a significantly high number of active switches and the number of switches in the charging loop $N_{path,\ C,}$ which increases the power loss and distorts the quality of the voltage waveform. Hence, this work proposes a new SCMLI topology that retains the good traits of the SCMTI with device count reduction**.** The proposed inverter possesses a low $N_{path,\ C}$, significantly reducing the power loss for higher voltage levels. The proposed inverter is compared with other recent SC topologies to show its superiority. The number of active switches is the lowest compared to the SCMTI at each voltage level of the proposed inverter topology. For the proposed 7-level inverter, the requirement of active switches is only 12, which is 25% less than the SCMTI topology. This will reduce the overall cost and size significantly. The merits and feasibility of the proposed SCMLI are verified through simulation. Then a laboratory prototype is developed and tested for the 7-level module under steady-state and dynamic conditions to validate the simulation model. Finally, PLECs power-loss modelling and conversion efficiency evaluations are provided for the proposed topology, and a comparison is made with the SCMTI topology. The proposed inverter's maximum experimental efficiency is 97.5% at 1.2 kW rated power. The proposed topology's thermal analysis and loss estimation show better efficiency over the SCMTI topology. Further, the results show that the proposed inverter has 1% higher efficiency at a switching frequency of 10 kHz and 3% higher at a switching frequency of 20 kHz. This comparison confirms that the proposed topology has a significant loss reduction than the SCMTI, proving its potential merits.

ABSTRAK

Penyongsang pelbagai aras (MLI) berasaskan kapasitor bersuis (SC) telah mendapat perhatian dalam aplikasi tenaga boleh diperbaharui kerana pengimbangan kendiri voltan kapasitor dan penggalakan voltan keluaran AC. Dalam kebanyakan SCMLI sedia ada, tempoh pengecasan dan nyahcas yang tidak sama bagi SC telah menyebabkan masalah riak voltan kapasitor yang tinggi. Mutakhir ini, topologi penyongsang jenis-t modular berasaskan kapasitor bersuis (SCMTI) telah menyelesaikan masalah tersebut dengan memanjangkan tempoh pengecasan semua SC kepada sekurang-kurangnya separuh daripada tempoh masa asas pensuisan. Walau bagaimanapun, topologi SCMTI mempunyai dua kelemahan utama: iaitu bilangan suis aktif yang tinggi dan bilangan suis dalam gelung pengecasan N_{patch},c, yang akan meningkatkan kehilangan kuasa dan mengherotkan kualiti bentuk gelombang voltan. Oleh itu, penyelidikan ini mencadangkan topologi SCMLI baharu yang mengekalkan ciri-ciri baik SCMTI tetapi dengan pengurangan bilangan peranti. Penyongsang yang dicadangkan mempunyai $N_{patch,C}$ yang rendah, yang akan mengurangkan kehilangan kuasa untuk penjanaan bilangan aras voltan yang lebih tinggi. Penyongsang yang dicadangkan dibandingkan dengan topologi SC lain yang terbaru untuk menunjukkan keunggulannya. Bilangan suis aktif adalah yang paling rendah berbanding SCMTI pada setiap aras voltan topologi penyongsang yang dicadangkan. Bagi penyongsang 7 aras yang dicadangkan, keperluan suis aktif hanya 12, iaitu 25% kurang daripada topologi SCMTI. Ini akan dapat mengurangkan kos dan saiz keseluruhan dengan ketara. Kebaikan dan kebolehlaksanaan SCMLI yang dicadangkan disahkan melalui simulasi. Kemudian, prototaip makmal dibangunkan dan diuji untuk modul 7 aras di bawah keadaan mantap dan keadaan dinamik untuk mengesahkan model simulasi. Akhir sekali, pemodelan kehilangan kuasa menggunakan PLECs dan penilaian kecekapan penukaran dijalankan untuk topologi yang dicadangkan, dan perbandingan dibuat dengan topologi SCMTI. Kecekapan maksimum penyongsang yang dicadangkan ialah 97.5% pada kadaran kuasa 1.2 kW. Analisis terma dan anggaran kehilangan kuasa topologi yang dicadangkan menunjukkan kecekapan yang lebih baik daripada topologi SCMTI. Selanjutnya, keputusan menunjukkan bahawa penyongsang yang dicadangkan mempunyai kecekapan 1% lebih tinggi pada frekuensi pensuisan 10 kHz dan 3% lebih tinggi pada frekuensi pensuisan 20 kHz. Ini mengesahkan bahawa topologi yang dicadangkan telah dapat mengurangkan kehilangan kuasa yang ketara berbanding SCMTI, dan ini membuktikan potensi meritnya.

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LIST OF ABBREVIATIONS

ADC	-	Analogue-To-Digital Converter
ANPC	-	Active Neutral-Point Clamped
CC	-	Crisscross
CG	-	Common-Ground
CHB	-	Cascaded H-Bridge
CMV	-	Common-Mode Voltage
CC	-	Crisscross Capacitor
CS	-	Cross-Switched
DAC	-	Digital-To-Analogue Converter
D2T	-	Dual T-Type
ESR	-	Equivalent Series Resistance
EVs	-	Electric Vehicles
FFT	-	Fast Fourier Transform
FCC	-	Flying-Capacitor Clamped
FC	-	Flying-Capacitor
GTOs	-	Gate Turn-Off Thyristor
HBU	-	Half-Bridge Units
HFAC	-	High Frequency Alternating Current
HVDC	-	High Voltage DC
IGBTs	-	Insulated-Gate Bipolar Transistor
LS	-	Level-Shifted
MLI	-	Multilevel Inverter
MOSFETs	-	Metal-Oxide Semiconductor Field-Effect Transistor
MS	-	Multisource
NPC	-	Neutral-Point Clamped
OC	-	Open-Circuit
PV	-	Photovoltaic
PWM		Pulse Width Modulation
RCP	-	Rapid Control Prototyping
RTI	-	Real-Time Interface

RTW	-	Real-Time-Workshop
RES	-	Renewable Energy Systems
RV	-	Reverse Voltage
SC	-	Switched-Capacitor
SCR	-	Silicon Controlled Rectifier
STATCOMs	-	Static Compensators
SCMTI	-	Switched-Capacitor-Based Modular T-Type Inverter
T3	-	3-Level T-Type
THD	-	Total Harmonics Distortion
TBV	-	Total Blocking Voltage

LIST OF SYMBOLS

N_{path}	-	Number of Conducting Switches in Load Current Path
$N_{path, C,}$	-	Number of Conducting Switches in Charging Path
n	-	Number of SC Units
N_{diodes}	-	Number of Diodes
N_{IGBT}	-	Number of IGBTs
N_{L}	-	Number of Levels
N_{y}	-	Variety of DC Sources
V_{in}	-	Input DC Voltage
V_{o}	-	Output Voltage
I_{o}	-	Output Current
I_{c}	-	Charging Current
$S_{u1, 1}$	-	Switch $u1, 1$ in upper SC unit
$S_{u1, 2}$	-	Switch $u1, 2$ in upper SC unit
$S_{u2, 1}$	-	Switch $u2, 1$ in upper SC unit
$S_{u2, 2}$	-	Switch $u2, 2$ in upper SC unit
$S_{l1, 1}$	-	Switch $l1, 1$ in lower SC unit
$S_{l1, 2}$	-	Switch $l1, 2$ in lower SC unit
$S_{l2, 1}$	-	Switch $l2, 1$ in lower SC unit
$S_{l2, 2}$	-	Switch $l2, 2$ in lower SC unit
S_{T1}	-	Switch T_1 in t-type stage
S_{T2}	-	Switch T_2 in t-type stage
S_{T3}	-	Switch T_3 in t-type stage
S_{T4}	-	Switch T_4 in t-type stage
$V_{o, max}$	-	Maximum output voltage
$V_{Su1, 1}$	-	Standing Voltage of Switch $u1, 1$
$V_{Su1, 2}$	-	Standing Voltage of Switch $u1, 2$
$V_{Su2, 1}$	-	Standing Voltage of Switch $u2, 1$
$V_{Su2, 2}$	-	Standing Voltage of Switch $u2, 2$
$V_{Sl1, 1}$	-	Standing Voltage of Switch $l1, 1$

$V_{Sl1,2}$	-	Standing Voltage of Switch *l*1, 2
$V_{Sl2,1}$	-	Standing Voltage of Switch *l*2, 1
$V_{Sl2,2}$	-	Standing Voltage of Switch *l*2, 2
V_{ST1}	-	Standing Voltage of Switch ST1
V_{ST2}	-	Standing Voltage of Switch ST2
V_{ST3}	-	Standing Voltage of Switch ST3
V_{ST4}	-	Standing Voltage of Switch ST4
a	-	Mid-Point of the DC-Link Capacitors
b	-	Output Terminal
M_a	-	Modulation Index
$V_{o,1}$	-	Peak Output Voltage of the Fundamental Component
N_L	-	Number of Voltage Levels
A_{ref}	-	Amplitude of Sinusoidal Reference Voltage
f_o	-	Output Frequency
f_c	-	Carrier Signal Frequency
$C_{u,1}$	-	Upper SC Unit First Capacitor
$C_{u,2}$	-	Upper SC Unit Second Capacitor
$C_{l,1}$	-	Lower SC Unit First Capacitor
$C_{l,2}$	-	Lower SC Unit Second Capacitor
$C_{d,1}$	-	Upper DC-Link Capacitor
$C_{d,2}$	-	Lower DC-Link Capacitor
$\Delta Q_{cu,1}$	-	Maximum Amount of Electric Charge of $C_{u,1}$
$\Delta Q_{cu,2}$	-	Maximum Amount of Electric Charge $C_{u,2}$
$\Delta Q_{cl,1}$	-	Maximum Amount Of Electric Charge $C_{l,1}$
$\Delta Q_{cl,2}$	-	Maximum Amount Of Electric Charge $C_{l,2}$
$t_1, t_2, t_3, \ldots$	-	The Intersection Points of the Reference and Carriers
φ	-	Phase Angle
$\Delta V_{cu,1}$	-	Voltage Ripple of $C_{u,1}$
$\Delta V_{cu,2}$		Voltage Ripple of $C_{u,2}$
$\Delta V_{cl,1}$		Voltage Ripple of $C_{l,1}$
$\Delta V_{cl,2}$		Voltage Ripple of $C_{l,2}$

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CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter provides an introduction to the thesis, including the research background and problem statement of the research work, highlighting the major challenges associated with SCMTI topology and the related solutions. In the end, the research objectives, the scope of the research work, and the thesis outline are included.

1.2 Research Background

In recent times, the demand for multilevel inverters (MLIs) increased significantly in high-power and medium-voltage industrial applications, particularly for applications in renewable energy sources with grid integration. MLIs are more efficient as compared to classical two-level inverters due to their several advantages: low-voltage-rated power switches, low dv/dt, minimum electromagnetic interference, and high-power handling ability [1, 2]. In general, three types of MLLs are widely used in the industry, i.e., cascaded h-bridge (CHB) MLI [3], neutral-point-clamped (NPC) MLI [4], and flying-capacitor clamped (FCC) MLI [5]. However, these topologies require a large number of power switches and capacitors. The CHB also requires multiple isolated DC sources. Complex control strategies and/or additional circuitry are required for capacitor balancing in the NPC and FCC, especially at higher-level generation. Several hybrid inverter topologies have been derived from classical topologies to reduce the number of components.

Furthermore, these inverter topologies are buck-type. They are not capable of voltage boosting, and their gain is limited to unity, requiring a front-end DC-DC boost converter for a two-stage power conversion structure [6]. Alternatively, step-up AC transformers can also be used with some limitations, such as low efficiency and bulky. It may be noted that these solutions lead to increased size, cost, control complexity, and reduced conversion system efficiency. The voltage boosting capability will be essential when the inverter is designed for a grid-connected photovoltaic (PV) system since the low-input-side DC voltage should be boosted to an acceptable range. Those topologies with 50% or 70% DC bus utilization may need an additional DC-DC boost converter or multiple PV modules to elevate the input voltage (e.g., up to 800 V for connection to a 311 V grid) [7].

Therefore, the switched-capacitor MLI (SCMLI) based on the series/parallel conversion technique is a promising alternative to the classic MLI topologies [2]. SCMLIs have many distinguishing features, including voltage boosting ability, single DC source utilization, self-balancing of the capacitor’s voltage without auxiliary circuits, and simple control techniques. The utilized capacitors are periodically charged from the DC source prior to supplying the load. The SCMLIs achieve voltage boosting in single-stage DC-AC power conversion, eliminating the need for external circuitry. This significantly reduces the number of DC sources and makes the inverter less complicated. However, higher voltage levels can be achieved at the cost of more circuit components. This leads to an increased cost and complex inverter configurations. Therefore, research in SCMLIs is growing by developing more compact topologies with reduced components. It can be observed from the literature that the significant limitations associated with SCMLIs [8] are:

a) Require a significantly high number of switches and capacitors when higher-level output voltage waveforms are intended.

b) Require a large number of conducting switches in the load current path (N_{path}) and charging path ($N_{path, C}$), which distort the quality of the voltage waveform.

c) Require large capacitors to alleviate high voltage ripples and high current spikes due to uneven charging and discharging duration of capacitors in each cycle of operation.

Based on these constraints, a new switched-capacitor-based modular t-type (SCMTI) [9] has been recently proposed to resolve the voltage ripple and current spike issues associated with SCMLIs. The topology successfully addressed these limitations by extending the charging durations of SCs. All the employed SCs can be fully charged for at least half of the fundamental cycle to effectively reduce the capacitors' voltage ripples and current spikes. Additionally, this topology successfully retained all the characteristics of existing SC-based topologies with added benefits of higher gain and self-balancing of the capacitors.

1.3 Problem Statement

Despite the superior characteristics, SCMTI suffers from two main limitations. First, this topology requires a high number of active switches to generate an extended number of voltage levels and voltage gain. Increasing the number of actives necessitates additional gate-driver, dead-band circuits and their related heat sinks, and protection requirements. Moreover, the high number of active switches further increases the computational burden on the controller. This, in turn, contributes to an increase in the cost, size, and control complexity of the SCMTI at higher voltage levels. Thus, impart limitations on system design and practical implementation greatly impact its market penetration. Consequently, careful consideration must be made to ensure that the inverter can still generate good quality output with high efficiency without degrading the implementation cost and complexity issues.

Second, it requires to conduct a large number of power switches in the load current path and to charge the SCs when voltage levels increase. This, in turn, degrades the output voltage quality and decreases the peak amplitude of output waveforms due to voltage drops in conducting switches during their on-state. As the higher magnitude of charging current occurs for a small duration, the current rating of the power switches in the charging paths must be of high value, increasing the total cost and power losses.

1.4 Research Objectives

This thesis proposes a modified switched-capacitor-based inverter with the following objectives:

(a) To reduce the required number of active switches to generate an extended number of output voltage levels.

(b) To reduce the number of switches in current flow paths for producing the highest output voltage and to charge the capacitors when output voltage levels increase.

(c) To analyze the performance and feasibility of the developed topology under various simulation and experimental settings.

1.5 Resfearch Scope

The research in this field focuses on the efforts and initiatives to improve performance and reduce the cost and complexity of inverter circuits. The classical and NPC will be briefly reviewed first. Then switched-capacitor-based MLI structures will be explained in detail with critical analysis. The aim of this thesis is to introduce an improved SC topology that addresses the limitations of SCMTI topology. The prime objectives will be to reduce the number of switches in conduction paths and capacitors charging paths to lower power loss, improve conversion efficiency, and reduce the cost. First, the circuit derivation procedure will be provided on how the proposed topology can be derived from the SCMTI circuit. After a step-by-step process, a generalized topology can be obtained with a lower active switch count while preserving the merits of the SCMTI topology.

The working principle will be provided in detail. This is followed by power loss analysis, design guidelines, and comparative analysis with other SC topologies. The simulation models will be developed in Simulink/PLECs to verify the inverter operation and feasibility through simulation results. The proposed topology will be further tested and validated experimentally. A down-scale prototype will be developed for experimental purposes due to laboratory constraints and safety concerns. Finally, a detailed power loss analysis using PLECs software will be conducted to prove the claim of low power loss and improved efficiency. For power loss and efficiency analysis, the proposed inverter will be tested at high power to confirm its performance.

1.6 Thesis Organization

This thesis includes five chapters that are described as follows:

Chapter 1 introduces the research problem and objectives, emphasizing on the major challenges associated with the SCMTI topology. The chapter also provides the scope of the research and the thesis structure.

Chapter 2 briefly reviews the classical and neutral-point-clamped (NPC) MLIs with a reduced component count. The advantages and limitations of these topologies based on the literature for each topology are also presented. The terminology and assessment parameters of MLIs are briefly discussed. This chapter classifies different SC topologies based on the topological layout of circuits. Various SC topologies are briefly discussed and critically reviewed in this chapter, and a comprehensive quantitative and qualitative analysis is summarized based on different circuit parameters and characteristics.

Chapter 3 presents the step-by-step procedure of the circuit derivation of the proposed topology. The proposed inverter circuit configuration with a detailed explanation of its working principle and modes of operations is introduced. Derivations of equations are provided for power loss and to find the suitable components for the presented topology. The comparative analysis and cost comparison against its benchmarked topology (SCMTI) and recently introduced SCMLIs are included in this chapter.

Chapter 4 provides details about the laboratory setup of the proposed topology. The information about the dSPACE platform setup and the program codes to execute the control algorithms is also provided in this chapter. Some simulation results using high switching frequency are presented. Further detailed experimental results with inverter operated at high and fundamental switching frequencies are provided to show the performance of the proposed topology. The results are compared and analyzed accordingly. Comparison is made with other counterpart topologies in terms of different parameters. Finally, power loss and efficiency analysis for the 7-level proposed and SCMTI topologies are included.

Chapter 5 Conclusion based on the objectives of this research work is presented. Finally, the future scope of this work is also discussed.

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LIST OF PUBLICATIONS

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1. **Saifullah Kakar**, SBM Ayob, A Iqbal, NM Nordin, MSB Arif, S Gore "New asymmetrical modular multilevel inverter topology with reduced number of switches" IEEE Access, vol. 9, pp.27627-27637. Feb 2022. **DOI:**10.1109/ACCESS.2021.3057554. **(Q2, IF: 3.467)**

2. **Saifullah Kakar**, MSB Arif, SM Ayob, NM Nordin, Saad Mekhilef, Mehdi Seyedmahmoudian, Alex Stojcevski "An improved seven-level switched-capacitor-based neutral-point-clamped inverter" Frontiers in Energy Research vol. 10. Jul 2022. **(Q3, IF: 3.85)**

3. **Saifullah Kakar**, SM Ayob, MSB Arif, NM Nordin, Z Daud, R Ayop "A new multilevel inverter topology based on switched-capacitor technique" International Journal of Power Electronics and Drive Systems vol. 12(1). Jul 2020. DOI: http://doi.org/10.11591/ijpeds.v12.i1.pp627-636. **(Indexed by SCOPUS)**

4. **Saifullah Kakar**, SM Ayob, MSB Arif, NM Nordin, Z Daud, R Ayop "A generalized switched-capacitor-based modular t-type inverter topology with reduced switch count" International journal of circuit theory and applications.

5. **Saifullah Kakar**, SM Ayob, SS Lee, NM Nordin, MS Arif, R Barzegarkhoo, Y.P. Siwakoti. "A Common-Ground-Type Five-Level Inverter with Dynamic Voltage Boost". *Electronics* 2022, *11*(24), 4174; https://doi.org/10.3390/electronics11244174. **(IF=2.69)**

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1. **Saifullah Kakar**, SM Ayob, NM Nordin, SS Lee, MSB Arif "Switched-Capacitor-Based Modular T-Type Inverter with Reduced Switch Count" in 2020 IEEE International Conference on Power and Energy (PECon), 165-170. DOI**:** 10.1109/PECon48942.2020.9314519. **(Indexed by SCOPUS)**