

PERFORMANCE EVALUATION OF GRAPHENE BASED PRIORITY  
ENCODER FOR ANALOG TO DIGITAL CONVERTER APPLICATION

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## ABSTRACT

Continuous scaling and performance optimization on transistors, the basic building blocks for every electronic devices are highly anticipated to fulfil the rocketing technology. By 2021, the transistors were manufactured with 5nm-scale technology by a numbers of chip manufacturer, this significantly increase the number of transistor per area in a chip. In the future, 3nm and 1nm technology will be discovered. The continuous size shrinking will impact the performance degradation on the conventional metal-oxide semiconductor field-effect transistors (MOSFETs). The International Roadmap Device Semiconductor (IRDS) have several alternative materials such as silicon nanowire, carbon nanotube (CNT), graphene, graphene nanoribbon (GNR) to continue the journey of continuous scaling. Apart from that, the advance device architecture such as FinFET, Multiple gate MOSFET, Gate-all-around FET, Vertical MOSFET, SOI MOSFET also been introduced. The aim of this work is to design a priority encoder by adopting GNR-FETs-based model and FinFET CMOS-based model. Performance on propagation delay, average power, power-delay product (PDP) and energy delay product (EDP) were evaluated between these two models. The designed priority encoder was then implemented into a flash analog to digital converter to evaluate its functionality. All designs and performance evaluations was carried out by using HSPICE simulation software. Through simulation, it is found that the flash analog to digital converter behave accordingly when the GNR-FETs-based priority encoder is applied. In addition, the propagation delay exhibit 61% improvement compared to FinFET CMOS counterpart. In terms of PDP and EDP exhibit 57% and 83% improvement respectively. The outcome of this study is intriguing and can be further implement to other application.

## ABSTRAK

Pengurangan size dan pengoptimuman prestasi yang berterusan pada transistor, blok asas bagi setiap peranti elektronik sangat dinantikan untuk memenuhi teknologi meningkat dengan pantas. Menjelang 2021, transistor dapat dihasilkan dengan teknologi 5nm oleh pelbagai pembuat. Oleh itu, bilangan transistor setiap chip meningkat secara ketara. Pada masa akan datang, teknologi 3nm dan 1nm akan ditemui. Pengecutan saiz berterusan akan mempengaruhi penurunan prestasi dan menghadapi halangan yang berterusan pada MOSFETs. IRDS mempunyai beberapa bahan alternatif seperti nanowire silikon, nanotube karbon nanotube (CNT), graphene, graphene nanoribbon (GNR) untuk meneruskan penyelidikan penskalaan yang berterusan. Selain itu, seni bina peranti canggih seperti FinFET, Multiple gate MOSFET, Gate-all-around FET, Vertical MOSFET, SOI MOSFET juga diperkenalkan. Matlamat kerja penyelidikan ini adalah untuk merancang pengkod prioriti dengan menggunakan model berasaskan GNRFETs dan model berasaskan CMOS FinFET. Prestasi kelajuan penghantaran data, penggunaan kuasa, PDP dan EDP akan dinilai antara kedua-dua model ini. Pengkod prioriti yang dirancang telah diaplikasi ke dalam litar penukar analog ke digital untuk penilaian fungsi. Semua reka bentuk dan penilaian prestasi telah dilakukan dengan menggunakan perisian simulasi HSPICE. Melalui simulasi, didapati bahawa penukar analog ke digital berfungsi dengan sewajarnya apabila penekod prioriti berasaskan model GNRFETs diaplikasikan. Di samping itu, prestasi kelajuan penghantaran data mempamerkan peningkatan sebanyak 61% berbanding dengan model FinFET. Dari segi PDP dan EDP, masing-masing menunjukkan peningkatan sebanyak 57% dan 83%. Hasil Kajian ini didapati menarik dan boleh diimplementasikan selanjutnya kepada aplikasi lain

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## LIST OF ABBREVIATIONS

GO	Graphene Oxide
rGO	Reduced Graphene Oxide
SWCNTs	Single-Walled Carbon Nanotubes
MWCNTs	Multi-Walled Carbon Nanotubes
GNR	Graphene Nano Ribbon
CVD	Chemical Vapour Deposition
FET	Field Effect Transistor
MOSFET	Metal-oxide Semiconductor Field Effect Transistor
G NRFETs	Graphene Nano Ribbon Field Effect Transistor
PUN	Pull-Up Network
PDN	Pull-Down Network
ADC	Analog to Digital Converter
PDP	Power Delay Product
EDP	Energy Delay Product

# CHAPTER 1

## INTRODUCTION

### 1.1 Problem Background

Moore's Law refers to the number of transistors on a single integrated circuit (IC) doubles approximately every two years. The number of transistors of a single IC in 1970 was around 2000. While this number was grown up to 10 billion when approaching the year of 2020 [1]. The speedy ramping up of technology in the past decades increase the demand of the electronic devices drastically. Optimization on these electronic devices in terms of power, speed, and size always the most trending research directions to fulfil the needs of societies. Silicon has been widely used in semiconductor fabrication due to its stability, low cost and some unique characteristics. However the further optimization and miniaturization on the silicon-based electronic devices have led to some performances degradation in the Beyond Moore era. One of the main challenge on producing more competitive devices in the aspects of power, speed and size is the short channel effect in the silicon MOSFET. Short channel effect is the scenario that happened when the channel length is smaller than the sum of source and drain depletion region. The side effect including instability of the threshold voltage. The instability of the threshold voltage will impact the performance of transistor when doing the switching activities.

Other than the conventional MOSFET, there are also some other advanced device architectures been introduced, such as, FinFET, Multiple Gate MOSFET, Gate-all-around FET, Vertical MOSFET, Silicon-on-Insulator MOSFET and etc. All of the advance architectures are trying to resolving the issue faced during miniaturization of MOSFET.

The key aim is still to achieve a smaller in scale and higher performance device in future. This is to fulfil the speedy digitalization of the current world and future. These high speed devices took a very important role in telecommunication, Internet of things and etc. A borderless world that allowing individuals to access or share information between each other can be achieve with all of this aid.

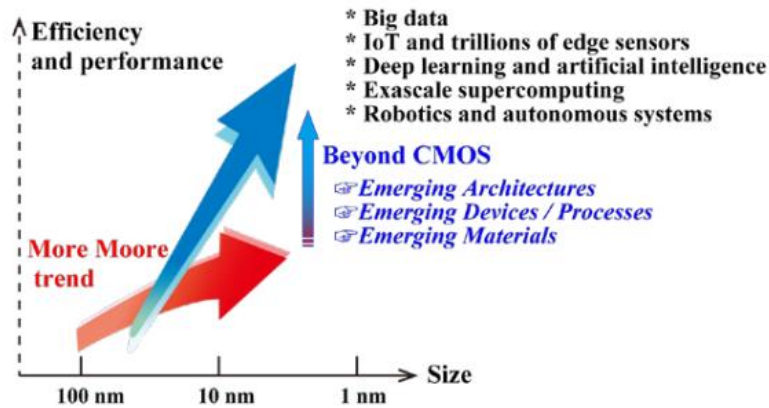


Figure 1.1: More Moore trend, Beyond CMOS and Applications [2].

## 1.2 Problem Statement

Silicon as the main semiconductors raw materials has led to some performance degradation in the Beyond Moore era. Power consumption of electronics devices been increased in this era of digitalization, to cope with variety of functions and capabilities per user's needs. Demand on data transmission speed between electronics devices in analog or digital format been surged to handle massive of data in recent years. The research questions are:

- How much of the speed improvement in terms of propagation delay of GNRFETs-based priority encoder compare to Silicon FinFET-based priority encoder?
- How much of the power improvement of GNRFETs-based priority encoder compare to Silicon FinFET-based priority encoder?
- How does a GNRFETs-based priority encoder impact the functionality of a Flash ADC?

### **1.3 Research Objectives**

This research focus on the utilization design on transistor level circuit, functional simulations and performance evaluations. The objectives are:

- To design a priority encoder based on graphene nanomaterial.
- To test the functionality of the graphene-based encoder in analog to digital converter.
- To benchmark the performance of 16nm GNR-FETs-based ADC with 16nm Silicon FinFET-based ADC.

### **1.4 Project Scope**

HSPICE simulator will be used for functional simulation and performance evaluation of the designed circuit. The SPICE model for 16nm Silicon FinFET is adopted from Predictive Technology Model (PTM) [3]. While the SPICE model for 16nm GNR-FETs is adopted from Chen et. al [4]. The designed priority encoder will apply to Flash ADC circuit to verify its functionality. The figure of merit in this project include propagation delay, average power consumption, power delay product (PDP), energy-delay product (EDP). This study did not consider the effect of interconnect.

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