HARDWARE/SOFTWARE CO-DESIGN OF TWO-STAGE SMART ARRHYTHMIA CLASSIFIER BASED ON MULTI-PROCESSOR FIELD PROGRAMMABLE GATE ARRAY SYSTEM-ON-CHIP

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DEDICATION

This thesis is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to mymother, who taught me that even the largest task can be accomplished if it is done onestep at a time.

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ABSTRACT

Cardiovascular diseases are the top cause of deaths in Malaysia since 2000. Arrhythmia is one of the precursors for cardiovascular disease that can be diagnosed via electrocardiogram (ECG). This research proposes an embedded multi-processor system-on-chip (MPSoC) architecture of in-house smart arrhythmia classifier using Nordic NRF5282 microcontroller unit (MCU) and DBM Cyclone V system-on-chip SoC (DBM SoC). The MCU houses Bluetooth low energy (BLE) and a 64 MHz Cortex-M4 processor. DBM SoC consists offield programmable gate array (FPGA) with logic elements (LE) and a hardcore ARM Cortex A9 processor that can run at 800MHz frequency. Hardware accelerator for compute intensive Fast Fourier Transform (FFT) is implemented in FPGA using soft intellectual property (IP) provided by vendor Intel. The high-performance DBM SoC will execute arrhythmia classification while the MCU act as master processor that are able to power cycle DBM SoC. Bluetooth communication between MCU and external mobile phone allow user to control DBM SoC, ECG acquisition via mobile phone. Sanity verification, timing performance benchmarking and power measurement are performed on the proposed MPSoC system. Results show that the proposed MPSoC system is able to classify an ECG signal into 6 types of arrhythmias namely Atrial Fibrilaltion (AFib), Ventricular Tachycardia (VTach), premature atrial contractions (PAC), premature ventricular contractions (PVC), left bundle branch block (LBBB), right bundble branch block (RBBB) and normal sinus rhythm (NSR). The proposed system is also able to classify a 10 seconds ECG input data within 1 second, equivalent to real-time detection performance. Results also show the battery-powered MPSoC platform consumes less power in idle mode when the DBM SoC is turned off. The battery life is greatly improved which increase portability and usability as well.

ABSTRAK

Penyakit kardiovaskular adalah salah satu penyakit pembunuh utama di Malaysia sejak 2000. Aritmia adalah salah satu punca penyakit kardiovaskular yang boleh didiagnosis dengan peranti elektrokardiogram (ECG). Projek ini membentangkan reka bentuk dalaman aritmia pengelas dengan kaedah seni bina berbilang pemproses system-on-chip (MPSoC) menggunakan unit mikropengawal Nordic NRF52832 (MCU) dan DBM Cyclone V system-on-chip (DBM SoC). MCU menpunyai Bluetooth low energy (BLE) dan 64 MHz pemproses Cortex-M4. DBM SoC menpunyai Field Programmable Gate Array (FPGA) dengan unsur logik (LE) dan pemproses ARM Cortex A9 yang dapat beroperasi di 800 MHz. Pemecut perkakasan Fast Fourier Transform (FFT) yang menggunakan Intel FFT IP telah dilaksanakan. DBM SoC yang berpretasi tinggi akan melaksanakan pengelasan aritmia manakala MCU yang bertindak sebagai pemproses utama boleh mengawal DBM SoC. Komunikasi Bluetooth antara MCU dan telefon bimbit membolehkan pengguna mengawal DBM SoC, pemerolehan ECG melalui telefon bimbit. Pengesahan kewarasan, penanda aras prestasi masa dan pengukuran kuasa dilakukan pada sistem MPSoC yang dicadangkan. Sistem yang dicadangkan juga boleh mengklasifikasikan data input ECG 10 saat dalam masa 1 saat, bersamaan dengan prestasi pengesanan masa nyata. Keputusan juga menunjukkan platform MPSoC berkuasa bateri menggunakan lebih sedikit kuasa dalam mod melahu apabila SoC DBM dimatikan. Hayat bateri bertambah baik yang meningkatkan kemudahalihan dan kebolehgunaan juga.

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LIST OF ABBREVIATIONS

CVD	-	Cardiovascular Diseases
AFib	-	Atrial Fibrillation
VTach	-	Ventricular Tachycardia
PAC	-	Premature Atrial Contractions
PVC	-	Premature Ventricular Contractions
LBBB	-	Left Bundle Branch Block
RBBB	-	Right Bundle Branch Block
NSR	-	Normal Sinus Rhythm
MCU	-	Microcontroller Unit
MPSoC	-	Multiprocessor system-on-chip
BLE	-	Bluetooth Low Energy
FPGA	-	Field Programmable Gate Array
FFT	-	Fast Fourier Transform
LE	-	Logic Elements
RTC	-	Real-time Clock
ECG	-	Electrocardiogram
AV	-	Atrialventricular
SA	-	Sinoatrial
SCA	-	Sudden Cardiac Arrest
SCD	-	Sudden Cardiac Death
CPU	-	Central Processing Unit
GPU	-	Graphical Processing Unit
SoC	-	system-on-chip
OCCA	-	On-chip Communication Architecture
MPU	-	Microprocessor Unit
PLL	-	Phase Lock Loop

DMA	-	Dynamic Memory Access
EMACS	-	Ethernet Media Access Controller
OTG	-	On-The-Go
MMC	-	Multimedia Card
SPI	-	Serial Peripheral Interface
I2C	-	Inter-integrated Circuit
CAN	-	Controller Area Network
UART	-	Universal Asynchronous Receiver Transmitter
DAP	-	Debug Access Port
ETR	-	Embedded Trace Router
HDL	-	Hardware Descriptive Language
CU	-	Control Unit
DPU	-	Datapath Unit
FSM	-	Finite State Machine
ADC	-	Analog to Digital Converter
PIO	-	Peripheral Input-Output
OS	-	Operating System
LUT	-	Look-up Table
VF	-	Ventricular Fibrillation
FF	-	Flip Flop
RAM	-	Random Access Memory
BRAM	-	Block RAM
SoCEDS	-	System-on-Chip Embedded Design Suite
GSRD	-	Golden System Reference Design
SCP	-	Secure Copy
EDA	-	Electronic Design Automation
HPS	-	Hard Processor System
TP	-	True Positive
TN	-	True Negative

FP	-	False Positive
FN	-	False Negative
ALM	-	Adaptive Logic Module
CMSIS	-	Common Microcontroller Software Interface Standard
NN	-	Neural Network
DSP	-	Digital Signal Processing
HLS	-	High Level Synthesis

CHAPTER 1

INTRODUCTION

1.1 Project Background

Based on Department of Statistics Malaysia, ischemic heart diseases contributed highest mortalities in Malaysia in 2019 compared to other causes of death, such as pneumonia and cerebrovascular diseases [1]. In fact, ischemic heart diseases and stroke are the top cause of death globally since 2000 [2]. Figure 1.1 illustrates 16% of the total deaths are caused by ischemic heart diseases in Malaysia. This proves that cardiovascular diseases (CVD) remains the top killers since 2000 consecutively.

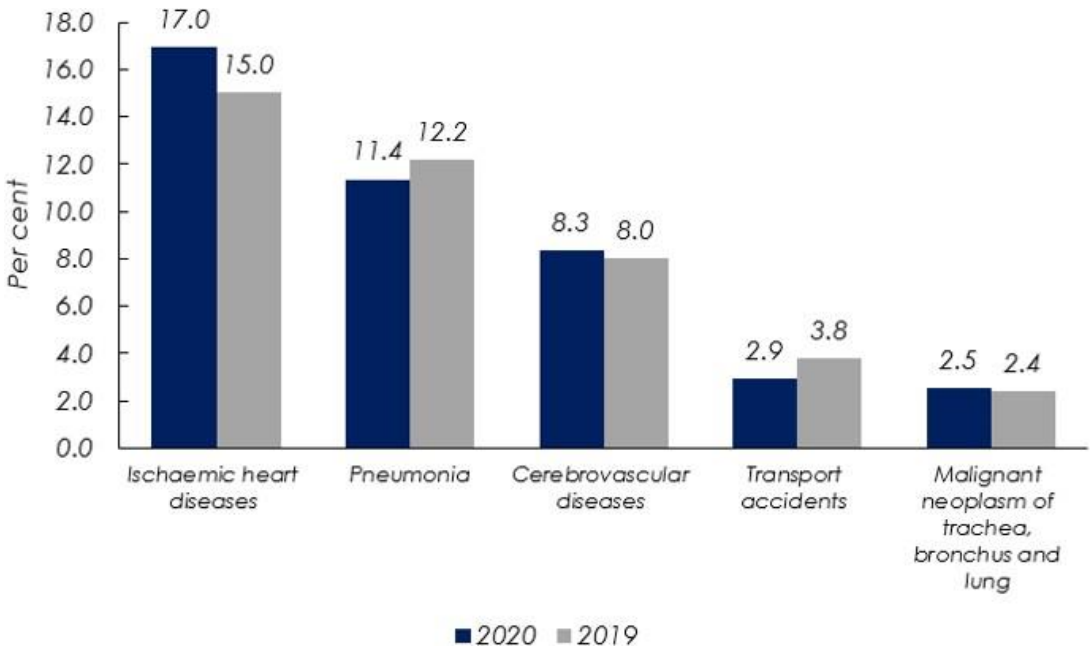

Figure 1.1 Top causes of death in Malaysia, 2018 & 2019 [1].

Arrhythmia, the precursor of CVDs, is the abnormal rhythm of the heartbeat that caused by irregularities at the cardiac conduction of electrical signals [3, 4]. Common arrhythmias such as ventricular tachycardia can lead to ventricular fibrillation and eventually sudden cardiac arrest [4, 5]. Patients with atrial fibrillation has higher

probabilities of evolving stroke [6]. Arrythmia has obscure symptoms and most patients neither aware of it nor take frequent heart monitoring test. It can only be detected via electrocardiogram (ECG) analysed by cardiologist. Hence, CVDs are also known as the silent killers. The best approach to mitigate the mortality caused by CVDs is via frequent heart monitoring to detect any abnormalities in heart rhythm.

ECG is a non-invasive procedure which measures electrical signals generated by the heart chamber during cardiac cycle [7]. It provides essential details on the heart's rhythm. Cardiologists perform diagnosis based on the signal waveform generated by the heart. However, ECG devices are cost expensive and most of them only acquire impulses but still require professionals to analyse the data. The classification performed is not standalone. Generally, ECG devices available in the market that provide classification functionality, usually do not have state-of-the-art classification algorithm or do not have the capabilities to detect multiple arrhythmias. One example is Holter monitor which although are portable, it performs ECG acquisition solely and the data has to be processed at hospital afterwards [8]. Hospitals do possess advance ECG equipment but those devices are bulky, costly and consume high power.

1.2 Problem Statement

Thoughfield programmable gate array system-on-chip (FPGA SoC) provides the capability of running compute intensive algorithm with superior performance in short design cycle [9, 10], the power consumption is higher compared to application-specific integrated circuit (ASIC). Low power design is a critical design attribute in portable device as the power source depends solely on the built-in battery [11]. Hence FPGA SoC is suitable for prototyping within short design cycle or devices who are constantly connected to a wall socket. FPGA SoC requires constant power fed to enable continuous arrhythmia algorithm processing. This put a strain on the battery and generates heat which cause discomforts to user.

Existing device in market able to perform ECG classification using microcontroller which utilize low power consumption and dissipate less heat compared

to FPGA SoC. However, the microcontroller devices are using less powerful processor cores that are not able to perform sophisticated algorithm for higher detection accuracy [10]. In addition, the existing devices are only able to detect single arrhythmia which are not practical as there are more than a few arrhythmias which are life-threatening. Some ECG devices, such as Holter monitor, are not standalone and only acquire ECG signals that is needed to transfer to external computing power forfinal classification. To leverage the low power dissipation of microcontroller coupled with high compute performance of FPGA-SoC, multi-processor architecture is explored. Multiple arrhythmia classifications based on machine learning for heart ECG monitoring are a complex algorithm which require efficient computing architecture, such as multi-processor embedded system to perform real-time processing performance.

To reduce power consumption, compute-intensive with higher power consumption processing block is switched offwhen the device is in hibernate state where background processes such as Bluetooth, power monitoring and data logging are executed by the main processor to ensure basic interaction with user. A systematic approach is required to develop complex master-slave multi-processor embedded system processing architecture that involve embedded OS kernel as well as communication bus protocol between master and slave peripherals. Data integrity is important as well in multi-processor architecture as the clocks are running at different frequencies. Hence, a robust communication bus protocol ensures the data transfer between processors is valid and uncorrupted.

Multiple arrhythmia classifications based on machine learning are complicated and occupied all the resources in single processor. An efficient computing architecture is required to perform classification algorithm as well as peripheral processes (Bluetooth, RTC etc.) simultaneously. SoC FPGA houses a hard processor system (HPS) which consists of a powerful physical processor such as Cortex ARM and FPGA portion which consists of logic elements for hardware accelerator implementation to improve performance but at the cost of higher power consumption compared to microcontrollers. Existing algorithm implemented on development board requires power supply from power outlet which is bulky and reduces portability. Hence, this project proposes an ECG monitoring equipment for multiple arrhythmias detection based on multi-

processor system-on-chip (MPSoC) architecture technology targeting general public. The prototype will consume less power, have Bluetooth capabilities for edge user usability and able to detect 6 types of arrhythmias in real time performance with high accuracy. Functionality verified prototype will retain the same classification capabilities albeit consume less power. Patients are referred to hospital for further diagnosis and follow-up treatment.

1.3 Objective

Based on the aforementioned problem statement, this project aims to design a device with power optimization capable of executing multiple arrhythmia classifications:

1. To design a smart arrhythmia classifier based on master-slave method on multiprocessor-based embedded system with combination of Nordic ARM microprocessor, Cyclone V FPGA-SoC and battery module onboard.
2. To develop a proof-of-concept lab demonstration prototype by integration of the smart arrhythmia classifier in (1) with in-house mobile app to form the complete heart monitoring application.
3. To conduct system functionality verification and performance measurement in term of timing and power.

1.4 Project Scope

The system prototyping platform is targeted for a development board which implements multi-processor architecture that houses Nordic nRF52832 chip which act as the master SoC and a DBM Cyclone V FPGA SoC chip as the slave SoC. The processing architecture is designed based on hardware/software co-design technique. The overall system functionality is tested with ECG signals generated from Fluke ProSim 3 patient simulator. Six types of arrhythmias such as Afib, Vtach, PAC, PVC, LBBB, RBBB and normal sinus rhythm. This project focuses on implementation

technology, there are no changes required on algorithm processingflow. The algorithms are ported over from the previous research [12, 13]. On the slave processor, HPS houses arrhythmia classifier algorithm and FFT software driver. FPGA portion houses FFT hardware accelerator. Android application is modified to illustrate real-time ECG signal display, arrhythmia classification result, heart rate display and prototype's battery display. Figure 1.2 below depicts the scope of work.

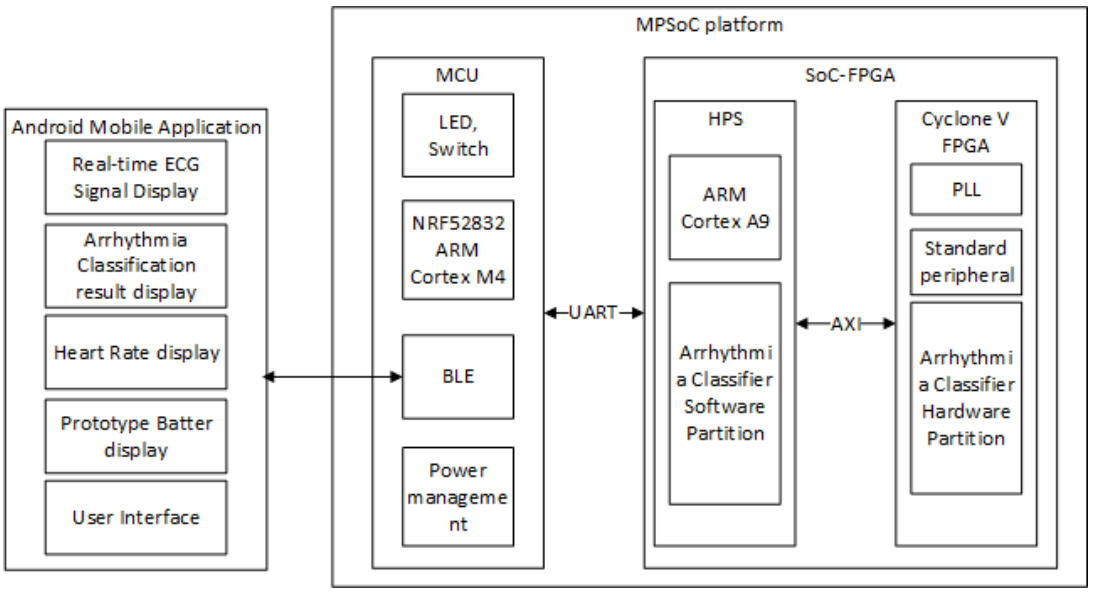

Figure 1.2 Project Scope.

1.5 Project Report Organization

This project report is divided into six chapters where thefirst chapter has discussed the project background, problem statement, project objectives and scope of work. The second chapter presents the related knowledge background as well as the related work by other researchers in recent years. The project methodology chapter discusses the research and design workflow with associated design tools. Chapter 4 discusses the proposed MPSoC implementation in detail. All the result will be presented in Chapter 5 with analysis discussion. Finally, Chapter 6 concludes this project and recommendation for future works.

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