PARAMETER VARIATIONS OF 20 NM GAAS JUNCTIONLESS-GATE-ALL-AROUND FIELD-EFFECT TRANSISTOR WITH QUANTUM MECHANICAL EFFECTS

MUHAMMAD FAIDZAL BIN MOHAMAD RASOL

UNIVERSITI TEKNOLOGI MALAYSIA

PARAMETER VARIATIONS OF 20NM GAAS JUNCTIONLESS-GATE-ALL-AROUND FIELD-EFFECT TRANSISTOR WITH QUANTUM MECHANICAL EFFECTS

MUHAMMAD FAIDZAL BIN MOHAMAD RASOL

A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Philosophy

School of Electrical Engineering
Faculty of Engineering
Universiti Teknologi Malaysia

SEPTEMBER 2021

ACKNOWLEDGEMENT

In preparing this thesis, there are many people who I would like to express my appreciation for their helps and encouragements that they have given to me over the past one year. First and foremost, I wish to express my sincere appreciation to my project supervisor and co-supervisor, Dr. Zaharah Binti Johari and Dr Rashidah Binti Arsat, for encouragement, contributed towards my understanding and thoughts, guidance, critics, motivations and friendship. Furthermore, my special appreciation to Dr Fatimah Khairiah Binti Abd. Hamid for her guidance, advices and motivation. My humble thanks also credit to Prof Dr. Razali Bin Ismail for believing in me and encourage to pursue my study. Nonetheless, my appreciation goes to Nanoelectronics Laboratory staff, En Mohd Zulkifli for his favors in accommodating very convenient lab environment. I would like to acknowledge the support I received from research members who sharing their valuable ideas and recommendation to complete my research. I also hereby gratefully honoured to the Research Management Centre (RMC) of Universiti Teknologi Malaysia for providing and excellent research environment and to the research grant from GUP 16J29 and CRG 05G00 for the financial support. On a personal note, I would like to thanks my family especially my mother, Robiah Binti Hasim and my eldest brother, Mohd Rashidi for their support, prayers and motivation in completing this thesis. My sincere appreciation also extends to Yusril Ehza Mahendra, Khairunnisa, Fatien, all my colleagues, Majlis Felo, and everyone who support me indirectly. It is not possible to list all of them in this limited space.

ABSTRACT

The scaling down of nanoelectronic device dimension beyond the Moore's Law era has introduced the use of new material and device architecture of Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). The use of nanomaterial and advanced device architecture allows the mitigation of the short channel effect at narrow MOSFET gate length. The purpose of this research is to study the performance of 20nm GaAs Junctionless-Gate-All-Around (JGAA) transistor incorporating the quantum mechanical effect. This device performance is then compared with conventional silicon material for comparative study. The device is designed, simulated and characterized using Technology Computer Aided Design (TCAD) from Sentaurus. The electrical parameter extracted from the current-voltage (I-V) characteristic includes the threshold voltage (V_{th}), drive current (I_{on}) and leakage current (I_{off}). For JGAA MOSFET, the geometry scaling in radial direction includes the thickness of the channel radius and oxide layer, which can contribute to quantum effect. The charge distribution along the mid-region of the device is extracted to observe the carrier movement profile. Through simulation, it is proven that at shorter gate length, GaAs channel JGAA transistor exhibit better performance in terms of the on current and threshold voltage. Further evaluation shows that the classical model, the drift-diffusion model (DDM), which is the default carrier transport model, failed to incorporate the quantum effect, which is found to be non-negligible, particularly when the channel radius and oxide thickness is made less than 10nm and 14nm respectively. The inclusion of the quantum effect is based on the Density Gradient Model (DGM). It is found that the quantum effect significantly affects the drive current and leakage current by 28% for GaAs when the channel radius is scaled down less than 5nm, while minimal effect can be seen on the threshold voltage. Due to the considerable quantum effect, the carrier distribution around the channel moves further away from the semiconductor/oxide interface to the centre of the channel. This work highlight 90% increment on the on-current for GaAs JGAA MOSFET compared to silicon JGAA MOSFET and further shows the flexibility of III–V compound materials as potential materials to replace the conventional silicon. The results also indicate the necessity of considering the quantum model to generate accurate data for the projection of future nanoelectronics devices. It can be seen that this work is in agreement with other results obtained using silicon as channel for junctionless MOSFET and close with International Roadmap for Devices and Systems (IRDS) target for low power application.

ABSTRAK

Pengecilan dimensi peranti nanoelektronik yang melangkaui era Hukum Moore telah memperkenalkan penggunaan bahan baru dan seni bina peranti semikonduktor oksida logam transistor kesan medan (MOSFET). Penggunaan bahan nano dan seni bina peranti termaju membolehkan pengurangan kesan saluran pendek (SCEs) pada panjang pintu MOSFET yang sempit. Tujuan penyelidikan ini adalah untuk mengkaji prestasi transistor 20nm GaAs Junctionless-Gate-All-Around (JGAA) yang menggabungkan kesan mekanikal kuantum. Prestasi peranti ini kemudian dibandingkan dengan bahan silikon konvensional untuk kajian perbandingan. Peranti ini direka, disimulasikan dan dicirikan menggunakan Technology Computer Aided Design (TCAD) dari Sentaurus. Parameter elektrik yang diekstrak dari ciri arus–voltan (I-V) meliputi voltan ambang (V_{th}), arus salir (I_{on}) dan arus bocor (I_{off}). Untuk JGAA MOSFET, penskalaan geometri dalam arah radial merangkumi ketebalan jejari saluran dan lapisan oksida yang boleh menyumbang kepada kesan kuantum. Taburan cas di sepanjang kawasan tengah peranti diekstrak untuk memerhatikan profil pergerakan pembawa. Melalui simulasi, terbukti bahawa pada panjang pintu yang lebih pendek, transistor GaAs Junctionless-Gate-All-Around (JGAA) menunjukkan prestasi yang lebih baik dari segi arus salir dan voltan ambang. Penilaian lebih lanjut menunjukkan bahawa model klasik, model drift-diffusion (DDM) yang merupakan model pengangkutan pembawa gagal menunjukkan kesan kuantum yang didapati tidak dapat diabaikan terutamanya apabila ketebalan jejari saluran dan lapisan oksida masing-masing kurang dari 10nm dan 14nm. Rangkuman kesan kuantum adalah didasarkan pada model kecerunan ketumpatan (DGM). Ia mendapati bahawa kesan kuantum mempengaruhi arus salir dan arus bocor secara signifikan sebanyak 28% untuk GaAs ketika jejari saluran dikecilkan kurang dari 5nm, sementara kesan minimum dapat dilihat pada voltan ambang. Oleh kerana kesan kuantum yang besar, taburan pembawa di sekitar saluran bergerak lebih jauh dari antara muka semikonduktor/oksida ke pusat saluran. Kajian ini menonjolkan kenaikan 90% pada arus salir untuk GaAs JGAA MOSFET berbanding dengan Silicon JGAA MOSFET dan seterusnya menunjukkan kelenturan bahan kompaun III-V sebagai bahan berpotensi untuk menggantikan silikon konvensional. Hasilnya juga menunjukkan perlunya mempertimbangkan model kuantum untuk menghasilkan data yang tepat untuk unjuran peranti nanoelektronik masa depan. Ini dapat dilihat bahawa kajian ini sesuai dengan hasil lain yang diperoleh menggunakan silikon untuk junctionless MOSFET dan hampir dengan sasaran panduan antrabangsa untuk peranti dan sistem (IRDS) untuk aplikasi kuasa rendah.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

CMOS	-	Complementary Metal-Oxide-Semiconductor
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect-Transistor
GAA	-	Gate-All-Around
JGAA	-	Junctionless-Gate-All-Around
IRDS	-	International Roadmap of Devices and Systems
NTRS	-	National Technology Roadmap for Semiconductors
ITRS	-	International Technology Roadmap for Semiconductors
I-V	-	Current Versus Voltage
MATLAB	-	Matrix Laboratory
3D	-	Three Dimension
2D	-	Two Dimension
1D	-	One Dimension
SCEs	-	Short Channel Effects
DIBL	-	Drain Induced Barrier Lowering
TCAD	-	Technology Computer Aided Design
QME	-	Quantum Mechanical Effect
SiO_2	-	Silicon Oxide
GaAs	-	Gallium Arsenide
GaN	-	Gallium Nitride
InAs	-	Indium Arsenide
CNT	-	Carbon Nanotube
IoT	-	Internet of Things
GUI	-	Graphical User Interface
BTBT	-	Band To Band Tunnelling

LIST OF SYMBOLS

I_{off}	-	Leakage Current @ Off-state Current
I_{on}	-	Drive Current @ On-state Current
V_{th}	-	Threshold Voltage
SS	-	Subthreshold Slope
λ	-	Natural Length
χ	-	Electron Affinity
Ø	-	Electrostatic Potential
μ_n	-	Electron Mobility
h	-	Plank Constant
q	-	Electronic Charge
n	-	Electron Densities
p	-	Hole Densities
N_D	-	Ionised Donors Concentration
N_A	-	Ionised Acceptor Concentration
ρ_{Trap}	-	Concentration of Surface Trap
J_n	-	Electron Current Density
E_C	-	Conduction Band Energy
T_n	-	Electron Temperature
m_n	-	Electron Effective Mass
K	-	Boltzmann Constant
N_C	-	Conduction Band Density of States
E_{F_n}	-	Fermi Level Energy
V_d	-	Drain Voltage
V_{gs}	-	Gate-Source Voltage
I_{ds}	-	Drain-Source Current
$R_{channel}$	-	Radius of Channel
T_{ox}	-	Oxide Thickness
N_d	-	Doping Concentration
E_g	-	Energy Bandgap

L_s	Length of Source
L_d	Length of Drain
ε	Permittivity

LIST OF APPENDICES

APPENDIX	TITLE	PAGE

CHAPTER 1

INTRODUCTION

1.1 Research Background

The evolution of transistor application in recent years have caught researcher attention in a field of nanoelectronics devices. The demand for higher processing speed, reduced cost and area has led to downsizing the size of the transistor. Transistor is a basic building for many aspects of electronic system and the technology associated with its architecture have dramatically changed since a past few years. It has many possible uses in amplification and Complementary Metal Oxide Semiconductor (CMOS) integrated circuit (IC). The sizing of transistor dimension follows the Moore's Law where the scaling has reached its end and alternative approach is necessary to sustain the miniaturization of the transistor besides preserve its electrical performance. For the past few decades, the number of transistor in a single chip have been following the Moore's Law [1]. Moore's law stated that the number of transistor will be double for every two years. Figure 1.1 shows that the transistor scaling using Moore's law prediction. The scaling factor is reduced by 70% size reduction of the technology nodes every two years has been adapted for linear scaling device.

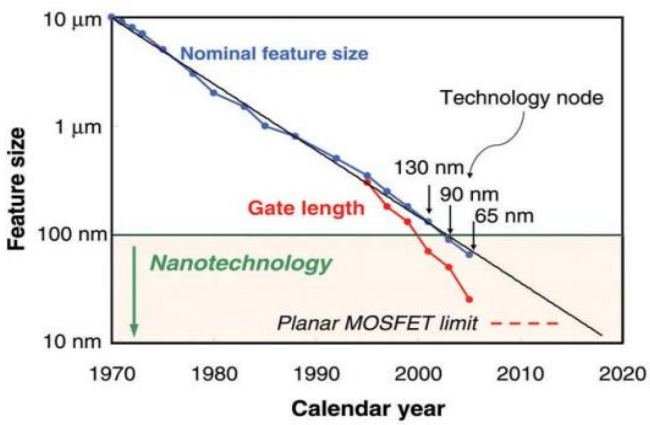

Figure 1.1Transistor scaling according to Moore's Law [2]

Thus, the advantages of such scaling can be seen through introduction of several processors in the market now. This is because its functionality has grown with transistors increment which much better in speed with small area at low cost. However, there are several issues as we downscale the size in traditional MOSFET such as threshold voltage roll-off, DIBL effect, velocity saturation decreases, leakage current increases, enhance surface scattering and mobility degradation [3]. All these effect might degrade the device performance.

However, International Roadmap for Devices and Systems (IRDS) is the organisation who provide a standard semiconductor roadmapping has generally outlined several potential devices and possible issue occurred in future development and research [4 -5]. IRDS be responsible for a guideline in research direction which helps appointed to set roadmap of the transistor and IRDS is the evolution from National Technology Roadmap for Semiconductors (NTRS) and International Technology Roadmap for Semiconductor (ITRS) previously. NTRS and ITRS were more focusing on the alternative methods to improve the performance of transistor but less attention on the application. Therefore, additional information and guidelines features in emerging architecture and systems for big data and cloud storage (IoT) was added while remaining the guideline from ITRS. The evolution of IRDS as shown in Figure 1.2.

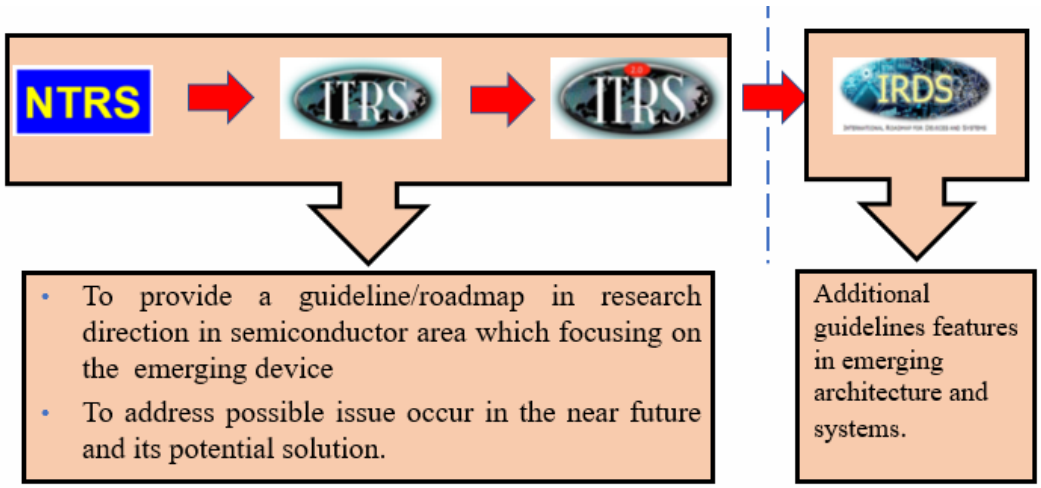

Figure 1.2 Evolution of IRDS

In general, the evolution of many aspects of transistor architecture aimed to mitigate the short channel effect (SCEs) which becomes pronounced at smaller device dimension. One way to overcome the SCEs is to use transistor with architecture with an ability to withstand the scaling limit. There has been an extensive research on the use of transistor architecture like FinFET, Multigate structure, Junctionless transistor and GAA transistor [6-8]. These kind of device configuration has found to have positive impact on the device performance as the channel dimension shrinked down. For example, Sachdeva et al., (2016) [9] showed GAA MOSFET is promising solution to reduce SCEs and improvement in device reliability. In another work by Jena et al., (2015) [10] reported a cylindrical architecture which the gate is surrounded by the body of the channel have shown to have better gate controlled. Furthermore, the GAA architecture have also proven to have excellent short channel immunity. In IRDS also shows that the GAA transistor will become a new transition of architecture since FinFET now is likely to sustain in the industry until the end of 2023 as shown in Table 1.1. Beyond 2019, a new transition from FinFET to GAA will be a hot topic in research area. In the same table shows that the technology node is keep decreasing by the year. It is to make sure that more transistor can be fit in a single chip. Recent research on nanoelectronic devices has also been focusing on the junctionless transistor [11]. This is due to less process involve in the fabrication as well as the simple architecture. Junctionless transistor used heavily doped with same doping level and have proven to improve the on current and large early voltage [12]. It has many advantages such as no P-N junction which make the structure simple, eliminates the doping concentration gradient and produce better short channel effect. Therefore, scaling down into 20 nm length is feasible.

Table 1.1 Device architecture roadmap for logic device technologies [4]

Year of Production	2017	2019	2021	2024	2027	2030	2033
Logic Industry "Node Range" Labelling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
Logic device structure options	FinFET FDSOI	FinFET LGAA	LGAA FinFET	LGAA VGAA	LGAA VGAA	VGAA LGAA 3DVLSI	VGAA LGAA 3DVLSI

Now, in the beyond Moore era have emerge the new device architecture such as, multiple gate transistor, gate all around (GAA) transistor and junctionless transistor. This is followed by the use of advance material such as carbon nanotube, graphene, strained silicon and the III-V materials [13-16]. IRDS have outlined several long-term challenges from 2021 - 2028. One of the important parameters delineated is on the device structure and materials. In IRDS under emerging research material has highlighted potential device which apart of high mobility material as shown in Table 1.2. Hence, there is a needs to further study the capability and benefits for such materials. In general, the evolution of many aspect of transistor architecture using advance architecture and non - silicon material aimed to mitigate the short channel effect (SCEs) problem which become pronounce at smaller device dimension particularly at sub – 10 nm gate length. The use of new device architecture and materials are to mitigate the short channel effect (SCE) often happen as the transistor is scaled down particularly to nanoscale where it involves the modification of the transistors channel. However, the smaller device dimension seems to be traded off with its performance as the SCEs become pronounce [17].

Table 1.2 Material for transistor scaling from IRDS under Emerging Research Material

Application	Emerging Material	Potential Advantage
High mobility semiconductors	InGaAs, InSb, strained III–V on silicon for p-channel	High hole mobilities for complementary MOSFETs
High mobility and steep subthreshold transistors	III–V (GaAs and GaN) nanowires, carbon nanotubes	High electron mobility with high gate control of leakage current
Ultra – high K gate dielectric with EOT	Extremely high – k dielectric such as TiO_2 or $SrTiO_2$	Improved transistor performance with low gate leakage and improved energy efficiency

Although the effect of using this kind of transistor architecture in terms of its electrical properties have been demonstrated, more work need to be done on

investigating the feasibility of using Junctionless-Gate-All-Around (JGAA) MOSFET using III - V channel material. III-V materials are predicted to be a good candidate to replace silicon for next generation. III-V material are under consideration for use in nanowire FET because of their high mobility compared to silicon which advantages to increase the drive current [12]. The semiconductor material used for transistor has traditionally been silicon, but there are more options available materials nowadays. These include GaAs (Gallium arsenide) and GaN (Gallium nitride). Notably, studies have reported excellent performance for GaAs and GaN materials. These materials are rapidly becoming the preferred semiconductor material for many transistor applications. The interest in III-V CMOS comes from outstanding electron transport in these materials which leads to higher electron mobility, excellent thermal properties and suitable for higher frequencies. Due to its benefit, the work done among researchers related to application of III-V material on the multigate structure were highlighted in the literature. Since JGAA MOSFET have showing a good performance among the other multigate structure due to its better good electrostatic control, III-V materials will help to boost the electrical performance specifically on the on current (I_{on}), threshold voltage (V_{th}) and current ratio (I_{on}/I_{off}).

Thus, this research proposes a transistor utilizing a JGAA MOSFET based III–V material channel which remains surrounded by a cylindrical structure using Sentaurus TCAD. To improve the accuracy and effectiveness of the device, suitable model taking into account in TCAD tools which are drift-diffusion and the quantum mechanical model. The outcome of this study is expected to produce high performance transistor using innovative device architecture at shorter gate length and improved power management in multibillion transistor circuit employed in microprocessor. This is in line with 11th Malaysia Plan for creation of new knowledge and identifying long term solution using advance material for electronic devices.

1.2 Problem Statement

For many applications using transistor, it is desirable to achieve high on current, low leakage current and lower threshold voltage. However, a major

challenge for transistor in nanoelectronics application is on the downsizing of the channel area to accommodate more transistors in an integrated circuit. In the IRDS also highlighted that the technology node used is predicted to be smaller as the gate length keeps on shrinking over the years. There are several issues when the size of conventional MOSFET been scaled down into a smaller size where short channel effects (SCEs) and quantum mechanical effects (QME) become pronounce. The issues such as threshold voltage roll-off, DIBL effect, leakage current increases etc. As a result, maintaining a low leakage current and as the same time preserve the high on current has become difficult. This will consequently affect the threshold voltage. High on current and lower leakage current is necessary for high speed in any transistor technology and low static power dissipation. Previous studies have demonstrated a variety of advance transistor architecture including FinFET [18], multigate transistor [19], carbon based devices [20-21], junctionless type of MOSFET [11] and High-K dielectric materials [22]. Although these kind of architecture improves performance, the process parameter involves is far from optimal. This make it falls short of those predicted from IRDS. It also necessary to include the right model to be incorporate with the classical model in TCAD tools to improve the accuracy of device performance. Considering high mobility channel, this study will investigate the used III – V material as a channel to be replaced on silicon material as suggested by the IRDS under Emerging Research Material. There are many transistor options at the market today combine various technologies with different semiconductor materials. As a result, it can be confusing to narrow down which one is the most suitable for transistor applications. GaAs and GaN are the most suitable materials for high speed transistor application. This research aimed to develop a device that suits for transistor application such as memory. Therefore, in this work, GaAs and GaN which are the III-V compound material is proposed as a substitute for silicon integrated with JGAA MOSFET to investigate the electrical significant of this material to sustain higher drive current while keeping the leakage current low which is hardly achieve using conventional silicon transistor. The technology node use in this research is 20 nm following the technology node predicted by IRDS. We predict smaller gate length is used for the future development of device as they keep moving to smaller dimensions. The development of device considering the quantum mechanical effect which is paramount important at thinner radius and gate oxide to improve the accuracy of the device model. The literature reviews highlighted in Chapter 2 can be a guideline in

finding the strength and weakness from the published works in order to find the research gap for this work.

The research problems are summarized as follows:

(a) The SCE and QME become pronounce when downscale the transistor size in conventional MOSFET.

(b) Numerical model that effect the device performance specifically quantum and short channel model.

(c) Alternative solutions to improve device performance which apart of high mobility material on channel such as III-V materials compared to silicon.

1.3 Research Objectives

From the research gaps and shortcomings that has been identified, the objectives of the research are summarized as follow:

(a) To design the 20 nm GaAs JGAA MOSFET using Sentaurus Synopsys TCAD.

(b) To study the effect of quantum mechanical effects on the 20 nm GaAs JGAA MOSFET.

(c) To evaluate and benchmark the performance of 20 nm GaAs JGAA MOSFET in this work with published work using conventional silicon on junctionless MOSFET and IRDS targeted.

1.4 Research Scopes

The scopes of the research are addressed as below:

1. Simulation of 20 nm GaAs JGAA MOSFET: The work is performed using Sentaurus Technology Computer Aided Design (TCAD) tools. GaAs and GaN are used as channel materials and silicon dioxide (SiO_2) as gate oxide material. The condition for quantum effect is considered when the radius and oxide thickness of GAA structure less than 10nm.

2. Computational simulation: In the simulation, from the existing model from TCAD tools, Density Gradient model, high field degradation (mobility model) and hydrodynamic model are included to study the QME for short channel device. Drift diffusion model is the default carrier transport model in Sentaurus TCAD.

3. Simulation work: The channel radius ($R_{channel}$), oxide thickness (T_{ox}) and doping concentration (N_d) were varied to see how it significantly influenced the quantum effect. The electrical performance evaluation was carried out by extracting the current-voltage (I – V) characteristic to evaluate the electrical properties such as V_{th}, I_{on}, current ratio (I_{on}/I_{off}) and the charge distribution along the channel radius.

1.5 Research Contributions

The research contributions are summarised as below:

1. Design device structure for 20 nm GaAs JGAA MOSFET: The silicon JGAA MOSFET has performed using Sentaurus TCAD. Then, III-V materials such as GaN and GaAs were tested on the JGAA MOSFET replacing the conventional silicon as channel material. The effect of gate length, radius of

channel, oxide thickness and doping concentration on the device structure were studied through the Current-Voltage (I_{ds}-V_{gs}) characteristics curve. Both materials were compared to each other and with the published work to see the electrical performance for both devices.

2. To study the quantum effect: To avoid mismatch and to extend the accuracy of the analysis, quantum mechanical and short channel effect are crucial to be considered. Conventional model is not able to capture the behaviour of device correctly. An appropriate model is chosen to accommodate for smaller radius and oxide thickness of the device. We used the simplified model to replace Schrodinger equation namely density gradient model to define quantum effect. The inclusion of High Field Degradation model and hydrodynamic model are necessary to include the short channel effects. The electrical performance evaluation was carried out by extracting the current-voltage characteristic and the normalised charge distribution (eDensity) along the channel radius. The GaAs JGAA MOSFET was first applied with classical model allowing the study of quantum effect.

3. Device benchmarking: To further evaluate the results, the final device of 20 nm GaAs JGAA MOSFET presented is compared with 20 nm silicon JGAA MOSFET. The performance is compare between V_{th}, I_{on}, and I_{off}. In addition, the final device also is compared with the published work that using silicon channel on junctionless MOSFET and IRDS targeted for low power application.

1.6 Thesis Organization

Chapter 1 explained the fundamental knowledge regarding this research focus. The challenges and potential solutions is highlighted based on the roadmapping in the semiconductor field provided by the International Roadmap Device Semiconductor (IRDS) to give a landmark for research directions. The problem statements are

summarized in details after identifying the strength and weaknesses of previous works also following the IRDS projections for future nanoscale devices. The research objectives and research scopes are identified and discussed further through literature and tools available. Finally, the research covered and contributions are explained in chapter 1.

Chapter 2 is the part where literature reviews is covered related to high mobility channel specifically III-V materials on advanced transistor. The evolutions from planar MOSFETs to the advanced MOSFETs are also covered to give an exposure and understanding on the concept to develop a device structure. Then, the review on the fundamental knowledge on quantum and short channel effect were highlighted to identify the appropriate model in describing the carrier transport in the GaAs JGAA structure.

Chapter 3 elaborates the research flow using the general flowchart and then more specific on the development of device. Systematic research was executed related to the scope of works mentioned in Chapter 1. The model used in TCAD tools also emphasized. The important parameters used for TCAD simulations also highlighted in this section.

Chapter 4 present the numerical simulation for short channel GaAs JGAA MOSFET. The simulation works has included the quantum and short channel effects to accommodate the analysis for short channel device. The analysis is conducted by variation of channel radius, oxide thickness and doping concentration since those parameters is vital to account the quantum effect. Besides, the study of III-V materials on channel replacing the conventional silicon is investigated before GaAs is chosen for final benchmarking due to better electrical performance. The benchmarking is compared between the published works and IRDS projection at gate length of 20nm. The electrical performance is carried out by investigating on the current-voltage (I_{ds}-V_{gs}) characteristics curve and normalized charge distribution along the channel radius.

Chapter 5 summarized the finding and contributions reflected to the objectives in Chapter 1. The future work recommendation to improve the proposed device is

mentioned which very beneficial for upcoming research and may be used for many applications.

REFERENCES

1. Schaller, R. R. Moore's law: past, present and future. IEEE spectrum, , 34(6): 52–59, 1997.
2. Thompson, S. E., & Parthasarathy, S. Moore's law: the future of Si microelectronics. Materials Today, 2006, 9(6), 20–25.
3. Razavi P, Orouji AA. Dual material gate oxide stack symmetric double gate MOSFET: improving short channel effects of nanoscale double gate MOSFET. In2008 11th International Biennial Baltic Electronics Conference 2008, pp. 83-86.
4. The International Roadmap for Devices and Systems (IRDS). The International Roadmap for Devices and Systems: More Moore. Technical report. IEEE. 2017.
5. The International Roadmap for Devices and Systems (IRDS). The International Roadmap for Devices and Systems: IRDS Executive Summary. Technical Report. IEEE. 2017 Kim SD, Guillorn M, Lauer I, Oldiges P, Hook T, Na MH. Performance trade-offs in FinFET and gate-all-around device architectures for 7nm-node and beyond. In2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) 2015 Oct 5, pp. 1-3.
6. Huang YL, Lin CH, Liu CW, inventors; Taiwan Semiconductor Manufacturing Co (TSMC) Ltd, assignee. Vertical gate all around (VGAA) devices and methods of manufacturing the same. United States patent US 9,536,738. 2017 Jan 3.
7. C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge. Junctionless multigate field-effect transistor, Appl. Phys. Lett., Feb. 2009, vol. 94, no. 5, pp. 053511-1–053511-2.
8. Sachdeva TK, Aggarwal SK, Kushwaha AK. Design Analysis and Simulation of 30 nm Cylindrical Gate all around MOSFET. IEEE Trans. IJARCCE. 2016 Oct;5(10).
9. Jena B, Pradhan KP, Sahu PK, Dash S, Mishra GP, Mohapatra SK. Investigation on cylindrical gate all around (GAA) to nanowire MOSFET for

circuit application. Facta Universitatis, Series: Electronics and Energetics. 2015 Jul 2;28(4):637-43.

10. Bavir M, Abbasi A, Orouji AA. A Simulation Study of Junctionless Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor with Symmetrical Side Gates. Silicon. 2019 Sep 2:1-0.
11. J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, et al.,. Nanowire transistors without junctions, Nat. Nanotechnol., Mar. 2010, vol. 5, no. 3, pp. 225–229.
12. Kumar K, Sahithi C, Sahoo R, Sahoo SK. Ultra low power full adder circuit using carbon nanotube field effect transistor. In2014 International Conference on Power, Control and Embedded Systems (ICPCES) 2014 Dec 26, (pp. 1-4).
13. Srivastava A, Banadaki YM, Fahad MS. Dielectrics for graphene transistors for emerging integrated circuits. ECS Transactions. 2014 Mar 24;61(2):351.
14. Grillet C, Logoteta D, Cresti A, Pala MG. Assessment of the electrical performance of short channel InAs and strained Si nanowire FETs. IEEE Transactions on Electron Devices. 2017 Mar 23;64(5):2425-31.
15. Waldron N. III-V Devices and Technology for CMOS. InHigh Mobility Materials for CMOS Applications, Woodhead Publishing, 2018 Jan 1, pp. 231-280.
16. Hu G, Xiang P, Ding Z, Liu R, Wang L, Tang TA. Analytical models for electric potential, threshold voltage, and subthreshold swing of junctionless surrounding-gate transistors. IEEE Transactions on Electron Devices. 2014, Jan 14;61(3):688-95.
17. Li KS, Chen PG, Lai TY, Lin CH, Cheng CC, Chen CC, Wei YJ, Hou YF, Liao MH, Lee MH, Chen MC. Sub-60mV-swing negative-capacitance FinFET without hysteresis. In2015 IEEE International Electron Devices Meeting (IEDM) 2015 Dec 7, (pp. 22-6).
18. Seifert N, Jahinuzzaman S, Velamala J, Ascazubi R, Patel N, Gill B, Basile J, Hicks J. Soft error rate improvements in 14-nm technology featuring second-generation 3D tri-gate transistors. IEEE Transactions on Nuclear Science. 2015 Dec 17;62(6):2570-7.
19. Dekker C. How we made the carbon nanotube transistor. Nature Electronics. 2018 Sep;1(9):518.

20. Vieira NC, Borme J, Machado Jr G, Cerqueira F, Freitas PP, Zucolotto V, Peres NM, Alpuim P. Graphene field-effect transistor array with integrated electrolytic gates scaled to 200 mm. Journal of Physics: Condensed Matter. 2016 Feb 1;28(8):085302.
21. Chatterjee N, Gupta A, Pandey S. III–V Junctionless Nanowire Transistor with High-k Dielectric Material and Schottky Contacts. Journal of Nanoelectronics and Optoelectronics. 2017 Sep 1;12(9):925-31.
22. Thompson, S. E. and Parthasarathy, S.Moore's law: the future of Si microelectronics. Materials today, 2006. 9(6): 20–25.
23. Mandelman, J. A., Dennard, R. H., Bronner, G. B., DeBrosse, J. K., Divakaruni, R., Li, Y. and Radens, C. J. Challenges and future directions for the scaling of dynamic random-access memory (DRAM). IBM Journal of Research and Development, 2002. 46(2.3): 187–212.
24. Hosseini, R., Fathipour, M., & Faez, R., "Quantum simulation study of gate-all-around (GAA) silicon nanowire transistor and double gate metal oxide semiconductor field effect transistor (DG MOSFET)", *International Journal of Physical Sciences*, 2012 *7*(28), 5054-5061.
25. Hareland, S.A., Krishnamurthy, S., Jallepalli, S., Yeap, C.F., Hasnat, K., Tasch, A.F. and Maziar, C.M., 1996. A computationally efficient model for inversion layer quantization effects in deep submicron N-channel MOSFETs. *IEEE Transactions on Electron Devices*, *43*(1), pp.90-96.
26. Momose HS, Ono M, Yoshitomi T, Ohguro T, Nakamura SI, Saito M, Iwai H. Tunneling gate oxide approach to ultra-high current drive in small geometry MOSFETs. InProceedings of 1994 IEEE International Electron Devices Meeting 1994 Dec 11, (pp. 593-596).
27. Prégaldiny F, Lallement C, van Langevelde R, Mathiot D. An advanced explicit surface potential model physically accounting for the quantization effects in deep-submicron MOSFETs. Solid-State Electronics. 2004 Mar 1;48(3):427-35.
28. Taur Y, Buchanan DA, Chen W, Frank DJ, Ismail KE, Lo SH, Sai-Halasz GA, Viswanathan RG, Wann HJ, Wind SJ, Wong HS. CMOS scaling into the nanometer regime. Proceedings of the IEEE. 1997 Apr;85(4):486-504.

29. Padilla JL, Gamiz F, Godoy A. Impact of quantum confinement on gate threshold voltage and subthreshold swings in double-gate tunnel FETs. IEEE transactions on electron devices. 2012 Oct 9;59(12):3205-11.

30. Iniguez B., J. D. R. J. H. H. M. L. and Pallaras, J. Explicit continuous model for long-channel undoped surrounding gate MOSFETs. IEEE Transactions on Electron Devices., 2005. 52(8): 1868-73.

31. Vimala, P., and N. B. Balamurugan. "Modeling and simulation of centroid and inversion charge density in cylindrical surrounding gate MOSFETs including quantum effects." *Journal of Semiconductors* 34.11 (2013): 114001.

32. Roldan, J. B., et al. "Modeling the centroid and the inversion charge in cylindrical surrounding gate MOSFETs, including quantum effects." *IEEE transactions on electron devices* 55.1 (2007): 411-416.

33. Stern, Frank, and W. E. Howard. "Properties of semiconductor surface inversion layers in the electric quantum limit." *Physical Review* 163.3 (1967): 816.

34. Stern, Frank. "Self-consistent results for n-type Si inversion layers." *Physical Review B* 5.12 (1972): 4891.

35. Ferain, Isabelle, Cynthia A. Colinge, and Jean-Pierre Colinge. "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors." *Nature* 479.7373 (2011): 310-316.

36. Kaur, Ravneet, et al. "Unified subthreshold model for channel-engineered sub-100-nm advanced MOSFET structures." *IEEE transactions on electron devices* 54.9 (2007): 2475-2486.

37. Navarro C, Bawedin M, Andrieu F, Sagnes B, Martinez F, Cristoloveanu S. Supercoupling effect in short-channel ultrathin fully depleted silicon-on-insulator transistors. Journal of Applied Physics. 2015 Nov 14;118(18):184504.

38. Seo J, Lee J, Shin M. Analysis of drain-induced barrier rising in short-channel negative-capacitance FETs and its applications. IEEE Transactions on Electron Devices. 2017 Feb 14;64(4):1793-8.

39. Chau, R., Doczy, M., Doyle, B., Datta, S., Dewey, G., Kavalieros, J., Jin, B., Metz, M., Majumdar, A. and Radosavljevic, M., 2004, October. Advanced CMOS transistors in the nanotechnology era for high-performance, low-power

logic applications. In *Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.* Vol. 1, pp. 26-30.

40. Fahad HM, Hussain MM. Are nanotube architectures more advantageous than nanowire architectures for field effect transistors?. Scientific reports. 2012 Jun 27;2(1):1-7.
41. Colinge, Jean-Pierre. "From gate-all-around to nanowire MOSFETs." *2007 International Semiconductor Conference*. Vol. 1. IEEE, 2007.
42. Poiroux, T., et al. "Multiple gate devices: advantages and challenges." *Microelectronic Engineering* 80 (2005): 378-385.
43. Poiroux, T., et al. "Multigate silicon MOSFETs for 45 nm node and beyond." *Solid-state electronics* 50.1 (2006): 18-23.
44. Collaert, N., De Keersgieter, A., Dixit, A., Ferain, I., Lai, L. S., Lenoble, D., & Jurczak, M, “Multi-gate devices for the 32 nm technology node and beyond”, Solid-State Electronics, 52(9), (2008), 1291-1296.
45. Sekigawa, Toshihiro. "Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate." *Solid-State Electronics* 27.8 (1984): 827-828.
46. Colinge, Jean-Pierre. "The SOI MOSFET: From single gate to multigate." *FinFETs and other multi-gate transistors*. Springer, Boston, MA, 2008. 1-48.
47. Colinge, J. P., Gao, M. H., Romano, A., Maes, H. & Claeys C. Silicon-on-insulator ‘gate-all-around device’. Tech. Digest IEEE Electron Devices Meet. IEEE, 1990, 595–598.
48. Pratap, Yogesh, et al. "An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating the influence of device design engineering." *Microelectronics Journal* 45.4 (2014): 408-415.
49. Chiang, Te-Kuang. "A compact model for threshold voltage of surrounding-gate MOSFETs with localized interface trapped charges." *IEEE Transactions on Electron Devices* 58.2 (2011): 567-571.
50. Zhang, Lining, et al. "Analytical solution of subthreshold channel potential of gate underlap cylindrical gate-all-around MOSFET." *Solid-state electronics* 54.8, 2010, 806-808.

51. Sharma, Dheeraj, and Santosh Kumar Vishvakarma. "Precise analytical model for short channel cylindrical gate (CylG) gate-all-around (GAA) MOSFET." *Solid-state electronics* 86, 2013, 68-74.

52. Jena, B., et al. "Performance analysis of undoped cylindrical gate all around (GAA) MOSFET at subthreshold regime." *Advances in Natural Sciences: Nanoscience and Nanotechnology* 6.3, 2015, 035010.

53. Ansari, L., Feldman, B., Fagas, G., Colinge, J. P. & Greer, J. C. Simulation of junctionless Si nanowire transistors with 3 nm gate length. Appl. Phys. Lett. 97, 062105, 2010.

54. Wong HY, Braga N, Mickevicius RV. Enhancement-Mode Recessed Gate and Cascode Gate Junctionless Nanowire With Low-Leakage and High-Drive Current. IEEE transactions on Electron Devices. 2018 Jul 30;65(9):4004-8.

55. J. Colinge, "Junctionless transistors," *IEEE International Meeting for Future of Electron Devices, Kansai*, Suita, Japan, 2012, 2012, pp. 1-2.

56. Mirza MM, Schupp FJ, Mol JA, MacLaren DA, Briggs GA, Paul DJ. One dimensional transport in silicon nanowire junction-less field effect transistors. Scientific reports. 2017 Jun 7;7(1):1-8.

57. Memišević E, Svensson J, Hellenbrand M, Lind E, Wernersson LE. Scaling of vertical InAs–GaSb nanowire tunneling field-effect transistors on Si. IEEE Electron Device Letters. 2016 Mar 23;37(5):549-52.

58. Guerfi Y, Larrieu G. Vertical silicon nanowire field effect transistors with nanoscale gate-all-around. Nanoscale research letters. 2016 Dec;11(1):1-7.

59. Llinas JP, Fairbrother A, Barin GB, Shi W, Lee K, Wu S, Choi BY, Braganza R, Lear J, Kau N, Choi W. Short-channel field-effect transistors with 9-atom and 13-atom wide graphene nanoribbons. Nature communications. 2017 Sep 21;8(1):1-6.

60. Qiu, C., Zhang, Z., Xiao, M., Yang, Y., Zhong, D. and Peng, L.M.,. Scaling carbon nanotube complementary transistors to 5-nm gate lengths. *Science*, *355*(6322), 2017, pp.271-276.

61. Park, S. H., Liu, Y., Kharche, N., Salmani Jelodar, M., Klimeck, G., Lundstrom, M. S., & Luisier, M. Performance Comparisons of III–V and Strained-Si in Planar FETs and Nonplanar FinFETs at Ultrashort Gate Length (12 nm). IEEE Transactions on Electron Devices, 59(8), 2012, 2107–2114.

62. Sun, Y., Kiewra, E. W., de Souza, J. P., Bucchignano, J. J., Fogel, K. E., Sadana, D. K., & Shahidi, G. G.. High-Performance $\hbox{In}_{0.7}\hbox{Ga}_{0.3}\hbox{As}$ -Channel MOSFETs With High-κ Gate Dielectrics and α-Si Passivation. IEEE Electron Device Letters, 2009, 30(1), 5–7.

63. Y. Xuan, T. Shen, M. Xu, Y. Q. Wu, and Q. D. Ye, "High-performance surface channel In-rich In0.75Ga0.25As MOSFETs with ALD high-κ as gate dielectric," in IEDM Tech. Dig., 2008, pp. 1–4.

64. S. Oktyabrsky and P. Ye, Fundamentals of III–V Semiconductor MOSFETs. New York: Springer-Verlag, 2010.

65. da Nobrega RV, Fonseca YM, Costa RA, Duarte UR. "Comparative Study on the Performance of Silicon and III-V Nanowire Gate-All-Around Field-Effect Transistors for Different Gate Oxides", Proc. Semiconductors and Micro and Nano Technology. 2018 Jul.

66. Schwarz, M., & Kloes, A., "Analysis and performance study of III–V Schottky barrier double-gate MOSFETs using a 2-D analytical model", IEEE Transactions on Electron Devices, (2016), 63(7), 2757-2763.

67. Kulkarni S, Joshi S, Bade D, Subramaniam S. "Design Optimization of 10 nm Channel Length InGaAs Vertical Gate-All-Around Transistor (Nanowire)", InComputing, Communication and Signal Processing, 2019, pp. 611-619.

68. Dutta, T., Kumar, S., Rastogi, P., Agarwal, A., & Chauhan, Y. S., "Impact of channel thickness variation on bandstructure and source-to-drain tunneling in ultra-thin body III-V MOSFETs", IEEE Journal of the Electron Devices Society, (2016), 4(2), 66-71.

69. Gu, J. J., Wu, H., Liu, Y., Neal, A. T., Gordon, R. G., & Peide, D. Y., "Size-Dependent-Transport Study of $\hbox {In} _ {0.53}\hbox {Ga} _ {0.47}\hbox {As} $ Gate-All-Around Nanowire MOSFETs: Impact of Quantum Confinement and Volume Inversion", IEEE electron device letters, (2012), 33(7), 967-969.

70. Gupta R, Vaid R. "TCAD performance analysis of high-K dielectrics for gate all around InAs nanowire transistor considering scaling of gate dielectric thickness", Microelectronic Engineering, 2016 Jul, 1;160:22-6.

71. Kiran KS, Reddy KJ. Design and Simulation of group III-V Gate All around MOSFET. IJRTI. 2016;1(3):42-6.

72. Chatterjee N, Pandey S. Simulation and Finite Element Analysis of Electrical Characteristics of Gate-all-Around Junctionless Nanowire Transistors. Журнал нано-та електронної фізики. 2016, 01025-1).

73. Babu SS, Moni DJ, Padickala PJ. TCAD simulation study of GaN based junctionless GAA nano transistor for high frequency applications. In2016 3rd International Conference on Devices, Circuits and Systems (ICDCS) 2016 Mar 3, pp. 226-230.

74. R. Y. ElKashlan, O. Samy, A. Anis, Y. Ismail, and H. Abdelhamid, "Unified quantum and reliability model for ultrathin double-gate MOSFETs," Silicon, Feb. 2019, vol. 12, no. 1, pp. 21–28.

75. A. S. Medury and H. Kansal, "Quantum confinement effects and electrostatics of planar nano-scale symmetric double-gate SOI MOSFETs," in Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC), Jun. 2019, pp. 1–3.

76. Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs," IEEE Electron Device Lett., Dec. 1993, vol. 14, no. 12, pp. 569–571.

77. H. Majima, H. Ishikuro, and T. Hiramoto, "Experimental evidence for quantum mechanical narrow channel effect in ultra-narrow MOSFET's," IEEE Electron Device Lett., Aug. 2000, vol. 21, no. 8, pp. 396–39.

78. D. Sharma and S. K. Vishvakarma, "Precise analytical model for short channel cylindrical gate (CylG) gate-all-around (GAA) MOSFET," Solid-State Electron., Aug. 2013, vol. 86, pp. 68–74.

79. H. A. El Hamid, B. Iniguez, and J. Roig Guitart, "Analytical model of the threshold voltage and subthreshold swing of undoped cylindrical gate-all-around-based MOSFETs," IEEE Trans. Electron Devices, Mar. 2007, vol. 54, no. 3, pp. 572–579.

80. Ancona, M. G., & Biegel, B. A., "Nonlinear discretization scheme for the density-gradient equations", International Conference on Simulation Semiconductor Processes and Devices 2000, September, pp. 196-199.

81. Wettstein, A., "Quantum effects in MOS devices", (Doctoral dissertation, ETH Zurich), 2000.

82. Matsuzawa, K., Takagi, S. I., Takayanagi, M., & Tanimoto, H, "Device simulation of surface quantization effect on MOSFETs with simplified density-gradient method", *Solid-State Electronics*, *46*(5), 747-751, 2000.

83. Chen X, Tan CM. “Modeling and analysis of gate-all-around silicon nanowire FET”, Microelectronics Reliability. 2014 Jun 1;54(6-7):1103-8.

84. A. Dasgupta et al., “BSIM compact model of quantum confinement in advanced nanosheet FETs,” IEEE Trans. Electron Devices, Feb. 2020, vol. 67, no. 2, pp. 730–737.

85. Hamid, F. K., Johari, Z., Alias, N. E., Lim, W. H., Sultan, S. M., Leong, W. S., & Ismail, R, “Modeling of inversion and centroid charges of long channel strained-silicon surrounding gate MOSFETs incorporating quantum effects”, Semiconductor Science and Technology, 2020, 35(2), 025010.

86. Yuan Y, Yu B, Song J, et al. “An Analytical model for threshold voltage shift due to quantum confinement in surrounding gate MOSFETs with anisotropic effective mass”, Solid-State Electron, 2009, 53: 140.

87. Wu Y S, Su P. “Analytical quantum-confinement model for shortchannel gate-all-around MOSFETs under subthreshold region”, IEEE Trans Electron Devices, 2009, 56(11): 2720.

88. Moreno E, Roldan J B, Barrera D, et al. “An analytical model foe square GAA MOSFETs including quantum effects”, Solid-State Electron, 2010, 54: 1463.

89. Van Dort, M. J., P. H. Woerlee, and A. J. Walker, "A simple model for quantisation effects in heavily-doped silicon MOSFETs at inversion conditions.", *Solid-State Electronics*, 1994, 37.3: 411-414.

90. M. G. Ancona and H. F. Tiersten, “Macroscopic physics of the silicon inversion layer,” Phys. Rev. B, 1987, vol. 35, pp. 7959–7965.

91. Penzin, Oleg, et al., "Extended Quantum Correction Model Applied to Six-Band ${\bf k}\cdot {\bf p} $ Valence Bands Near Silicon/Oxide Interfaces.", *IEEE transactions on electron devices*, 2011, 58.6: 1614-1619.

92. Ieong, MeiKei, Ronald Logan, and James Slinkman., "Efficient quantum correction model for multi-dimensional CMOS simulations.", *Simulation of Semiconductor Processes and Devices 1998*. Springer, Vienna, 1998, 129-132.

93. X. Wang and T.-W. Tang, “Comparison of three quantum correction models for charge density in MOS inversion layers,” J. Comput. Electron., Jul. 2002, vol. 1, no. 1/2, pp. 283–287.

94. F. A. Noor, C. Bimo, and Khairurrijal, “Analytical quantum drain current model in undoped cylindrical surrounding-gate MOSFETS,” J. Telecommun. Electron. Comput. Eng., 2017, vol. 9, no. 1–5, pp. 101–105.

95. P. Vimala and N. B. Balamurugan, “Modeling and simulation of centroid and inversion charge density in cylindrical surrounding gate MOSFETs including quantum effects,” J. Semicond., 2013, vol. 34, no. 11.

96. J. B. Roldan, A. Godoy, F. Gamiz and M. Balaguer, "Modeling the Centroid and the Inversion Charge in Cylindrical Surrounding Gate MOSFETs, Including Quantum Effects," in IEEE Transactions on Electron Devices, 2008, vol. 55, no. 1, pp. 411-416.

97. Sun, S. X., Ma, L. H., Cheng, C., Zhang, C., Zhong, Y. H., Li, Y. X., ... & Jin, Z., “Numerical simulation of the impact of surface traps on the performance of InP-based high electron mobility transistors”, physica status solidi (a), 2017, 214(10), 1700322.

98. Synopsys, Mountain View, CA, Synopsys Sentaurus Device Manuals.

99. Ajayan, J., Ravichandran, T., Prajoon, P., Pravin, J. C., & Nirmal, D., “Investigation of breakdown performance in $$ L_ {g} $$ L g= 20 nm novel asymmetric InP HEMTs for future high-speed high-power applications”, Journal of Computational Electronics, 2018, 17(1), 265-272.

100. Pan A, Leung G, Chui CO. Junctionless silicon and In 0.53 Ga 0.47 As transistors—Part I: Nominal device evaluation with quantum simulations. IEEE Transactions on Electron Devices. 2015 Aug 25;62(10):3199-207.

101. Saraswat KC, Chui CO, Kim D, Krishnamohan T, Pethe A. High mobility materials and novel device structures for high performance nanoscale MOSFETs. In2006 International Electron Devices Meeting 2006 Dec 11, pp. 1-4.

102. Moon SH, Nisha NN, Saha JK. Characterization of Nanowire Field Effect Transistor and Comparison Based on Different Performance Criteria. In2019 International Conference on Sustainable Technologies for Industry 4.0 (STI) 2019 Dec 24, pp. 1-5.

103. Lee Y, Shin C. Impact of equivalent oxide thickness on threshold voltage variation induced by work-function variation in multigate devices. IEEE Transactions on Electron Devices. 2017 Mar 15;64(5):2452-6.

104. Islam, A., & Kalna, K., “Analysis of electron transport in the nano-scaled Si, SOI and III-V MOSFETs: Si/SiO2 interface charges and quantum mechanical effects”, In *IOP Conference Series: Materials Science and Engineering*, IOP Publishing, 2019, April, Vol. 504, No. 1, p. 012021.

105. Mohammadi, S., & Afzali-Kusha, A., “Drain current model for strained-Si/Si1− xGex/strained-Si double-gate MOSFETs including quantum effects”, Semiconductor science and technology, 2011, 26(9), 095022.

106. Rout, S. P., & Dutta, P., “Impact of high mobility III-V compound material of a short channel thin-film SiGe double gate junctionless MOSFET as a source”, Engineering Reports, 2020, 2(1), e12086.

107. Hu, V. P. H., & Wang, C. T., “Optimization of III–V heterojunction tunnel FET with non-uniform channel thickness for performance enhancement and ambipolar leakage suppression”, Japanese Journal of Applied Physics, 57(4S), 04FD18, 2018.

108. Pethe, A., Krishnamohan, T., Kim, D., Oh, S., Wong, H. S. P., & Saraswat, K., “Investigation of the performance limits of III-V double-gate n-MOSFETs”, In 2006 16th Biennial University/Government/Industry Microelectronics Symposium, 2006 June, pp. 47-50.

109. Venugopalan, S., Karim, M. A., Salahuddin, S., Niknejad, A. M., & Hu, C. C., “Phenomenological compact model for QM charge centroid in multigate FETs”, IEEE transactions on electron devices, 2013, 60(4), 1480-1484.

110. Singh, D., Vig, R., Madhu, C., & Kaur, R., “Comparison Between the Performance of Trigate Junctionless Transistor and Double-Gate Junctionless Transistor with Same Device Length”, In Intelligent Communication, Control and Devices, Springer, Singapore, 2018, pp. 991-997.

111. Merad, F., & Guen-Bouazza, A., “DC performance analysis of a 20nm gate lenght n-type silicon GAA junctionless (Si JL-GAA) transistor”, International Journal of Electrical and Computer Engineering, 2020, 10(4), 4043.

112. Wang, Y., Shan, C., Dou, Z., Wang, L. G., & Cao, F., “Improved performance of nanoscale junctionless transistor based on gate engineering approach”, Microelectronics Reliability, 2015, 55(2), 318-325.

LIST OF PUBLICATIONS

Journal with Impact Factor

1. A Study of 20nm GaAs Junctionless-Gate-All-Around Field Effect Transistor Including Quantum Mechanical Effects. IOP Semiconductor Science and Technology (IF: Q2, Submitted)

Journal with Scopus

1. A Performance Study of Long Channel GaAs Junctionless-Gate-All-Around Field Effect Transistor (In-Press)

Indexed Conference Proceedings

2. Rasol, M. F. M., et al. "Performance Analysis of Silicon and III-V Channel Material for Junctionless-Gate-All-Around Field Effect Transistor." *2020 IEEE Student Conference on Research and Development (SCOReD)*. IEEE, 2020.

3. Rasol, M. F. M., et al. "Stacking SiO 2/High-$ K $ Dielectric Material in 30nm Junction-less Nanowire Transistor Optimized Using Taguchi Method for Lower Leakage Current." *2019 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)*. IEEE, 2019.

Competition / Exhibition

1. 22nd Industrial Art and Technology Exhibition (INATEX) 2020