VARIABLE OXIDE THICKNESS OPTIMIZATION AND RELIABILITY ANALYSIS OF GATE-ALL-AROUND FLOATING GATE FOR FLASH MEMORY CELL

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A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Philosophy

School of Electrical Engineering
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APRIL 2020

DEDICATION

To my beloved husband, family and friends.

ACKNOWLEDGEMENT

I would like to express my deepest appreciation to whom I owe a debt in completing this Master's degree work. Million thanks to my family, especially to my parents and parent-in-law, for all their understandings and emotional supports to give me the encouragement to go forth in my career and life.

Firstly, I would like to express my great appreciation to my beloved husband for his support and help throughout my Master journey.

Secondly, I would like to thank my supervisor, Dr. Nurul Ezaila Binti Alias for her valuable advice and great mentoring. She is tirelessly giving encouragement to do my work delicately and productively. She also pressure me to improve my writing and publish academic work. She always advise me to focus in order to accomplish every work by deadline in pursuing success.

Next, I also thank my co-supervisor (co-SV), Professor Razali Bin Ismail for his support and endearing advice that really motivated me to publish more academic work. I also want to deliver my appreciation and thank to my co-SV Dr. Zaharah Binti Johari for all the technical support and advice that inevitably improved the quality of my publication work. Her advice has made me even more motivated in delivering positive and quality output for my research work. My companions in the Computational Nanoelectronic Research lab for all the support in variety of ways. Special thanks to Dr. Afiq Nuruddin, Lim Wei Hong, Fatimah Khairiah and Zuriana for sharing their ideas and giving significant contribution in improving my works. Not to forget Mr. Zulkifli and Hilman for their support. Last but not least, to the Ministry of Higher Education (MOHE) for providing funds for conference travels and publication charges.

ABSTRACT

Gate-All-Around (GAA) transistor is one of the excellent devices that has been utilized for flash memory applications owing to its gate coupling which led to a higher gate electrostatic control, cheaper manufacturing cost and bigger data storage. However, GAA structure with floating gate memory cell may suffer from cell-to-cell interference resulting in higher operational voltage. One of the effective solutions for lowering the program/erase (P/E) voltage is by down-scaling the tunnel oxide thickness. However, scaling down the tunnel dielectric layer may degrade the data retention and endurance due to stress induced leakage current (SILC). Thus, a concept of tunnel barrier engineering using Variable Oxide Thickness (VARIOT) of low-k/high-k stack has been implemented on Gate-All-Around Floating Gate (GAA-FG) memory cell to reduce P/E operational voltage, to improve the efficiency of data retention after 10years and endurance after 10^4 of P/E cycles. This research begins with the VARIOT optimization of five high-k dielectric materials which are Zirconium dioxide, Hafnium (IV) Oxide, Lanthanum Oxide, Yttrium (III) Oxide, and Aluminium Oxide (ZrO_2, HfO_2, La_2O_3, Y_2O_3 and Al_2O_3) in which these high-k dielectrics can be embedded onto low-k dielectric layer which is Silicon Dioxide, SiO_2 using 3-Dimensional (3D) TCAD simulator of Silvaco ATLAS. Then, the transient performances of the GAA-FG memory cell with optimized parameters are assessed to offset the trade-off between P/E characteristics and the device reliability including data retention and endurance. From VARIOT optimization, interestingly, it is found that SiO_2/La_2O_3 asymmetric stack has become a promising candidate to improve the P/E characteristics and the reliability of GAA-FG memory cell due to the lowest programming voltage compared to other high-k dielectric materials. By using P/E operational voltage of 10/-12V, 20% improvement of threshold window has been observed for SiO_2/La_2O_3 stack compared to conventional single tunnel layer of SiO_2. Based on the proposed approach, the data retention slightly degrades by only ~5% after 10 years of extrapolation and reasonable P/E endurance is obtained with only ~16% loss after 10^4 of P/E cycles. Apparently, these findings indicate that better performances of GAA-FG memory cell with the incorporation of SiO_2/La_2O_3 tunnel layer which can be used to assist experimental work.

ABSTRAK

Transistor get-silinder-menyeluruh (GAA) adalah salah satu daripada perisian terbaik yang digunakan dalam aplikasi flash memori disebabkan gandingan get yang boleh memberi kesan kepada kesan elektrostatik get yang kuat, murah kos pembuatan dan besar data penyimpanan. Kebolehan struktur GAA dengan sel memori get-terapung (FG) boleh merosot daripada gangguan sel kepada sel yang memerlukan voltan operasi yang tinggi. Satu cara yang efektif bagi menurunkan voltan bagi operasi program/padam (P/E) ialah dengan mengurangkan ketebalan oksida terowong. Walau bagaimanapun, mengurangkan ketebalan terowong bagi lapisan dielektrik boleh mengurangkan prestasi data pengekalan dan pertahanan disebabkan oleh tekanan menghasilkan arus-kebocoran (SILC). Oleh itu, satu konsep yang dipanggil sebagai terowong penghadang Oksida Boleh-ubah (VARIOT) k-rendah/k-tinggi digunakan dengan GAA get-terapung (GAA-FG) bagi mengurangkan voltan operasi P/E, menambahbaik data pengekalan selepas 10 tahun dan data pertahanan selepas kitaran P/E sebanyak 10^4. Kajian ini dimulakan dengan pengoptimuman VARIOT bagi 5 bahan dielektrik (ZrO_2, HfO_2, La_2O_3, Y_2O, Al_2O_3) di mana dielektrik ini akan digabungkan dengan bahan k-rendah (SiO_2) menggunakan perisian Silvaco ATLAS. Kemudian, prestasi GAA-FG beserta parameter optimum diuji bagi meningkatkan kualiti prestasi sel dari aspek P/E dan kebolehpercayaan peranti (data pengekalan dan data pertahanan). Daripada pengoptimuman VARIOT, gabungan SiO_2/La_2O_3 adalah bahan yang berpotensi untuk menambahbaik prestasi P/E dan kebolehpercayaan sel memori GAA-FG disebabkan voltan program terendah berbanding 4 bahan dielektrik yang lain. Menggunakan voltan operasi P/E sebanyak 10V/-12V, sebanyak 20% penambahbaikan tingkap-ambang telah dilihat bagi gabungan SiO_2/La_2O_3 berbanding dengan hanya satu lapisan SiO_2 bagi oksida terowong. Tambahan pula, data pengekalan hanya berkurang sebanyak 5% selepas 10 tahun manakala data pertahanan berkurang sebanyak 16% selepas kitaran P/E sebanyak 10^4. Penemuan ini menunjukkan sel memori GAA-FG dengan terowong oksida SiO_2/La_2O_3 boleh digunakan untuk membantu kerja eksperimen.

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LIST OF ABBREVIATIONS

BiCS – Bits-Cost Scalable

CB – Conduction Band

CG – Control Gate

CMOS – Complementary Metal-Oxide Semiconductor

CT – Charge Trap

C-FG – Conventional-Floating Gate

DC-SF – Dual Control Gate with Surrounding Floating-Gate

DIBL – Drain Induced Berrier Length

DQT – Direct Quantum Tunneling

DRAM – Dynamic Random Access Memory

EOT – Effective Oxide Thickness

ESCG – Extended Sidewall Control Gate

FeRAM – Ferro-electric Random Access Memory

FG – Floating Gate

F-N – Fowler-Nodheim

GAA – Gate-All-Around

GAA-FG – Gate-All-Aroound Floating Gate

GCR – Gate Capacitance Ratio

IPD – Interpoly-oxide Dielectric

IRDS – International Roadmap Device Structure

LPCVD – Low-Pressure Chemical Vapour Deposition

MOSFET – Metal-Oxide-Semiconductor Field Effect Transistor

MRAM – Magnetic Random Access Memory

NVM – Non-Volatile Memory

NW – Nanowire

P/E – Program/Erase

RAM – Random Access Memory

ROM – Read-Only-Memory

SRAM – Static Random Access Memory

SiNW – Silicon Nanowire

SCG – Sidewall Control Gate

SILC – Stress Induced Leakage Current

SONOS – Silicon-Oxide-Nitride-Oxide-Silicon

SiNWFET – Silicon Nanowire Field-Effect-Transistor

SS – Subthreshold Slope

S-SGT – Stacked Surroounding Gate Transistor

S-SCG – Separated Sidewall Control Gate

S/D – Source/Drain

TBE – Tunnel Barrier Engineering

VARIOT – Variable Oxide Thickness

VB – Valence Band

2D – 2-Dimensional

3D – 3-Dimensional

LIST OF SYMBOLS

A_{FN} – F-N coefficient

A_{gate} – area gate

A_{w} – area width

B_{FN} – F-N coefficient

E – electric field

E_{G} – band gap

I-V – current-voltage relationship

J_{g} – gate current density

L_{g} – gate length

m^* – effective mass

m_0 – electron effective mass

Q_{f} – fixed charges

T_{ox} – low-k tunnel oxide thickness

T_{hk} – high-k tunnel oxide thickness

T_{IPD} – intrepoly-oxide dielectric thickness

T_{FG} – floating gate thickness

V_{FG} – floating gate voltage

V_{g} – gate voltage

V_{prog} – program voltage

$V_{retention}$ – retention voltage

$V_{readdis}$ – read-disturb voltage

V_{th} – threshold voltage

V_{TP} – programmed threshold voltage

V_{TE} – erased threshold voltage

α_G – floating-to-control-gate-coupling coefficient

$_r$ – dielectric constant

Φ_B – barrier height

χ – electron affinity

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CHAPTER 1

INTRODUCTION

1.1 Research Background

Digital electronic advancement has led to the world economic growth in the late centuries. The example of modern digital electronics are high speed logic gate, sensors, increasing the number and size of pixels in digital camera and also memory capacity. Memory is one of the essential component in the modern electronic devices where it has been used commercially in personal computers, cellular phones, smart media, automotive system and etc. Memory is categorized into two types, which are volatile memory and non-volatile memory (NVM) as shown in Figure (1.1).

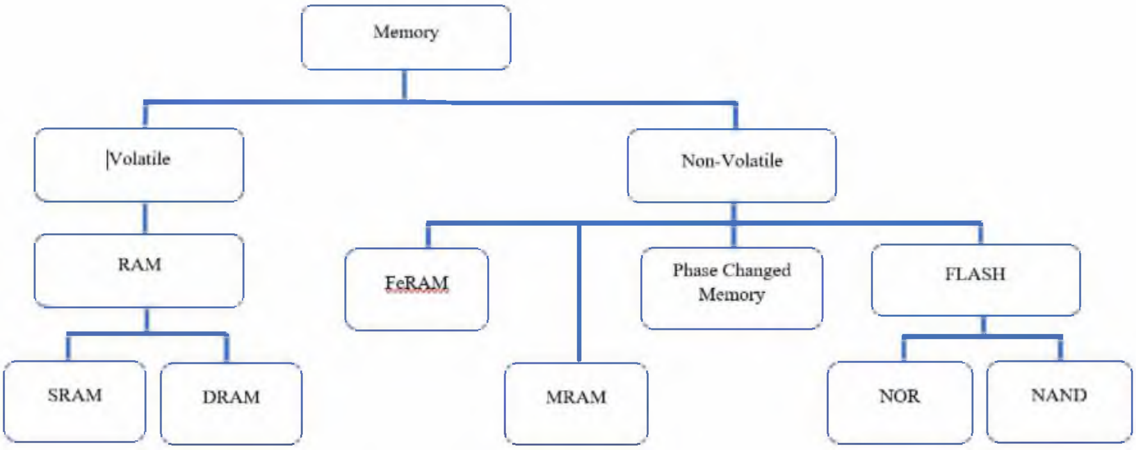

Figure 1.1 Complementary Metal-Oxide-Semiconductor (CMOS) memory device technology has been divided into two parts; volatile and non-volatile memory.[4]

Volatile memory is a computer memory that needs power to store data and it will lose the storage data when the power is off. It is known as Random-Access-Memory (RAM) and it is divided into two main categories which are Static-RAM (SRAM) and Dynamic-RAM (DRAM). SRAM is a cache memory which provides the fastest write/read (8ns) among all memories. However, SRAM cell density is very low because 6 transistors (6T) are required to occupy a single SRAM cell. Then, DRAM is introduced to overcome SRAM shortcoming where a single DRAM cell consists of one transistor and one capacitor (1T1C). There are many advantages of DRAM cell such as faster read operation speed, smaller cell size and low manufacturing cost except the write speed in DRAM is quite slower (50ns) than in SRAM. Even DRAM cell has many advantages unfortunately it is not a NVM where it needs power to retain data and the data retention is only 100ms in DRAM cell while it is 10 years in the flash memory.

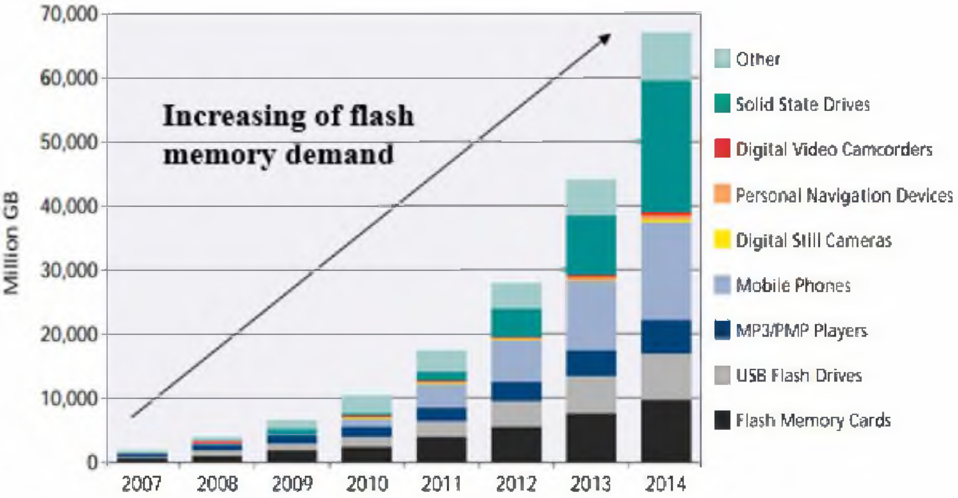

Figure 1.2 Flash Memory Demand from 2007 until 2014. It shows the increasing demand of flash memory in the market. (Source from Forward Insight)

Non-volatile memory (NVM) is one form of memory that retained memory and information in the absence of power and it is also referred as Read-Only-Memory (ROM) [4]. Nowadays, NVM technology become vital to the market due to the increasing demand in electronic devices such as cellular phones and laptop as shown in Figure 1.2. The important trait to make the NVM become indispensable is the capability to retain data after 10 years retention time and 10^4 endurance of P/E cycles (Source International Road-map Device Structure (IRDS) 2016 Edition). There are four different types of NVM either has been commercialized or are being developed in the industry: Ferro-electric Random Access Memory (FeRAM), Magnetic Random Access Memory (MRAM), Phase Changed Memory and Flash Memory. The performance and comparison of each type of memory is presented in Table 1.1 .Among these technologies, flash memory has many advantages for the following reasons:

1. Flash Memory has the biggest chip density as a single flash memory cell only consists of one transistor (1T). A FeRAM cell consists of one transistor and one capacitor (1T1C) meanwhile the MRAM cell contain one transistor and one magnetic tunnel junction (1T1M). Besides, Phase Changed Memory consists of one resistor and a bipolar junction transistor to demonstrate a changing phase of the memory.
2. Flash Memory presents multi-bit cell storage property compared to others by controlling charge storage amount in the floating gate cell. This will lead to the bigger memory capacity and lower the cost per bit significantly.
3. Flash Memory fabrication step is compatible to the conventional Complementary Metal-Oxide-Semiconductor (CMOS) process and it is alternative solution for the embedded memory applications. The structure of flash memory is simply easier to fabricate and integrate in which it only consisted of conventional Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) and floating gate(FG) memory cell sandwiched between silicon oxide, SiO_2 tunnel oxide and blocking oxide to form charge storage layer.

These three important advantages shows that flash memory is more reliable and promising to become the mainstream NVM nowadays. Nevertheless, flash memory also has some disadvantages as shown in Table 1.1 as flash memory device required longer time and higher voltage to program/erase its memory data. Thus, the scaling down of the flash memory must be continuously carried out to overcome flash memory's shortcomings to produce excellent device.

Table 1.1 NVM technology comparison between volatile memory (SRAM and DRAM) and non-volatile memory (Flash Memory, FeRAM, MRAM and Phase Changed Memory). From this Table, it can be summarized that flash memory shows the best performance and most compatible with the current CMOS process compared to other technology except its higher program/erase (P/E) voltage and slower P/E speed. [1]

Memory Name	SRAM	DRAM	Flash - NOR	Flash - NAND	FeRAM	MRAM	Phase Change Memory
Type	Volatile	Volatile	Non-Volatile (NV)	NV	NV	NV	NV
Cell Size Factor (F^2)	90~150	6~12	8~10	4	18	10~20	5~8
Largest Array Built (Mb)	-	-	256	2Gb	64	1	4
Multi-bit Storage	No	No	Yes	Yes	No	No	No
Relative Cost per Bit	High	Low	Medium	Medium	High		Low
3D Potential	No	No	Yes	Yes	No	No	No
CMOS Logic Compatibility	Good	Bad	Good	Good	Good		Good
Read/Program Voltage (V)	~1	~1	2/10	2/18	1.5/1.5	3.3/3.3	0.4/1
Program/Erase/Read Speed (ns)	8/8/8	50/50/8	1us/100ms/60ns		80/80/80	30/30/30	50/50/50
Direct Over-Write	Yes	Yes	No	No	Yes	Yes	Yes
Read Type	Destructive		Non-Destructive		Destructive		
Read Dynamic Range (margin)	100-200mV	100-200mV	Delta Current	Delta Current	100-200mV	20-40% R	10X-100XR
Endurance Write/Read	-	-	10^6	10^6	10^{12}	10^{14}	10^{12}
Retention Time	-	100ms	10 years	10 years	-	-	-
In production	Yes	Yes	Yes	Yes	Yes	2004	N/A

1.2 Flash Memory scaling and limitations

Nowadays, the minimum feature size of semiconductor flash memory technology has shrunk to 15nm and it's operational voltage is still more than 10V meanwhile the operational voltage for CMOS logic has been scaled down to a very small voltage, 1V. The semiconductor flash memory devices scaling is continuously expanding due to the growth of electronic device demand where FG has been commercialized as a charge storage layer as Figure 1.3shows the conventional FG structure. However, as the flash memory scaling technology node closer to sub 30nm, it faces several limitations as it is mostly comes from the device structures and materials.

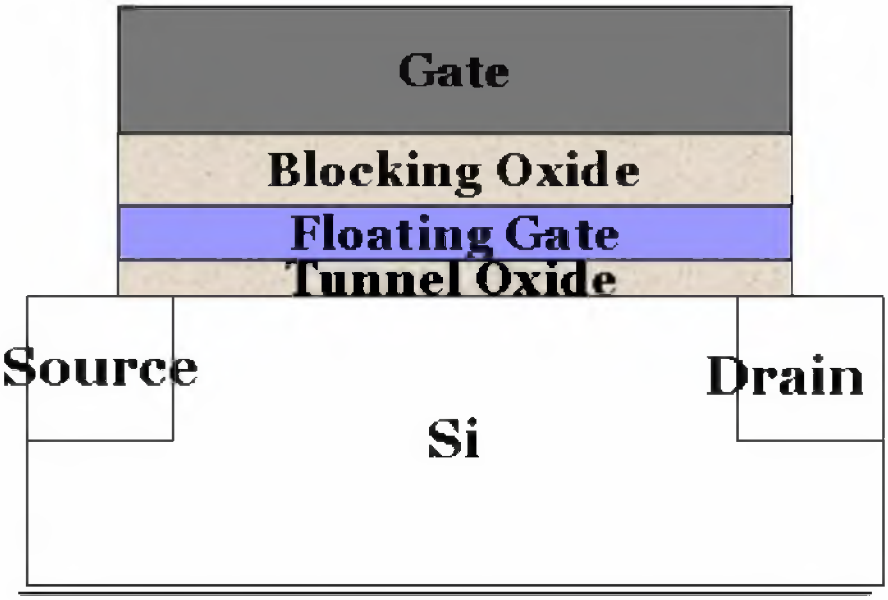

Figure 1.3 Device structure of FG flash memory showing each component of the cell.[5]

Commonly the scaling limitations will exist in each components of the FG flash memory cell such as tunnel oxide layer, poly-Si FG, interpoly-oxide dielectric (IPD) layer and poly-Si control gate. The main issue for each component in the FG cell is the inability to scale down the dielectric layers. For the tunnel oxide layer, the scaling limitation is the inability to scale down the layer itself. Conventionally, SiO_2 dielectric has been used as tunnel oxide layer because of its excellent interface properties with silicon, Si who has been used the a bulk. International Road-map

Device Structure (IRDS) 2016 has predicted the thickness limitation of the tunnel oxide layer is 6-7nm while maintaining the $4F^2$ cell size and major problems will arise if the thickness is reduced below this thickness limitation[4]. Therefore, due to the constraints and limitations to scale dielectric thickness of the two dimensional (2D) NAND flash memory, the three dimensional (3D) NAND flash memory is introduced where the memory density is increased by stacking more memory layers. However the cost per bit starts to increase after stacking several layers of device due to the additional photolithography process during 3D NAND flash memory fabrication as shown in the Figure 1.4.

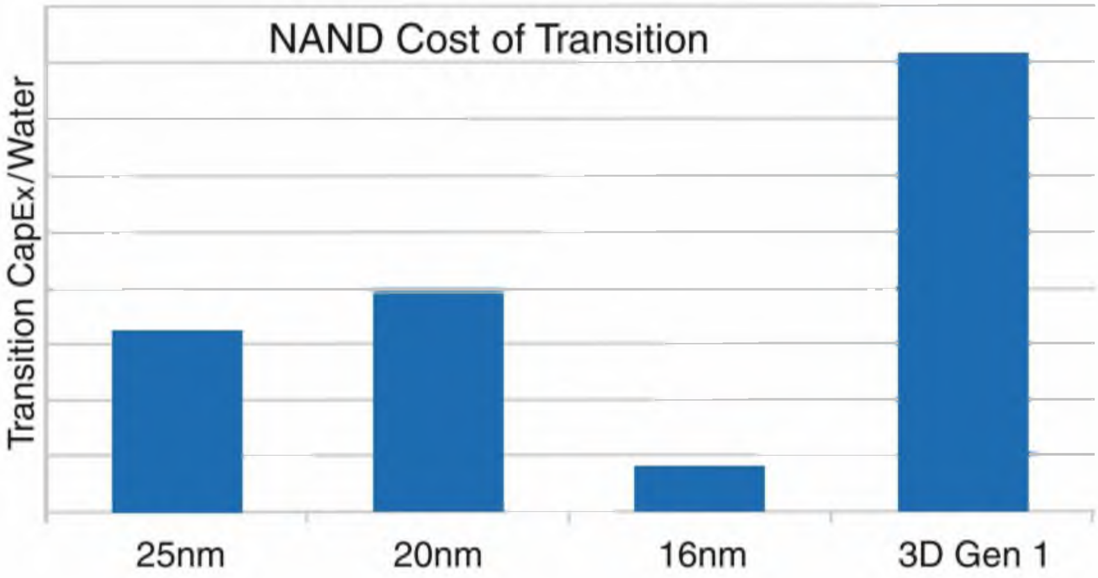

Figure 1.4 One time significant increase in capital expenditures for the first generation of 3D NAND which required more and complex fabrication process rather than required for the 2D NAND flash memory [2]. Y-Axis represents cost expenditure in billion for every different technology nodes.

In 2007, there is a technology that called Bits-Cost Scalable (BiCS) has been introduced to simplify the complicated fabrication steps of 3D NAND flash memory which offers big data and cheaper fabrication costs that subsequently boosts the flash memory industry. The essence of this technology has been its 'punch & plug' fabrication process in providing fewer lithography steps regardless of some stacked layers. The whole poly/oxide stacking is punched through to create holes before plugged by another electrode material to form the channel as shown in Figure 1.5.

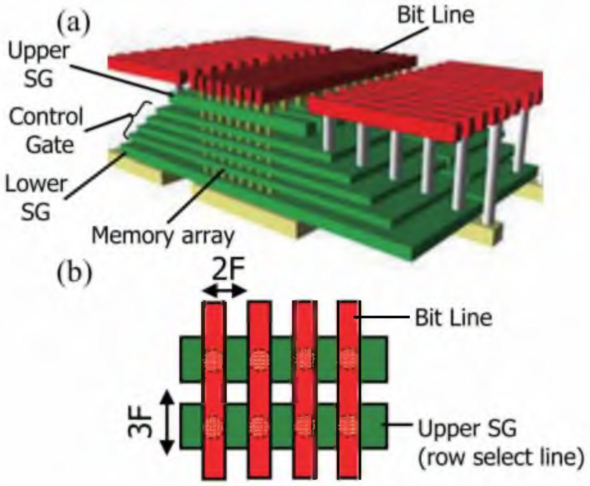

Figure 1.5 (a) Birds-eye view of BiCS flash memory, (b) Top down view of BiCS flash memory array[2].

The memory cell can be referred as gate-all-around (GAA) cell with either charge-trap (CT) or floating gate (FG) as the memory element. The CT 3D NAND cell arrays have been mainly researched due to simple cell process. Unlike 2D CT device, the CT nitride layer in the string of the planar 3D CT device is connected from bottom to top control gate (CG) along the channel side has led to the charge spreading issue, which is a bottleneck problem of 3D CT memory cell [2]. This causes the poor distribution of cell state and degradation of data retention characteristics. Meanwhile in 3D FG memory cell, the FG is completely surrounded by the tunnel oxide and IPD layers which becoming a reliable device structure without having any leakage path issue. This will lead to a better data retention and endurance characteristics that make the 3D FG memory cell becomes inevitable. In addition, 3D FG memory cell required lower operation voltage of 17-18V according to IRDS 2016 than planar 3D CT resulting to the highly enhanced device performance for 3D FG memory cell. The characteristics and comparisons between 3D FG and 3D CT are summarized in Table 1.2.

Table 1.2 Characteristics of 3D FG and 3D CT memory cell[2].

Characteristics	3D FG	3D CT
NAND cell size	Larger	Smaller
Manufacturing Step	More Complex	Complex
Scalability	Worse	Better
Endurance	Better	Worse
Data Retention	Better	Worse
Coupling/Interference	Not good	Better

1.3 Problem Statement

From the characteristics and comparisons shown in Table 1.2, some manufacturers like Micron focused on the development of 3D FG memory cell eventhough 3D CT memory cell has better scalability. In the last decade, many 3D FG NAND cell architectures have been proposed for example 3D Conventional FG (C-FG) [16] which is usually referred to as a 3D vertical FG cell. However C-FG cell may be susceptible to the cell-to-cell interference due to the poor FG coupling that require high programming voltage to process the data. Then, Gate-All-Around (GAA) C-FG cell with triangular Silicon Nanowire (SiNW) channel is proposed to reduce P/E voltage owing to the stronger electric field around the channel corners [17]. The nonlocalized trapping characteristics of the poly-Si FG made the injection of electrons easier during P/E process resulting in the high speed of P/E process. Nevertheless, the result also reported the charge loss of retention reliability after ten years of extrapolation is worse than 20% even though excellent P/E efficiency is demonstrated. To enhance the P/E efficiency, high electric field must be yielded in the tunnel oxide layer either by increasing the P/E voltages or by thinning the tunnel layer.

However, increasing the P/E voltages can cause over-programming to its neighboring cell, and thinning the tunnel layer will inevitably degrade its data retention capability due to electrons tunneling back into the channel during retention. Thus, inception of high-k dielectric material into the tunnel oxide layer becomes one of the excellent solutions, and it is often referred as Variable Oxide Thickness, VARIOT [18, 19, 20]. The previous study stated that VARIOT stack has high field sensitivity than single SiO_2 layer resulted in low P/E voltage, shorter P/E operation time and less leakage in long-term retention time [21]. Although the effect of incorporating the high-k dielectric material into the tunnel oxide layer is proven better; serious attention has been paid to the optimization of high-k dielectric materials based on their characteristics and suitability [15]. But considering the VARIOT distinct characteristics that has thicker physical thickness of tunnel oxide layer than single SiO_2 layer and high electric field yielding. So, it is expected to trade-off the P/E voltage and retention characteristic of the proposed device. From the literature review, with VARIOT technique can reduce percentage of charge loss with the right high-k materials.

1.4 Research Objectives

The main target of this research is to enhance the performance of GAA-FG memory cell by implementing the VARIOT concept based on the scaling limitations and trade-offs in C-FG cell, the research objectives are concluded as follow:

1. To determine the optimized VARIOT combination of low-k/high-k stack for GAA-FG cell with the minimum effective oxide thickness (EOT) and optimum low-k oxide thickness (T_{ox}) to offset the trade-off between P/E and reliability characteristics.
2. To characterize the electrical properties and reliability of the GAA-FG memory cell with optimized parameters from VARIOT optimization in terms of Data Retention and Data Endurance.

1.5 Research Scopes

The scopes of the research are summarized as below:

1. *Simulation Work*: The simulation work is divided into two parts; VARIOT optimization and the device simulation of the GAA-FG memory cell by using Technology-Computer-Aided-Design (TCAD). For VARIOT optimization, Silicon Nanowire (SiNW) structure is simulated with the given flash memory

constraints. Nevertheless, the tunnel barrier engineering of VARIOT concept is narrowed to asymmetric combination of low-k/high-k stack due to the fabrication limitation of symmetric combination. Afterwards, the device simulation of the GAA-FG memory cell with the optimized parameters is accessed to characterize and analyze the transfer characteristics and transient memory performances.

2. *Analysis Work*: The physical parameters and dimension of the GAA-FG memory cell are taken from the previous experimental work performed by [6]. However, cylindrical channel of GAA-FG cell is implemented in this research work instead of triangular channel as experimental work due to the vertical fabrication process issues. Furthermore, the physical transport between cylindrical and triangular channel is remain same to do the similar mechanism in the GAA-FG memory cell. The analysis work will be carried out to compare between the performance of GAA-FG with asymmetric VARIOT tunnel stack with the previously published work for 3D NAND structures [6].

1.6 Research Contribution

The significant contributions in this research can be highlighted as follow:

1. *VARIOT Optimization* : The optimization of VARIOT tunnel layer for multiple high-k dielectric materials where asymmetric combination of low-k/high-k stack is performed to determine the best asymmetric combination with optimum EOT and T_{ox} thickness. Then, the Fowler-Nodheim (F-N) coefficients have also been extracted for optimized parameters to be exploited in the next GAA-FG device characterization in analyzing the performances of the memory cell.
2. *GAA-FG with VARIOT tunnel layer* : The optimized parameters from VARIOT optimization can be employed as tunnel oxide layer in the memory cell devices to improve the P/E characteristics, its data retention as well as its data endurance.

1.7 Thesis Organization

Chapter 1 is the main root of this research where the memory devices background and its development are discussed. The various types of memory are discussed and the importance of flash memory is found as demand to the technology advancement. Then, flash memory scaling and challenges are highlighted in which the research's problem statements are determined. Based on the problem statements, the objectives of the research are proposed and the scope of the work has been identified. Finally, the research contributions has been highlighted and summarized in this chapter.

Chapter 2 discussed the 3D NAND cell structures of flash memory where multiple structures are identified and its characteristics are being highlighted. Furthermore, the concept of tunnel barrier engineering is discussed based on the types of dielectric stack as well as its physical transport. Then the transient parameters of the memory devices are also discussed to identify the physical mechanism in the devices.

Chapter 3 covers the research method of this work from the general flowchart and each technical flowchart such as VARIOT optimization and memory device characterization have been conducted to solve the problem statements. All of the research activities are listed in this chapter as well as the tools that were used in this research are highlighted. In addition, the approach details on the simulation work are presented and discussed such as dielectric material, optimization method, physical models, and device dimension. Lastly, the flow to characterize the memory device's reliability is summarized in the flowchart and discussed analytically.

In Chapter 4, the simulation results are presented which includes the optimization of VARIOT and characterization of GAA-FG memory device. The VARIOT optimized parameters are employed as tunnel oxide layer to analyze the transfer characteristics and transient performances of the GAA-FG memory cell. The simulation results on variation of low-k oxide thickness, T_{ox} in GAA-FG with VARIOT tunnel stack are also presented and discussed.

Finally, Chapter 5 conclude all the findings in this research and the research contributions are highlighted again. Besides, future works of this work are proposed to make sure the continuation of the research and contributions to the society.

REFERENCES

1. Meena, J. S., Sze, S. M., Chand, U. and Tseng, T. Y. Overview of emerging nonvolatile memory technologies. *Nanoscale Research Letters*, 2014. 9(1): 1–33.
2. Micheloni, R. *3D Flash Memories*. Dordrecht: Springer Netherlands. 2016.
3. Robertson, J. and Wallace, R. M. High-K materials and metal gates for CMOS applications. *Materials Science and Engineering R: Reports*, 2015. 88: 1–41.
4. Zhao, C., Zhao, C. Z., Taylor, S. and Chalker, P. R. Review on non-volatile memory with high-k dielectrics: Flash for generation beyond 32 nm. *Materials*, 2014. 7(7): 5117–5145.
5. Paolo, P., Luca, L. and Andrea, M. Floating Gate Devices: Operation and Compact Modeling [Book Review]. *IEEE Circuits and Devices Magazine*, 2006. 22(4): 33–33.
6. Lee, K. H., Tsai, J. R., Chang, R. D., Lin, H. C. and Huang, T. Y. Low- voltage high-speed programming/erasing floating-gate memory device with gate-all-around polycrystalline silicon nanowire. *Applied Physics Letters*, 2013. 103(15).
7. Endoh, T., Kinoshita, K., Tanigami, T., Wada, Y., Sato, K., Yamada, K., Yokoyama, T., Takeuchi, N., Tanaka, K., Awaya, N., Sakiyama, K. and Masuoka, F. Novel ultrahigh-density flash memory with a stacked-surrounding gate transistor (S-SGT) structured cell. *IEEE Transactions on Electron Devices*, 2001. 50(4): 945–951.
8. Seo, M. S., Park, S. K. and Endoh, T. 3-D vertical FG NAND flash memory with a novel electrical S/D technique using the extended sidewall control gate. *IEEE Transactions on Electron Devices*, 2011. 58(9): 2966–2973.
9. Aritome, S., Noh, Y., Yoo, H., Choi, E. S., Joo, H. S., Ahn, Y., Han, B., Chung, S., Shim, K., Lee, K., Kwak, S., Shin, S., Choi, I., Nam, S., Cho,G., Sheen, D., Pyi, S., Choi, J., Park, S., Kim, J., Lee, S., Hong, S., Park, S. and Kikkawa, T. Advanced DC-SF cell technology for 3-D NAND flash. *IEEE Transactions on Electron Devices*, 2013. 60(4): 1327–1333.

10. Aritome, S., Whang, S., Lee, K., Shin, D., Kim, B., Kim, M., Bin, J.,Han, J., Kim, S., Lee, B., Jung, Y., Cho, S., Shin, C., Yoo, H., Choi, S., Hong, K., Park, S. and Hong, S. A novel three-dimensional dual control-gate with surrounding floating-gate (DC-SF) NAND flash cell. *Solid-State Electronics*, 2013. 79(April 2016): 166–171.

11. Seo, M. S., Lee, B. H., Park, S. K. and Endoh, T. A novel 3-d vertical FG NAND flash memory cell arrays using the separated sidewall control gate (S-SCG) for highly reliable MLC operation. *3rd IEEE International Memory Workshop, IMW 2011*. IEEE. 2011. 1–4

12. Seo, M.-S., Lee, B.-H., Park, S.-K. and Endoh, T. Novel Concept of the Three-Dimensional Vertical FG nand Flash Memory Using the Separated- Sidewall Control Gate. *IEEE Transactions on Electron Devices*, 2012. 59(8):2078–2084.

13. Verma, S. *Tunnel Barrier Engineering for Flash Memory Technology*. Ph.D. Thesis. 2010.

14. Likharev, K. K. *(Theme 3) Crested Tunnel Barriers for Fast, Scalable, Nonvolatile Semiconductor Memories*. Technical Report 0704. 2006.

15. Verma, S., Pop, E., Kapur, P., Majhi, P., Parat, K. and Saraswat, K. C. Feasibility Study of Composite Dielectric Tunnel Barriers for Flash Memory. *2007 65th Annual Device Research Conference*. IEEE. 2007, vol. 24.

16. Prince, B. *Vertical 3D Memory Technologies*. vol. 9781118760. Chichester, United Kingdom: John Wiley Sons Ltd. 2014.

17. Tsai, J.-R., Lee, K.-H., Lin, H.-C. and Huang, T.-Y. Gate-all-around floating-gate memory device with triangular poly-Si nanowire channels. *Japanese Journal of Applied Physics*, 2014. 53(4S): 04ED14.

18. Jain, S., Gupta, D., Neema, V. and Vishwakarma, S. BE-SONOS flash memory along with metal gate and high-k dielectrics in tunnel barrier and its impact on charge retention dynamics. *Journal of Semiconductors*, 2016. 37(3): 1–6.

19. Jung, J. and Cho, W.-J. Tunnel Barrier Engineering for Non-Volatile Memory. *J. Semi. Technol. Science*, 2008. 8(1): 29–32.

20. Govoreanu, B., Degraeve, R., Van Houdt, J. and Jurczak, M. Statistical investigation of the floating gate memory cell leakage through high-k interpoly dielectrics and its impact on scalability and reliability. *Technical Digest - International Electron Devices Meeting, IEDM.* IEEE. 2008.

21. Verma, S., Pop, E., Kapur, P., Parat, K. and Saraswat, K. C. Operational Voltage Reduction of Flash Memory Using High-κ Composite Tunnel Barriers. *IEEE Electron Device Letters*, 2008. 29(3): 252–254. ISSN 0741-3106.doi:10.1109/LED.2007.915376.

22. Hamzah, A. *Charge-Based Compact Model of Gate-All-Around Floating Gate Nanowire with Variable Oxide Thickness forFlashMemory Cell.* Ph.D. Thesis. Universiti Teknologi Malaysia. 2018.

23. Likharev, K. K. Layered tunnel barriers for nonvolatile memory devices. *Applied Physics Letters*, 1998. 73(15): 2137–2139.

24. Govoreanu, B., Blomme, P., Rosmeulen, M., Van Houdt, J. and De Meyer, K. Variot: A novel multilayer tunnel barrier concept for low-voltage nonvolatile memory devices. *IEEE Electron Device Letters*, 2003. 24(2): 99–101.

25. Hamzah, A., Ezaila Alias, N. and Ismail, R. Low-voltage high-speed programming gate-all-around floating gate memory cell with tunnel barrier engineering. *Japanese Journal of Applied Physics*, 2018. 57(6): 1–20.

26. Sillvaco. *User' S Manual.* Technical Report 408. Silvaco. 2015.

27. Govoreanu, B., Blomme, P., Van Houdt, J. and De Meyer, K. Simulation of nanofloating gate memory with high-k stacked dielectrics. *International Conference on Simulation of Semiconductor Processes and Devices, SISPAD.* IEEE. 2003, vol. 2003-January.

28. Salmani-Jelodar, M., Ilatikhameneh, H., Kim, S., Ng, K., Sarangapani, P. and Klimeck, G. Optimum high-k oxide for the best performance of ultra-scaled double-gate mosfets. *IEEE Transactions on Nanotechnology*, 2016. 15(6): 904–910.

LIST OF PUBLICATIONS

International Conference

1. Farah A.Hamid , Afiq Hamzah , N. Ezaila Alias and Razali Ismail, Optimization of High-k Composite Dielectric Materials of Variable Oxide Thickness Tunnel Barrier for Nonvolatile Memory, (2019). 4th International Conference on Electronic Design, August 2018. (Oral Presentation)

Journal with Impact Factor

2. Farah A. Hamid, N. Ezaila Alias, Zaharah Johari, Afiq Hamzah, M. L. Peng Tan and Razali Ismail, Effect of Low-k Oxide Thickness Variation on Gate-All-Around Floating Gate with Optimized SiO2/La2O3 Tunnel Barrier. Material Research Express [Q3, IF=1.449]. DOI:10.1088/2053-1591/ab2869

Indexed Journal (SCOPUS)

3. Farah A.Hamid , Afiq Hamzah , N. Ezaila Alias and Razali Ismail, Optimization of High-k Composite Dielectric Materials of Variable Oxide Thickness Tunnel Barrier for Nonvolatile Memory, (2019).Indonesian Journal of Electrical Engineering and Computer Science, 14(2), pp 765-772. DOI:10.11591/ijeecs.v14.i2.pp765-772.