MODELLING AND SIMULATION OF 2D ALUMINIUM-DOPED SILICENE TRANSPORT PROPERTIES IN FIELD-EFFECT TRANSISTORS

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ABSTRACT

One of the more-than-Moore approaches is to use two-dimensional (2D) silicene as the channel in a transistor. Silicene shares outstanding electronic properties with graphene, yet provides an added advantage in terms of its compatibility with silicon (Si) wafer technology. However, pristine silicene has an almost zero bandgap at the Dirac point, which inhibits its potential as a field-effect transistor (FET). This study focused on the modelling and simulation of bandgap-engineered silicene FETs from material level to device level. Concerning material-level modelling, the nearest neighbour tight-binding (NNTB) model was used to obtain the dispersion (E-k) relation and density of states (DOS) of pristine silicene. A bandgap was then induced in silicene using aluminium (Al) substitutional doping at a uniform concentration to produce the $AlSi_3$ nanosheet. Applying this uniform doping technique, the locations of dopants are not restricted, unlike selective substitutional doping where the electronic properties vary with the doping locations. Al is among the most promising dopants for silicene because it does not distort the honeycomb lattice arrangement. The E-k relation and DOS of $AlSi_3$ were also obtained. Subsequently, the DOS and Fermi-Dirac probability distributions were used to compute the carrier transport properties of $AlSi_3$. Regarding the device-level modelling, the top-of-the-barrier (TOB) ballistic nanotransistor model was employed to simulate the proposed $AlSi_3$ FET model in terms of its output characteristics ($I_{DS} - V_{DS}$) and transfer characteristics ($I_{DS} - V_{GS}$). The device performance of the $AlSi_3$ FET was evaluated by benchmarking against published results in terms of device metrics such as threshold voltage (V_{th}), drain-induced barrier lowering (DIBL), subthreshold swing (SS) and on-off current (I_{on}/I_{off}) ratio. The $AlSi_3$ FET exhibits SS as low as $67.8\,mV/dec$, which is close to the ideal SS at room temperature (approximately $60\,mV/dec$), DIBL of $48.2\,mV/V$, and I_{on}/I_{off} ratio up to an order of five (approximately 2.6×10^5). The proposed $AlSi_3$ FET outperforms the Si FinFET (SS and DIBL reduction of approximately 46 % and 32 %, respectively, and I_{on}/I_{off} ratio improvement of approximately 10^2) and exhibits a device performance that is comparable to that of other low-dimensional materials. Subsequently, a SPICE model was created to facilitate further circuit-level simulation. This study demonstrates that $AlSi_3$ is one of the most promising 2D materials for modern nanoelectronic applications.

ABSTRAK

Salah satu pendekatan *more-than-Moore* adalah dengan menggunakan *silicene* dua dimensi (2D) sebagai saluran dalam transistor. *Silicene* berkongsi sifat elektronik yang luar biasa dengan grafin, malah terdapat kelebihan tambahan dari segi keserasiannya dengan teknologi wafer silikon (Si). Walau bagaimanapun, *silicene* asli mempunyai sela jalur yang hampir sifar pada titik *Dirac*, yang menghalang potensinya sebagai transistor kesan medan (FET). Penyelidikan ini memberi tumpuan kepada pemodelan dan simulasi untuk FET *silicene* yang mana sela jalurnya telah diubahsuai dari tahap bahan hingga tahap peranti. Pada pemodelan tahap bahan, model ikatan ketat terdekat (NNTB) digunakan untuk mendapatkan hubungan serakan (E-k) dan ketumpatan keadaan (DOS) *silicene* asli. Sela jalur kemudiannya diaruh ke dalam *silicene* menggunakan pengedopan gantian aluminium (Al) pada kepekatan seragam, untuk menghasilkan *nanosheet* $AlSi_3$. Dengan menggunakan teknik pengedopan seragam ini, lokasi bahan dop adalah tidak terbatas, berbeza dengan pengedopan gantian selektif di mana sifat elektronik berubah mengikut lokasi bahan dop. Al adalah antara bahan dop yang paling sesuai untuk *silicene* kerana ia tidak memutarbelitkan susunan kekisi heksagon. Hubungan E-k dan DOS untuk $AlSi_3$ juga diperoleh. Seterusnya, DOS dan taburan kebarangkalian *Fermi-Dirac* digunakan untuk menghitung sifat pengangkutan pembawa dalam $AlSi_3$. Pada pemodelan tahap peranti, model *nanotransistor* sawar-teratas (TOB) balistik digunakan untuk mensimulasi model FET $AlSi_3$ yang dicadangkan dari segi ciri keluaran ($I_{DS} - V_{DS}$) dan ciri pemindahan ($I_{DS} - V_{GS}$). Prestasi FET $AlSi_3$ dibandingkan dengan hasil terbitan lain dari segi metrik peranti seperti voltan ambang (V_{th}), penurunan sawar aruhan-saliran (DIBL), ayunan subambang (SS) dan nisbah arus buka-tutup (I_{on}/I_{off}). FET $AlSi_3$ menghasilkan SS serendah $67.8\,mV/dec$, yang hampir dengan SS ideal pada suhu bilik (lebih kurang $60\,mV/dec$), DIBL pada $48.2\,mV/V$ dan nisbah I_{on}/I_{off} hingga tertib ke-lima (lebih kurang 2.6×10^5). FET $AlSi_3$ yang dicadangkan mengatasi Si FinFET (pengurangan SS dan DIBL lebih kurang 46 % dan 32 %, masing-masing, dan peningkatan nisbah I_{on}/I_{off} lebih kurang 10^2) dan menunjukkan prestasi peranti yang setanding dengan material dimensi rendah yang lain. Seterusnya, model SPICE dihasilkan untuk memudahkan simulasi tahap litar selanjutnya. Kajian ini menunjukkan bahawa $AlSi_3$ adalah antara bahan 2D yang berpotensi untuk aplikasi nanoelektronik moden.

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LIST OF ABBREVIATIONS

1D	–	one-dimensional
2D	–	two-dimensional
3D	–	three-dimensional
Al	–	aluminium
$AlSi_3$	–	aluminium-doped silicene with uniform concentration
ASiNR	–	armchair silicene nanoribbon
B	–	boron
Br	–	bromine
BP	–	black phosphorene
BTE	–	Boltzmann's transport equation
BZ	–	Brillouin Zone
C	–	carbon
Cl	–	chlorine
CBM	–	conduction band minimum
CMOS	–	complementary metal–oxide–semiconductor
CNT	–	carbon nanotube
CPU	–	central processing unit
DFT	–	density functional theory
DG	–	dual-gated
DIBL	–	drain-induced barrier lowering
DOS	–	density of states
DV	–	divacancy
E-k	–	dispersion

ERM	–	emerging research material
F	–	Fluorine
FDI	–	Fermi-Dirac integral
FET	–	field-effect transistor
FM	–	ferromagnetic
GNR	–	graphene nanoribbon
GeNR	–	germanene nanoribbon
h-BN	–	hexagonal boron nitride
H	–	hydrogen
I	–	iodine
IC	–	integrated circuit
IRDS	–	International Roadmap for Devices and Systems
ITRS	–	International Technology Roadmap for Semiconductors
I-V	–	current-voltage
LOP	–	low operating power
LSTP	–	low-standby power
MATLAB	–	Matrix Laboratory
MBE	–	molecular beam epitaxy
MFP	–	mean free path
MOS	–	metal oxide semiconductor
MOSFET	–	metal-oxide-semiconductor field-effect transistor
MV	–	monovacancy
N	–	nitrogen
NEGF	–	non-equilibrium Green's function
NNTB	–	nearest neighbour tight-binding
O	–	oxygen

P	–	phosphorus
RMSD	–	root mean square deviation
SG	–	single-gated
Si	–	silicon
SiNR	–	silicene nanoribbon
SiNS	–	silicon nanosheet
SiNW	–	silicon nanowire
SOI	–	silicon-on-insulator
SPICE	–	simulation program with integrated circuit emphasis
SS	–	subthreshold swing
SW	–	Stone-Wales
TB	–	tight-binding
TFET	–	tunneling field-effect transistor
TOB	–	top-of-the-barrier
UTM	–	Universiti Teknologi Malaysia
VBM	–	valence band maximum
WOS	–	Web of Science
ZSiNR	–	zigzag silicene nanoribbon
ZZ	–	zigzag

LIST OF SYMBOLS

a_0	–	lattice constant
C_D	–	drain capacitance
C_G	–	gate capacitance
C_{Geff}	–	effective gate capacitance
C_{OX}	–	oxide capacitance
C_Q	–	quantum capacitance
C_Σ	–	total terminal capacitance
d	–	atomic bonding length
$DIBL$	–	drain-induced barrier lowering
DOS_e	–	DOS for electron
DOS_h	–	DOS for hole
e	–	elementary charge constant
E	–	total energy
E_{0Si}	–	onsite energy of silicon
E_{0Al}	–	onsite energy of aluminium
E_{c0}	–	energy at the conduction band minimum point
E_F	–	Fermi energy level
E_{FD}	–	Fermi energy level at drain terminal
E_{FS}	–	Fermi energy level at source terminal
E_g	–	energy bandgap
E_l	–	transverse electric field
E_{v0}	–	energy at the valence band minimum point
E_z	–	transverse electric field

$\mathcal{F}_j$	–	Fermi-Dirac integral of j^{th} order
h	–	Planck's constant
$\hbar$	–	reduced Planck's constant
$\hat{H}$	–	Hamiltonian operator
$I_{DS} - V_{GS}$	–	transfer characteristics
$I_{DS} - V_{DS}$	–	output characteristics
I_{off}	–	off-current
I_{on}	–	on-current
I_{DS}	–	drain current
k	–	wave vector
k_B	–	Boltzmann constant
k_x	–	x-component of wave vector
k_y	–	y-component of wave vector
L	–	channel length
l_{ap}	–	MFP of acoustic phonon scattering
l_{op}	–	MFP of optical phonon scattering
L_{Si}	–	length of quasi-1D silicene
M	–	number of modes
m_e^*	–	electron effective mass
m_h^*	–	hole effective mass
n_{AlSi_3}	–	electron concentration of $AlSi_3$
N_A	–	width of ASiNR
N_c	–	effective DOS for electron
N_v	–	effective DOS for hole
N_Z	–	width of ZSiNR
p	–	positive integer for nanoribbon family

p_{AlSi_3}	–	hole concentration of $AlSi_3$
P_0	–	equilibrium hole concentration
P_g	–	pressure in vacuum condition
P_D	–	hole concentration at drain terminal
P_S	–	hole concentration at source terminal
q	–	electric charge constant
Q_{top}	–	charge at the TOB
r	–	position of a particle
R_g	–	growth rate
SS	–	subthreshold swing
T	–	lattice temperature
t_{OX}	–	oxide thickness
t_{Si-Si}	–	hopping integral of Si-Si bond
t_{Si-Al}	–	hopping integral of Si-Al bond
t_{Al-Si}	–	hopping integral of Al-Si bond
T_g	–	growth temperature
U	–	channel potential
U_L	–	Laplace potential
U_P	–	floating potential
U_{SCF}	–	self-consistent potential
v_h	–	average hole velocity
v_{ih}	–	intrinsic hole velocity
v_{inj}	–	average carrier injection velocity
v_{thp}	–	thermal velocity of hole
V_{bias}	–	bias voltage
V_{th}	–	threshold voltage

V_{DD}	–	maximum supply voltage
V_{DS}	–	drain voltage
V_{GS}	–	gate voltage
W	–	width of channel material
α_G	–	gate capacitance coupling factor
α_D	–	drain capacitance coupling factor
α_S	–	source capacitance coupling factor
Γ	–	Gamma function
ΔP	–	net mobile charge
Δz	–	buckling displacement
ε_0	–	vacuum permittivity
ε_r	–	relative permittivity
η	–	normalised thermal energy
η_c	–	normalised thermal energy for conduction band
η_v	–	normalised thermal energy for valence band
θ	–	angle between atomic bonds
ρ	–	momentum of a particle
ϕ_0	–	wavefunction
ψ	–	wavefunction of a quantum mechanical system

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CHAPTER 1

INTRODUCTION

1.1 Research background

A field-effect transistor (FET) is a three-terminal electronic device, which commonly has the architecture of a conduction channel controlled by a gated insulating layer. FETs are known to be the core boosting the advancement of modern semiconductor industry [1]. In the past few decades, in particular since 1960s, innovation in the semiconductor industry has been driven by Moore's law [2] and Dennard's scaling [3]. Gordon Moore projected that the packing density of transistors in a central processing unit (CPU) chip was going to be doubled every $18 - 24$ months as shown in Figure 1.1, owing to the maturity and cost effectiveness of the integrated circuit (IC) technology [4]. Notable inventions in the semiconductor industry include the IC, metal-oxide-semiconductor field-effect transistor (MOSFET) and complementary metal–oxide–semiconductor (CMOS) technology.

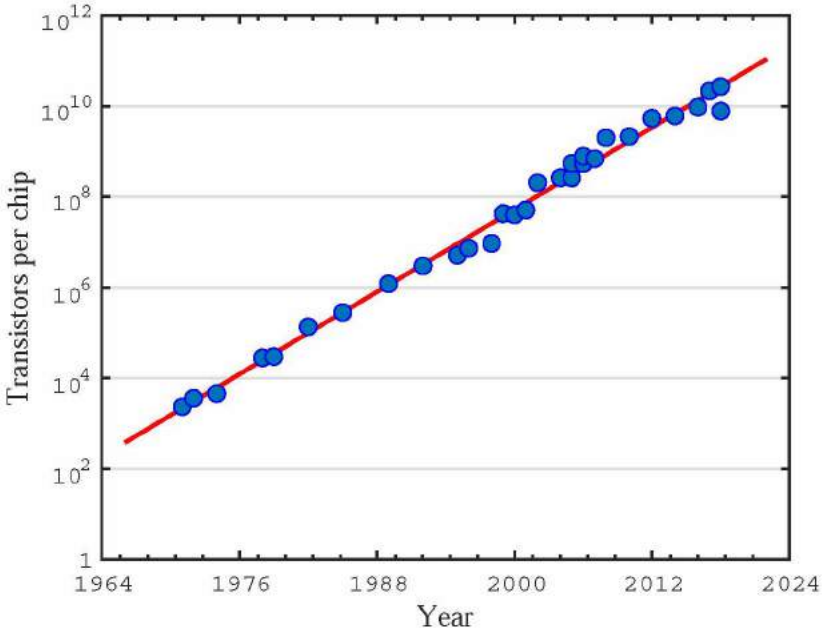
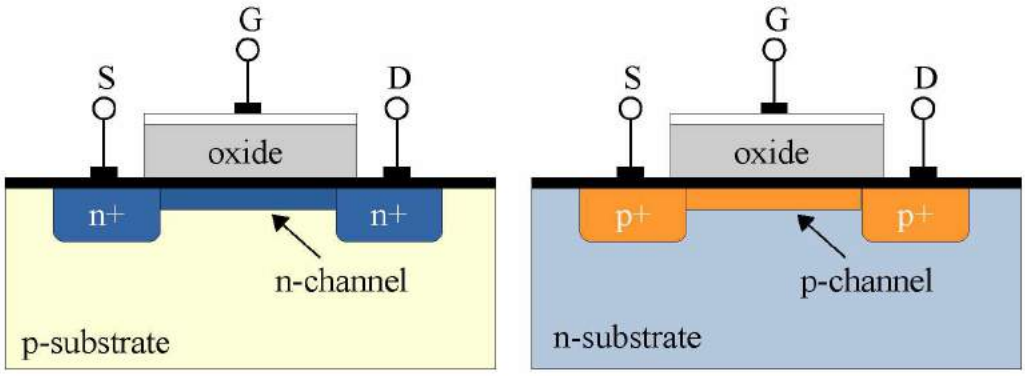


Figure 1.1: Moore's law [5].



(a) n-channel MOSFET (b) p-channel MOSFET

Figure 1.2: Schematic cross-section diagrams of enhancement mode MOSFETs. A conducting channel is induced between the source and drain when the gate voltage is above the so-called threshold voltage [6].

A CPU chip consists of a large number of CMOS circuits, that enables it to perform various calculations and logic functions. To date, the semiconductor industry has been able to integrate 39.54 billion transistors in a single CPU chip [7]. The CMOS technology was first demonstrated by Atalla and Kahng in Bell Labs in 1960 [8]. A CMOS circuit combines n-channel and p-channel MOSFETs (depicted in Figure 1.2) to build various logic gates for digital applications. In 1963, Wanlass and Sah, with Fairchild Semiconductor at the time, adapted Bell Labs' ideas and refined CMOS circuits for them to be more power- and area-efficient [9]. The remarkable invention of CMOS and IC technologies drove the success of the semiconductor industry and improved the technology of the modern world. In fact, the computing power of a CPU increases when the chip makers are able to pack more transistors inside a single chip by reducing the transistor size. However, transistor scaling is approaching its fundamental limits owing to the shortcomings of materials and fabrication technology. The semiconductor industry has been facing difficulties in sustaining Moore's law since the late 1990s [10].

As the semiconductor industry continued to grow, the semiconductor community decided to collaborate internationally to overcome major challenges in the industry. In 1998, a team of semiconductor industry experts from Europe, Japan, Korea, Taiwan, and the United States began to produce an annually updated roadmap,

namely the International Technology Roadmap for Semiconductors (ITRS) [11]. The primary objective of this roadmap was to provide the main reference for the research and development in both industry and academia. Following the introduction of mobile devices, such as smartphones and tablets, the ITRS was reorganised and renamed in 2013 as ITRS 2.0 to address the new ecosystem for the semiconductor industry.

In 2016, the International Roadmap for Devices and Systems (IRDS) [12] was initiated to succeed the ITRS 2.0. The refined scope of IRDS is wider and extend beyond "More Moore" initiatives, which were particularly stressed in ITRS 2.0. Interestingly, the emerging research material (ERM) focus team in IRDS 2017 listed two-dimensional (2D) materials as one of the solutions for transistor scaling and integration, as summarised in Table 1.1. Although 2D materials are substantially advantageous over conventional bulk materials, several major challenges still exist for 2D materials. Bandgap engineering in 2D materials must also be developed and optimised for various applications [13]. Thus, researchers must aggressively seek to resolve these issues and meet practical industrial needs [14, 15].

Table 1.1: Potential advantages and challenges of 2D materials for transistor scaling and integration (extracted from IRDS 2017 [12]).

Emerging Material	Potential Advantages	Challenges
2D Materials	• High mobility • Good channel control • Possibility of heterostructure and tunneling devices	• Techniques for doping • Improvement of contact resistance • Large area synthesis with low defect density

Recently, transistors have been scaled down to sub-10-nm regime, where they comprise from tens to a few atoms per device [5]. In this nanoscale regime, the modelling of semiconductor materials and electronic transport incorporating quantum-mechanical properties [16] has become an interesting research subject. The semi-classical transport model derived from Boltzmann's transport equation (BTE) can no longer accurately describe the electronic properties of such devices. The BTE model

must be modified by including the quantum-mechanical effects of carriers, which are described by Schrödinger equation in terms of wave functions [17]. Modelling of low-dimensional devices using this bottom-up approach under certain constraints can clearly describe and correctly predict the transport properties within the devices.

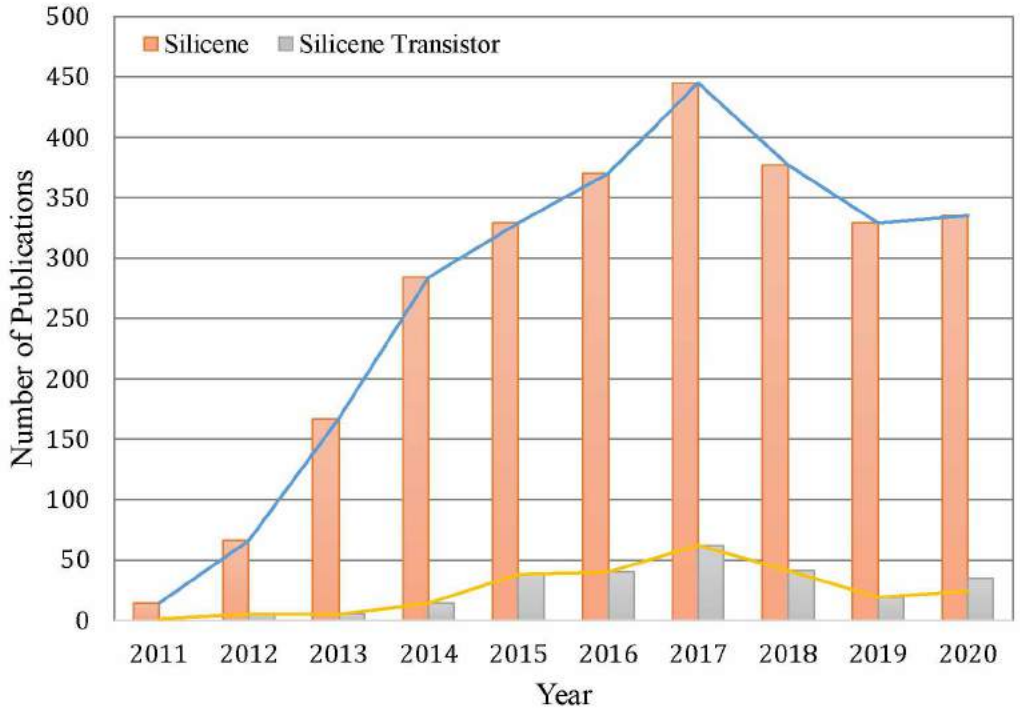


Figure 1.3: Trend of recent publications resulting from the topic search function available in the WOS database by Clarivate Analytics; silicene (red bars) and silicene transistor (grey bars) were employed as search keywords (accessed in 2021).

Research studies involving 2D materials were pioneered by the discovery of stable single-layer graphene by Novoselov *et al.* [18]. As a result, many other 2D materials, such as transition metal dichalcogenides, hexagonal boron nitride (h-BN), phosphorene, germanene, and silicene, were also explored. Silicene is particularly interesting because it is a monolayer allotrope derived from silicon (Si). Although the properties of silicene was theoretically predicted in 1994 by Takeda and Shiraishi [19], it did not attract much research interest until recently due to the major challenges in the fabrication technology. The success of graphene since 2004 [18], has stimulated the 2D materials-based research domain, leading to the rise of silicene-based studies. In 2015, the first silicene-based FET was fabricated by Tao's group [20]. Increasing research interest on silicene can be observed from the number of silicene-based publications

(indexed in the Web of Science by Clarivate Analytics), as depicted in Figure 1.3. However, less than 10 % of these studies were conducted on silicene-based transistors. Therefore, it is interesting to explore this topic further.

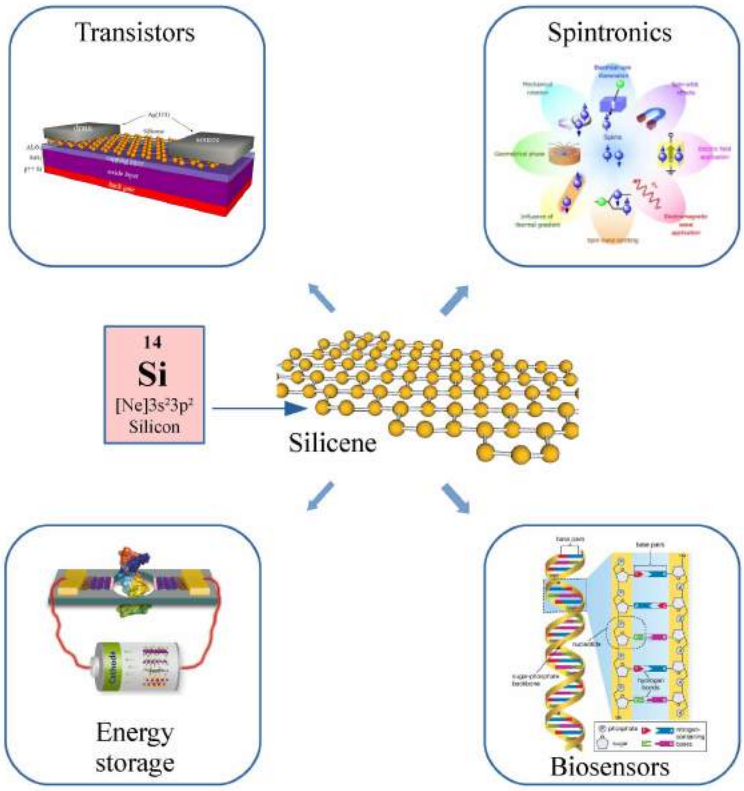


Figure 1.4: Potential applications of silicene nanosheets [21].

Similar to graphene [22, 23], silicene [24, 25] is a monolayer material consisting of Si atoms arranged in a honeycomb structure possessing a Dirac cone (with almost zero gap) in the bandstructure. This atomically thin property (the atomic radius of a silicon atom is approximately $0.12\,nm$ [26]), could provide the ultimate channel thickness scaling for nanoelectronic devices [27]. In addition, the FETs based on 2D materials can be used to create high-performance and low-power device technologies [28, 29]. Hence, 2D materials are among the most suitable candidates for creating a new generation of nanoelectronic devices, such as wearable and flexible devices, owing to their stable and atomically thin structure [30, 31]. Figure 1.4 shows the potential applications of silicene nanosheets [21]. Silicene has been identified as a 2D material that can improve transistor [20], spintronics [32], energy storage [33], and biosensors [34] applications.

Because of the fact that silicene is derived from Si, which is widely used in the fabrication of transistors, it has recently become a material of great interest [20]. In contrast to graphene, which requires redesigned fabrication equipment, silicene is potentially compatible with present Si-wafer fabrication processes. However, unlike graphene, which can be mechanically exfoliated from the bulk (i.e., graphite, which exists naturally) counterparts, the development of a technique that can synthesize high-quality free-standing silicene still constitutes a major challenge for researchers [35, 36]. This is why the majority of the silicene-based studies are still conducted through computational tools.

In short, computational studies to predict the electronic, carrier transport, and current transport properties of silicene-based nanoelectronic devices are very useful at the present stage. Moreover, it is important to tune the bandgap of silicene and explore the performance of bandgap-engineered silicene as a transistor. In this study, the modelling and simulation of a silicene-based transistor was conducted via nearest neighbour tight-binding (NNTB) and top-of-the-barrier (TOB) nanotransistor models to obtain its electronic and current transport properties. The performance of the transistor was also assessed by benchmarking against selected published models.

1.2 Problem statement

Silicene, as a potential 2D candidate for the future generation of electronic devices, has recently become an important research topic in the nanoelectronic research community. However, pristine silicene has an almost zero bandgap at the Dirac point, similar to graphene, which inhibits its potential as a FET. Hence, the essential physics behind bandgap engineering techniques to induce a bandgap in silicene should be extensively explored. Owing to the high cost and major challenges in the fabrication of silicene-based devices at this early stage, computational modelling and simulations could provide a fundamental understanding of the material before rigorous experimental efforts are invested. The issues that were bound to be addressed in this study include:

Issue 1: Electronic properties of pristine silicene and aluminium (Al)-doped silicene.

The fundamental electronic properties, including the bandstructures and density of states (DOS), of nanoelectronic materials are requisites prior to extended studies at device level. There is still a lack of details regarding the DOS of Al-doped silicene ($AlSi_3$) although Ding *et al.* [37] developed a density functional theory (DFT) model on $AlSi_3$, confirming its semiconducting electronic properties. Moreover, obtaining simple closed-form solutions from computationally expensive DFT model [38] constitutes a remarkable challenge. Thus, it is interesting to explore NNTB models for $AlSi_3$ for further insights into this promising semiconducting 2D material.

Issue 2: Carrier transport properties of Al-doped silicene.

Prior to applying $AlSi_3$ as the channel of a transistor, it is crucial to investigate its intrinsic carrier transport properties through the bandstructure and DOS. However, previous models on $AlSi_3$ were developed at material level; thus, the main findings of previous works were limited to information on the structural stability, bandstructures, and magnetic properties of the material.

Issue 3: Device performance of Al-doped silicene employed as the channel of an FET.

The commonly computed current-voltage (I-V) characteristics for a FET include the transfer and output characteristics curves. Nevertheless, it is difficult to justify and benchmark the performance of simulated I-V characteristics by merely analysing the transfer and output characteristics curves. In this study, the device performance of the $AlSi_3$ FET was justified by using appropriate transistor device metrics from the transfer and output characteristics curves.

1.3 Research Objectives

Unlike other 2D materials such as graphene and MoS_2 monolayers which require entirely redesigned fabrication equipment and techniques, silicene is potentially compatible with the Si-dominant semiconductor industry due to its Si atoms nature [20]. The primary aim of this study was to model and simulate the bandgap-engineered silicene from the material (atomic) level up to the transistor (device) level. On the basis of a systematic review of the existing literature (as discussed in Chapter 2), the objectives of this study were outlined as:

1. To model and analyse the dispersion (E-k) relation and DOS of pristine silicene and doped-silicene with Al at uniform concentration using the NNTB model and parabolic band assumptions.
2. To investigate the carrier transport properties of silicene doped with Al at uniform concentration along the zigzag transport direction, including the intrinsic carrier concentrations, intrinsic velocity, and ideal ballistic current transport.
3. To explore the device performance of Al-doped silicene FET by assessing the I-V characteristics using the TOB transistor model and benchmarking the results against other published studies in terms of device performance metrics, namely the threshold voltage (V_{th}), subthreshold swing (SS), drain-induced barrier lowering ($DIBL$), and on-current to off-current (I_{on}/I_{off}) ratio. A SPICE-compatible model was also inspected to facilitate future work at circuit-level simulation.

1.4 Research Scopes

This study is done based on computational modelling and simulation, with a focus on silicene and doped-silicene at material and device levels. The computational tools employed include Mathematica and MATLAB, which are licensed by Universiti Teknologi Malaysia (UTM). Some of the models were derived, simplified and verified using Mathematica to ensure accuracy. The models were then simulated using

MATLAB. The electronic properties that were computed include E-k relations and the DOS of pristine and Al-doped silicene; the NNTB model was used. The bandgap engineering technique used in this study to induce the bandgap in silicene was uniform substitutional doping of Al. The bandgap was obtained by computing the difference between the minimum point of the conduction band and the maximum point of the valence band. In this study, within the NNTB model, the Fermi energy levels for the bandstructures were always set to zero.

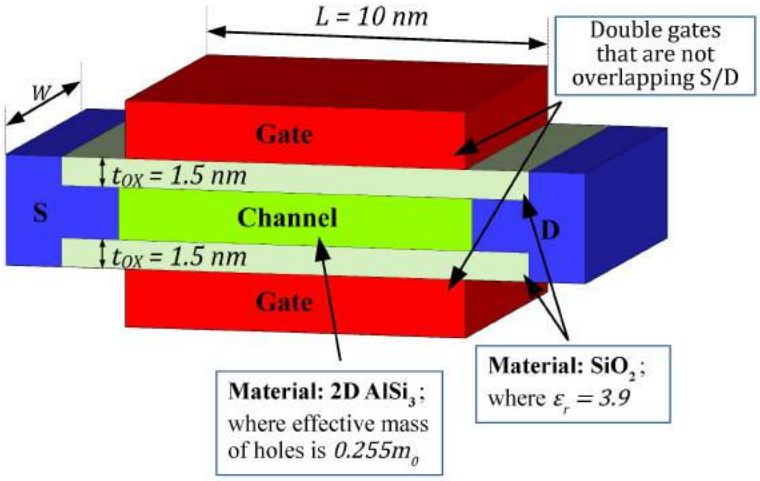


Figure 1.5: Proposed $AlSi_3$ transistor model with its device parameters.

Subsequently, the electronic and carrier transport properties of $AlSi_3$ were applied to the TOB nanotransistor model to obtain the I-V characteristics within the ballistic transport regime. In this regime, the electrons within the FET can travel without undergoing any scattering mechanism. Figure 1.5 shows the proposed FET and its parameters. This dual-gated (DG) structure was successfully fabricated by Tanaka *et al.* using a silicon-on-insulator (SOI) thin film [39]. Compared to single-gated (SG) SOI MOSFETs, DG structures offer excellent immunity to short-channel effects [39], especially in the subthreshold conduction region, because any current transport paths drawn between the source and drain terminals (including the leakage paths) are closer to one of the gates [40]. In the proposed device structure, the gates are built such that they do not overlap with the drain and source terminals to suppress switching performance penalties owing to parasitic capacitances [41, 42].

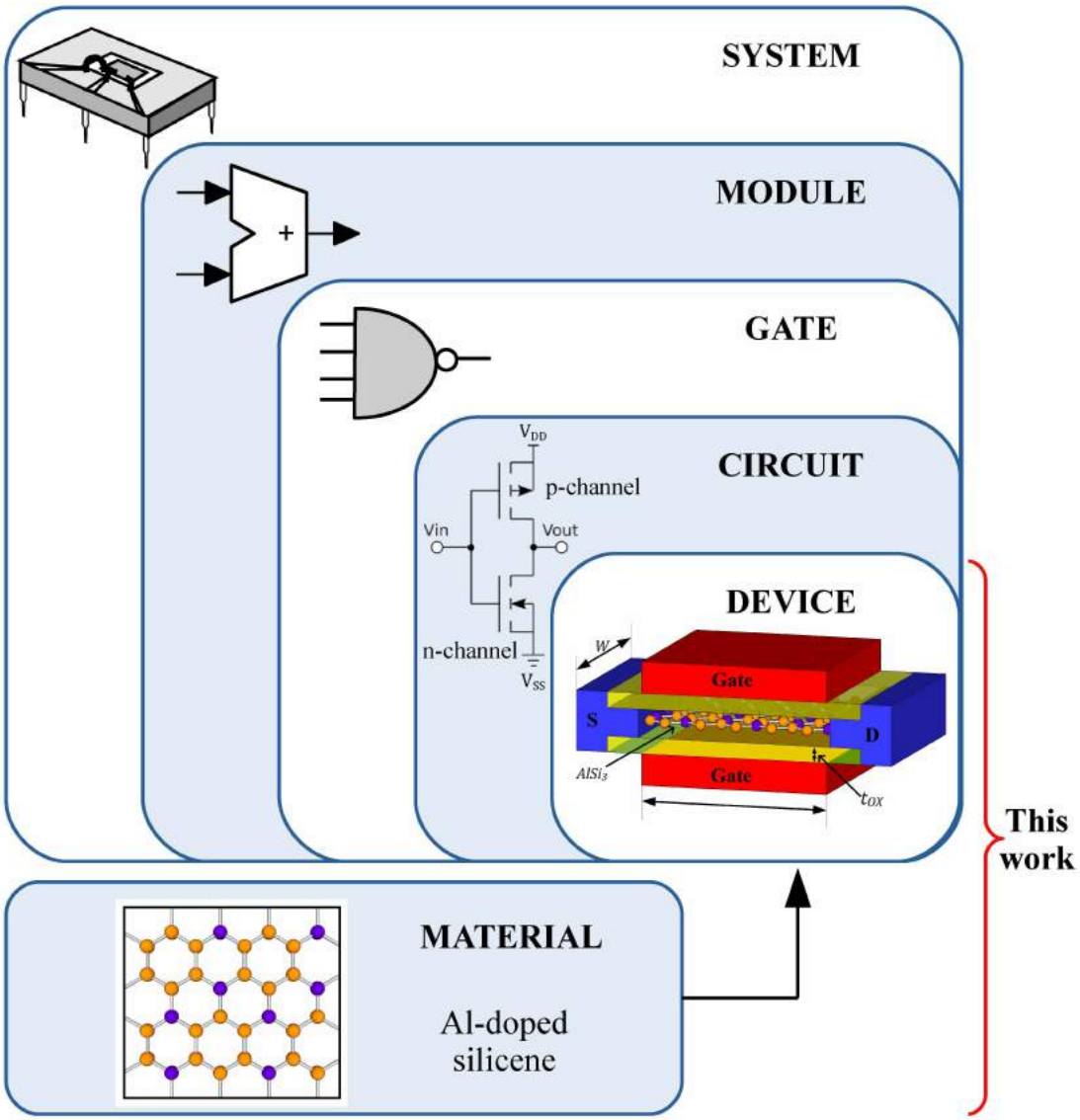


Figure 1.6: Design abstraction levels in modern digital circuits, adopted from [43].

In this study, the current flows in the transistor along the direction parallel to the direction from the drain terminal to the source terminal, with the gates controlling the potential barrier within the semiconductor channel. Three assumptions were made to simplify the modelling and simulation processes: (1) the $AlSi_3$ sheet was assumed to be stable in its planar form (without any buckling parameter); (2) the current in the channel flows in direction parallel to the zigzag edges of the $AlSi_3$ sheet; and (3) ideal metal contacts were used in the $AlSi_3$ FET. The proposed gate length for the FET in this study was $10\,nm$ in order to benchmark the $AlSi_3$ FET model against recently published results in a fair manner.

Subsequently, the I-V characteristics of the proposed $AlSi_3$ FET were benchmarked against published 2D transistor models. By using a graphical extraction method on the simulated I-V characteristics, the performance of the silicene FET was evaluated in terms of device performance metrics extracted from the I-V characteristics, including V_{th}, SS, $DIBL$, and I_{on}/I_{off} ratio. The benchmark of the results was based on results extracted from the closest possible published theoretical models owing to the unavailability of experimental data. Finally, a non-iterative analytical model for the proposed $AlSi_3$ FET was developed to enable cross-platform simulation. In summary, this study focuses on the modelling and simulation at the material and device levels according to the design abstraction levels in modern digital circuits as shown in Figure 1.6.

1.5 Research contributions

The scaling of CMOS technology is the dominant driving force for achieving high-performance computing power. Owing to the fundamental limitations of bulk materials, researchers are actively seeking potential 2D materials for next-generation nanoelectronic devices. Silicene is envisaged as one of the most promising 2D materials that could potentially leverage with the mature Si fabrication technology. In addition to its atomically thin structure, silicene exhibits a very high carrier mobility. Furthermore, these outstanding properties of silicene hold great promise for the "more than Moore" nanoelectronic era. Therefore, the exploration of silicene-based devices are important and creditable to the nanoelectronic research community.

Throughout this study, literature reviews were rigorously conducted to explore the big picture of the theoretical advances in bandgap engineered silicene and silicene-based FETs. These reviews were summarised and discussed systematically to construct the research framework and shape the main motivations of this study. Furthermore, theoretical models must be extended to predict the electronic properties of 2D materials for appropriate selection of dopants [28]. Hence, a model of the material resulting from the promising bandgap engineering technique, namely Al-doped silicene, was derived in this study. This technique was chosen to tune the semi-metallic bandgap of silicene

to a semiconducting bandgap, such that it becomes suitable for transistor applications. Subsequently, the ballistic current transport performance of the proposed device ($AlSi_3$ FET) was simulated using the TOB nanotransistor model and assessed based on its device performance metrics. The results of this study are significant for understanding the essential physics behind silicene-based devices before proceeding to address the practical digital circuit applications.

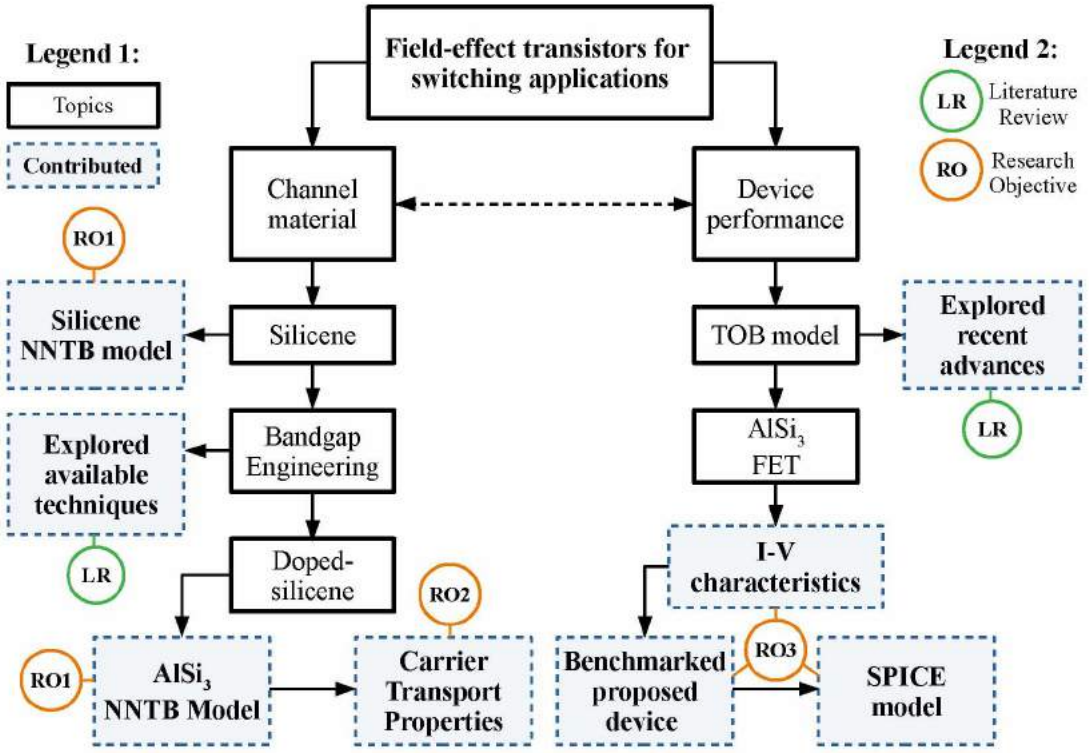


Figure 1.7: Contribution diagram of this thesis. Blue boxes highlight the outputs of this study.

Interestingly, a simulation program with integrated circuit emphasis (SPICE) model can also be created using the results from the proposed TOB nanotransistor model. Compact SPICE models are important in the IC design industry to predict, in mathematical form, the electronic performance of nanoelectronic devices before mass production [40]. Therefore, the results of the present study are useful for further circuit-level modelling and simulation. The main contributions of this study have been published in the form of articles in indexed journals and papers in conference

proceedings (attached in the List of Publications on page 195). Figure 1.7 summarises the research contributions of this thesis.

1.6 Thesis organisation

This thesis is composed of six chapters, where it begins in this chapter, with a brief introduction of the problem background, research objectives, scopes and research contributions. **Chapter 2** reviews the relevant theories, general information of silicene and related previous works which are available in the literature, laying out the overall theoretical dimensions of the research, and looking at how the topic has progressed in the recent years. The particular interest of the literature review is to investigate and understand the theoretical advancement of the bandgap engineering techniques of silicene and silicene-based transistors. As a result, the overview of the topic and research motivation of this work are identified.

Chapter 3 presents the overall research framework and the expected outcome for each phase in this research. The systematic flowcharts in **Chapter 3** act as the guideline throughout the research. Subsequently, **Chapter 4** and **5** describe the details of the models and simulation results at the material (atomic) and device (transistor) levels, respectively. The electronic properties including the bandstructure, bandgap, and density of states for silicene and bandgap engineered silicene are presented at the material level. Using these electronic properties, the research proceeds with the modelling and simulation of transistor at the device level. Then, the SPICE model of the proposed device is also created. After benchmarking and discussing the results of this work, **Chapter 6** concludes the key findings in this research and suggests potential further investigations on this research topic.

LIST OF PUBLICATIONS

Journal with Impact Factor (WOS - CIF: 28.362)

1. **Chuan, M.W.**, Wong, K.L., Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. 2D honeycomb silicon: a review on theoretical advances for silicene field-effect transistors. *Current Nanoscience*, 2020. 16(4): 595-607. doi:10.2174/1573413715666190709120019 **[Q3, IF 2019: 1.836]**

2. **Chuan, M.W.**, Wong, K.L., Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. Two-dimensional modelling of uniformly doped silicene with aluminium and its electronic properties. *Advances in Nano Research*, 2020. 9(2): 105-112. doi:10.12989/anr.2020.9.2.105 **[Q2, IF 2019: 4.583]**

3. **Chuan, M.W.**, Wong, K.L., Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. Electronic properties and carrier transport properties of low dimensional aluminium doped silicene nanostructure. *Physica E: Low-dimensional Systems and Nanostructures*, 2020. 116: 113731. doi:10.1016/j.physe.2019.113731 **[Q2, IF 2018: 3.176]**

4. **Chuan, M.W.**, Wong, K.L., Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. A review of the top of the barrier nanotransistor models for semiconductor materials. *Superlattices and Microstructures*, 2020. 140: 106429. doi:10.1016/j.spmi.2020.106429 **[Q2. IF 2018: 2.385]**

5. **Chuan, M.W.**, Wong, K.L., Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. Device modelling and performance analysis of two-dimensional $AlSi_3$ ballistic nanotransistor. *Advances in Nano Research*, 2021. 10(1): 91-99. doi:10.12989/anr.2021.10.1.091 **[Q2, IF 2019: 4.583]**

6. **Chuan, M.W.**, Lau, J.Y., Wong, K.L., Hamzah, A., Alias, N.E., Lim, C.S., Tan, M.L.P. Low-dimensional modelling of n-type doped silicene and its carrier transport properties. *Advances in Nano Research*, 2021. 10(5): 415-422. doi:10.12989/anr.2021.10.5.415 **[Q2, IF 2019: 4.583]**

7. **Chuan, M.W.**, Wong, K.L., Riyadi, M. A., Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. Semi-analytical modelling and evaluation of uniformly doped silicene nanotransistors for digital logic gates. *PLOS One*, 2021. 16(6): e0253289. doi:10.1371/journal.pone.0253289 **[Q2, IF 2019: 2.74]**

8. **Chuan, M.W.**, Riyadi, M. A., Hamzah, A., Rusli, M.S., Alias, N.E., Mohamed Sultan, S., Lim, C.S., Tan, M.L.P. Impact of phonon scattering mechanisms on the performance of silicene nanoribbon field-effect transistors. *Results in Physics*, 2021. 29: 104714. doi:10.1016/j.rinp.2021.104714 **[Q1, IF 2019: 4.476]**

Indexed Journal

1. **Chuan, M.W.**, Wong, K.L., Hamzah, A., Alias, N.E., Lim, C.S., Tan, M.L.P. Electronic properties of zigzag silicene nanoribbons with single vacancy defect. *Indonesian Journal of Electrical Engineering and Computer Science*, 2020. 19(1): 77-84. doi:10.11591/ijeecs.v19.i1.pp76-84 **[Indexed by SCOPUS]**

Indexed conference proceedings

1. **Chuan, M.W.**, Wong, K.L., Riyadi, M. A., Alias, N.E., Tan, M.L.P. Electronic properties of silicene nanoribbon using tight-binding approach. *International Symposium on Electronics and Smart Devices (ISESD) 2019*, 2019: 8909598. doi:10.1109/ISESD.2019.8909598 **[Indexed by WOS]**

2. **Chuan, M.W.**, Wong, K.L., Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. Device performance of silicene nanoribbon field-effect transistor under ballistic transport. *2020 IEEE International Conference on Semiconductor Electronics (ICSE)*, 2020: 9166895. doi:10.1109/ICSE49846.2020.9166895 **[Indexed by SCOPUS]**

Other publications

1. Wong, K.L., **Chuan, M.W.**, Hamzah, A., Rusli, M.S., Alias, N.E., Mohamed Sultan, S., Lim, C.S., Tan, M.L.P. Electronic properties of graphene nanoribbons with line-edge roughness doped with nitrogen and boron. *Physica E: Low-dimensional Systems and Nanostructures*, 2020. 117: 113841. doi:10.1016/j.physe.2019.113841 **[Q2, IF 2018: 3.176]**

2. Leong, C. H., **Chuan, M.W.**, Wong, K.L., Najam, F., Yu, Y. S., Tan, M.L.P. Compact device modelling of interface trap charges with quantum capacitance in MoS_2-based field-effect transistors. *Semiconductor Science and Technology*, 2020. 35(4): 045023. doi:10.1088/1361-6641/ab74f2 **[Q2, IF 2018: 2.654]**

3. Wong, K.L., **Chuan, M.W.**, Hamzah, A., Rusli, M.S., Alias, N.E., Lim, C.S., Tan, M.L.P. Carrier statistics of highly doped armchair graphene nanoribbons with edge disorder. *Superlattices and Microstructures*, 2020. 139: 106404. doi:10.1016/j.spmi.2020.106404 **[Q2, IF 2018: 2.385]**

4. Wong, K.L., **Chuan, M.W.**, Hamzah, A., Rusli, M.S., Alias, N.E., Mohamed Sultan, S., Lim, C.S., Tan, M.L.P. Carrier transport of rough-edged doped GNRFETs with metal contacts at various channel widths. *Superlattices and Microstructures*, 2020. 143: 106548. doi:10.1016/j.spmi.2020.106548 **[Q3, IF 2019: 2.120]**

5. Wong, K.L., **Chuan, M.W.**, Hamzah, A., Rusli, M.S., Alias, N.E., Mohamed Sultan, S., Lim, C.S., Tan, M.L.P. Performance metrics of current transport in pristine graphene nanoribbon field-effect transistors using recursive non-equilibrium Green's function approach. *Superlattices and Microstructures*, 2020. 145: 106624. doi:10.1016/j.spmi.2020.106624 **[Q3, IF 2019: 2.120]**

6. Wong, K.L., **Chuan, M.W.**, Chong, W.K., Alias, N.E., Hamzah, A., Lim, C.S., Tan, M.L.P. Carrier statistics of highly doped armchair graphene nanoribbons with edge disorder. *Advances in Nano Research*, 2019. 7(3): 209-221. doi:10.12989/anr.2019.7.3.209 **[Q2, IF 2018: 2.333]**

7. Wong, K.L., Tan, B.R., **Chuan, M.W.**, Hamzah, A., Rusli, M.S., Alias, N.E., Mohamed Sultan, S., Lim, C.S., Tan, M.L.P. Modeling of lightly-doped drain and source contact with boron and nitrogen in graphene Nanoribbon. *Chinese Journal of Physics*, 2019, 62: 258-273, doi:10.1016/j.cjph.2019.09.026 **[Q2, IF 2018: 2.544]**