THERMAL-SAFE SYSTEM-ON-CHIP TEST SCHEDULING USING DYNAMIC VOLTAGE AND FREQUENCY SCALING

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DEDICATION

To my lovely parents, *who gave me endless love, trust, constant encouragement over the years, and for their prayers.*

To my precious husband and kids, *for their patience, support, love, and for enduring the ups and downs during the completion of this thesis.*

This thesis is dedicated to them.

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ABSTRACT

Designing integrated circuits (ICs) has become more challenging when fabrication technology scales down. Overheating has been acknowledged as a major issue in testing due to high power consumption of a chip during test. A direct consequence of the increasing power density is the increasing junction temperature that poses several problems such as aging issue. Therefore, thermal estimation needs to be considered during test scheduling to avoid exceeding temperature limit of the System-on-Chips under test. This thesis proposes a new thermal model that considers metal layer effects of SoC, and thermal safe test scheduling with dynamic voltage and frequency scaling (DVFS) technique. The difference in estimated temperature is over 10 °C if the effect of metal interconnect is neglected. In DVFS, the energy savings obtained by eliminating the global clock are, in many cases, offset by the additional power consumed due to longer execution time. The thermal safe test scheduling problem is formulated as a combination optimization problem, and the integer logic programming is used to find the optimal solution of test schedule for a given SoC under thermal constraint. The proposed thermal model is a necessary tool for rapid thermal analysis of the system which is exposed to non-uniform substrate temperature including thermal effect from metal interconnects. This thermal model will be used to estimate temperature during test scheduling in order to optimize total test time under thermal constraint. Results on different benchmark SoCs have shown the effectiveness of the proposed technique which produces shorter testing time. Total test time reduction by using the proposed technique is 46% compared to conventional existing techniques. Overall, the proposed technique produced more effective thermal aware test scheduling.

ABSTRAK

Mereka bentuk litar bersepadu (IC) telah menjadi lebih mencabar apabila teknologi fabrikasi berskala rendah. Pemanasan lebih telah diakui sebagai isu utama dalam pengujian kerana penggunaan kuasa yang tinggi semasa cip melalui pengujian. Akibat langsung daripada ketumpatan kuasa yang semakin meningkat seterusnya meningkatkan suhu simpang akan menimbulkan beberapa masalah seperti isu penuaan. Oleh itu, anggaran terma perlu diambilkira semasa penjadualan ujian untuk mengelakkan dari melebihi had suhu daripada sistem-atas-cip (SoC) yang diuji. Tesis ini mencadangkan satu model terma baharu yang mempertimbangkan kesan-kesan lapisan logam di dalam SoC, dan ujian penjadualan terma-selamat dengan menggunakan teknik penskalaan voltan dan frekuensi dinamik (DVFS). Perbezaan suhu anggaran mencecah 10 °C jika lapisan logam saling hubung diabaikan. Masalah penjadualan ujian terma-selamat ini dirumuskan sebagai masalah pengoptimuman gabungan, dan pengaturcaraan logik dengan kekangan digunakan untuk mencari penyelesaian jadual ujian yang memberikan jumlah masa yang optimum bagi SoC dengan diberikan kekangan terma ke atasnya. Model terma yang dicadangkan diperlukan untuk analisis terma aras sistem yang pantas, yang mana pendedahan kepada suhu substrat yang tidak sekata adalah salah satu kesan daripada lapisan logam saling hubung. Model terma ini akan digunakan untuk menganggarkan suhu semasa penjadualan untuk mengoptimumkan jumlah masa ujian di bawah kekangan terma. Keputusan ke atas litar tanda aras SoC yang berbeza menunjukan teknik yang dicadangkan memberikan masa ujian yang lebih pendek. Jumlah masa pengujian dapat dikurangkan sehingga 46% berbanding dengan kaedah konvensional yang sedia ada. Pada keseluruhannya, teknik yang dicadangkan ini memberikan kesan yang lebih efektif dalam penjadualan ujian sedar terma.

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LIST OF ABBREVIATIONS

ATE	-	Automated test equipment
BIST	-	Built in Self-test
CAE	-	Computer-aided engineering
CFD	-	Computational Fluidic Dynamic
CMOS	-	Complementary metal-oxide semiconductor
CPU	-	Computer Processing Unit
CUT	-	Circuit under Test
DFT	-	Design for Test
DVFS	-	Dynamic Voltage and Frequency Scaling
GA	-	Genetic Algorithm
IC	-	Integrated Circuit
ILP	-	Integer Linear Programming
IP	-	Intellectual property
ITRS	-	International Roadmap Semiconductor
LFSR	-	Linear Feedback shift register
MG	-	Multi-Grid
PDE	-	Partial Differential Equation
RC	-	Resistor-Capacitor
RTL	-	Register Transfer Level
ROFs	-	Resistive Open Faults
SCO	-	Scheduling Consideration Order
SoB	-	System-on-Board
SoC	-	System-on-Chip
TAM	-	Test Access Time
TAP	-	Test Access Port
TAT	-	test access time
TCC	-	Test Compatibility Clique
TCG	-	Test Compatibility Graph
TCS	-	Test Compatibility subset
TTSV	-	Through-Silicon Vias
VLSI	-	Very Large Scale Integration
WBR	-	Wrapper boundary register
WIR	-	Wrapper Instruction Register
WPI	-	Wrapper Pin In
WPO	-	Wrapper Pin Out

CHAPTER 1

INTRODUCTION

This chapter describes the background and the importance of temperature aware testing methodology. This is followed by research objectives, scope, and contribution. After that, research methodology and thesis organization are also described is this chapter.

1.1 Overview

Knowing temperature during testing is very essential because some temperature –dependent defects become more easily tested when tests are applied [1] at specified temperature or within a given temperature range. To alleviate issues of long test time, test access mechanism and test wrapper for System-on-Chip (SoC) a core-based have been introduced to enable parallel testing of multiple cores [2]. However, the trade-off is the increasing power consumption that leads to crosstalk, voltage drop (also known as IR drop) and reliability issues. Besides, increasing power density, which is the amount of power per unit area also implies higher temperature and heat dissipation. This is because the heat generated continuously which directly increases the temperature on the SoC. The increases in power consumption due to process scaling, combined with high switching and poor cooling environment during testing have the potential to result in high temperature. The core-based designs are usually tested after assembly. A major challenge in testing SoC is test scheduling that determines the orders in which various cores are tested. Therefore, if the test scheduling is provided with temperature awareness, parallel testing of multiple cores will not encounter overheating issues.

1.2 Background

Advances in VLSI technology have allowed billions of transistors to be integrated into a single chip. This has led to the advent of System-on-Chip (SoC) design, which implements all major system components on a single chip to achieve both lower fabrication cost and higher speed performance. However, the increased complexity in such large and high performance systems has posed challenges to design, production and test. When the shrinking feature size of transistor enables implementation of SoC on nanometer regime, testing cost becomes more expensive because test time that involves multiple cores in the system is critical for time-to-market. In fact, testing cost is approximately 50% of manufacturing cost as reported in [3].

Power consumption and thermal issues are major concerns in design and fabrication of VLSI circuits. The increasing number of transistors in SoC and the operation frequency in SoC will directly exacerbate these issues. Furthermore, testing SoC results in excessive power consumption compared to normal mode because testing typically involves large number of switching activities [1]. Power consumption in SoC is converted directly into dissipated heat and this increases the temperature in SoC [4]. This is because a high temperature leads to reduced performance of devices with decreasing carrier mobility and increasing interconnect resistivity [1]. This leads to degradation of reliability because high temperature during testing exacerbates aging effects on the system. In the worst case, it could damage cores in the SoC. The impact of temperature on power consumption is firstly reflected by that leakage power increases rapidly with the increase of temperature [4]. As leakage power grows significantly in relation to dynamic power with the deep submicron technology, due to the reduction of threshold voltage, channel length, and gate oxide thickness, the total power consumption of a circuit grows rapidly also with the increase of temperature, which in turn will further increase the temperature [5]. This positive feedback may even lead to thermal runaway and burn the chip. Therefore, it is important to reduce the temperature of a chip in order to decrease the leakage power. As a result, several recent papers have addressed the problem of test scheduling in such a way that

resource, power, and thermal constraints are satisfied. The details for the problem addressed by previous researcher on test scheduling are discussed in Chapter 2.

Heat transfer during test session and normal mode can be transferred away from the core through its lateral neighbourhood and vertically to the heat sink. There is a real need to formulate and address power problems and temperature problems early in the design flow such as in Register Transfer Level (RTL) stage to speed up time-to-market, which indirectly contributes to reducing the design productivity gap. Referring to International Roadmap Semiconductor published in 2015 (ITRS'15) [6], even though the transistor count has kept on increasing and transistors are able to operate with each new technology generation at higher frequency than before, it has become practically impossible to keep on conjunctly increasing both of these factors due to physical limitations on power consumption that has to level off in order to make the integrated circuits (ICs) capable to operate under practical thermal conditions. Thermal effect may represent a limiting factor in the development of integrated circuit because hotspot may degrade circuit performance and reliability, and increase leakage power. Therefore, nowadays, thermal management module is included to regulate the temperature in the SoC during operation mode. In designing an efficient thermal management module, thermal simulation is necessary to perform thermal analysis. Besides regulating temperature for normal operation, temperature regulation during testing is equally important to avoid cores undergoing high temperature. When test scheduling is planned, some cores in the SoC could be firm cores or soft cores whereby accurate temperature is not yet known. For these cores, RTL thermal model which is temperature estimation model at early stage of design can be used to estimate their temperature. The existing thermal models, [4], [7]–[9] consider thermal effect of substrate and package only. However, the metal interconnect should be considered as well for causing heat transfer from core to core and heat transfer between metal and substrate due to temperature differences among these cores.

1.3 Problem Statement

Testing a core-based SoC with several modules integrated together is challenging. With test access time (TAM) and test wrapper, test scheduling is performed such that test patterns for each core are ordered to reduce the test time. However, the increased complexity of SoC results in huge test patterns. Similarly, increase of the patterns indicates higher power consumption in SoC. Even assuming tester memory size will be doubled every three years and more advanced test data compression techniques have been employed, test data reduction will remain a serious issue that must be tackled to control power consumption [2]. Test scheduling is typically carried out under power constraints since multiple cores are tested in parallel. This is because power-aware test scheduling has been introduced to overcome overheating of SoC during testing but soon it was reported in [10] that power-aware test scheduling cannot resolve hotspot issue in SoC. Instead, power density should be considered because it subsequently forms hotspots and increases the temperature in the system. This is because power density continuously causes heat dissipation among the cores in the SoC; thus, it increases the temperature on the cores and leads to thermal problem. Moreover, delay increases approximately 5% for every 10° C increase of temperature and the leakage current increases exponentially with temperature increase [11]. Therefore, thermal aware test scheduling is needed to cover hotspot issues in SoC especially during testing due to more power dissipation.

To deliver test time minimization for core-based SoC that considers temperature of each core to avoid hotspots, first, an efficient yet accurate thermal simulator needs to be developed to simulate temperature for each core in SoC when test patterns are pumped into the SoC. Information of temperature generated by the simulator is important to produce test schedule that has safe thermal ranges. Most of the recent thermal-aware test scheduling provides detailed temperature distribution, which is a resource and time-consuming task. However, thermal simulation can be performed at higher level such as architecture level or RTL. Therefore, it allows earlier detection of hotspot in SoC. Compact thermal modelling is one of the methods used to simulate temperature at architectural level using Resistance-Capacitance (RC) thermal model.

The temperature for any particular core does not only depend on its own power density, but also on the power densities of the adjacent cores. At first glance, it may seem that heat is mainly redistributed in the substrate layer and the contribution of interconnect is marginal [12]. The initial perception fails to take into account interconnect effects on temperature in the system. Since the cross sectional area of interconnect is generally smaller than that of the substrate, it may raise a concern that the resultant higher current density in interconnect may generate significant heat because the density of interconnect in the core increases with the number of transistors. Since VLSI circuits continue to be scaled aggressively, rapid increase in functional density has resulted in a steady increase in chip size. This has resulted in an increasing number of interconnect levels in order to realize all the inter-device and inter-block communications. The number of interconnect metal levels are increased from six levels at the 180 nm node to nine levels at the 45 nm node [13]. Furthermore, thermal conductivities of interconnect is higher than substrate. So, it is envisioned that thermal effects in interconnect can potentially become another serious design constraint. Therefore, this is the research gap on the thermal modelling.

Hotspots in metal layers are exacerbated by increasing current density and self-heating power consumptions on interconnect. Hot interconnect is becoming a serious problem when metal interconnect defects pass a speed test at nominal temperature, but fail at a higher temperature for the same test. This means that delay tests, such as maximum frequency test and transition delay test, should be applied at a higher temperature level in order to detect these temperature-dependent defects [5]. Therefore, metal layer must be modelled in thermal modelling in order to avoid under-estimation of the temperature. Continued scaling and the introduction of low dielectric in the back-end process technology on metal interconnect also affect hot interconnect. This is true because the rate of interconnect electro-migration is dependent on temperature exponentially [14]. According to [15], the interconnect temperature will be approaching 400-900 K at 22 nm technology node if the thermal challenge on interconnect is not properly dealt with along the road. Thus, thermal simulation that considers metal interconnect effect at architectural level could be a better solution to estimate temperature of each core in SoC test scheduling. This can be achieved by scheduling the tests with the aid of thermal simulation as heat is evenly distributed over the chip to reduce hotspots.

Temperature is a concern during testing due to the potential increased power consumption resulting from high switching activity. High temperature leads to performance degradation, which is due to reduced carrier mobility and driving current as well as increased interconnect delay. A recent study has shown that the maximal clock frequency has to be reduced by 23% when the temperature of a circuit is raised from 50° C to 110° C, when the circuit is operated at 1.1 V [5]. This clock frequency and temperature dependency should be carefully analyzed when developing frequency scaling technique to control temperature during testing in terms of timing. One method to reduce the power dissipation in CMOS circuits is to reduce the supply voltage, *Vdd*. However reducing *Vdd* has an inverse relation with gate delay where the gate delay increases as the voltage is reduced. In order to reduce the test time, the clock frequency must be increased. However, operating at higher frequency will drag the SoC into high power dissipations, leading to thermal issue. So, dependency between voltage, frequency and temperature requires a study when considering voltage and frequency scaling technique to overcome thermal issues during testing.

1.4 Research Objectives

The goal of this thesis is to develop an efficient thermally safe test scheduling algorithm with dynamic voltage frequency scaling (DVFS) for core based SoC. To accomplish the goal, two objectives are devised as follows:

Objective 1: To develop a new thermal model for SoC with consideration of interconnects effect.

To develop a thermal model of SoC with capability for calculating heat transfer among the cores and interconnect effect to the SoC within reasonable computation time, the simplified model was designed to represent the thermal behaviour of the chip to perform a quick thermal analysis with the improved accuracy in system design process. To accomplish this objective, the thermal model, in general, must estimate system temperatures, heat loads, and powers involved in the system.

Objective 2: To develop thermal safe test scheduling platform for SoC testing with DVFS.

The main objective of this research is to develop a test planning platform/framework in the aim to minimize total testing time under thermal constraints. This research will apply DVFS algorithm to solve the test scheduling problem. This algorithm considers DVFS technique under constraint of temperature limit in order to minimize the test time.

1.5 Scope of Study

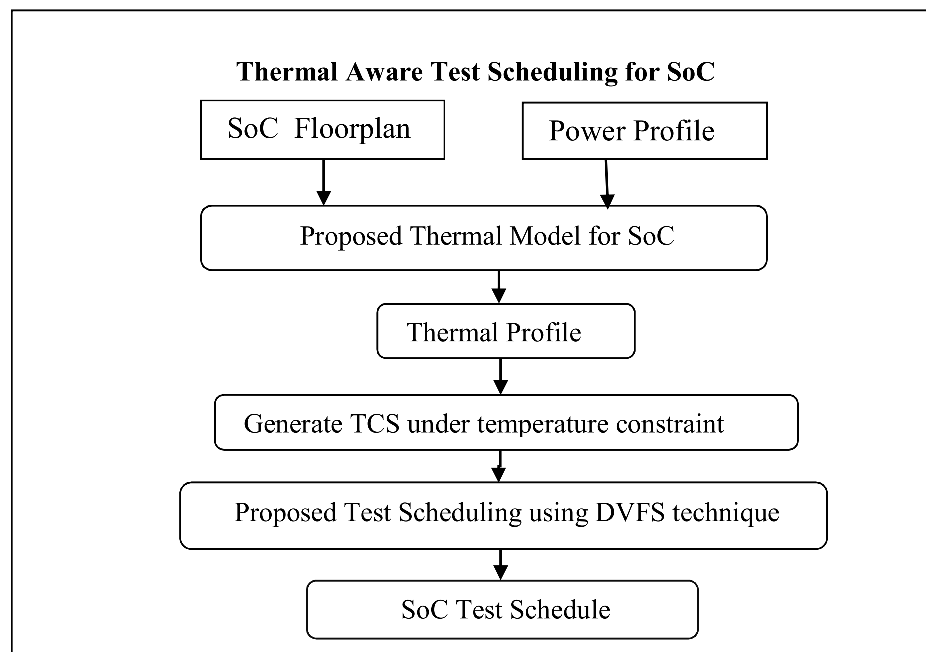

Figure 1.1 Scope of study of thermal aware test scheduling

In order to achieve the objective of the research, the following research scope has been outlined. The proposed thermal aware test scheduling platform consists of two stages as illustrated in Figure 1.1.For this thesis, SoC benchmark circuits are used to prove the effectiveness of the proposed methods. The first stage consists of the proposed thermal model at architectural level. The model requires reading SoC floorplan and power profile to estimate the temperature. SoC floorplan is provided by

the SoC benchmark and it was generated by the chip estimator tool [16]. Power profile consists of average power for each core in the SoC and is also provided by Millican and Salaju in [17]. Assumption for metal area is 50% of the die area [18]. Based on all these information, the cycle-accurate temperature for each core in SoC will be generated using the proposed thermal model.

For the second stage, the proposed SoC test scheduling consists of two major steps. First, test sessions are derived based on test compatibility graph (TCG). Second, test scheduling algorithm is developed to schedule the test sessions under the given temperature constraints with DVFS technique such that total test time is minimized. All the test sessions are dedicated with particular voltage and frequency specifications resulted from DVFS.

1.6 Organization of Thesis

The thesis is organized into seven chapters. Chapter 1 discusses the introduction, research problems, research scope and research objectives related to the development of thermal aware test scheduling on SoC using DVFS technique. In this chapter, we address the research problems and several research gaps which provide a motivation in our research. This research is intended to fill the research gap on thermal model and test scheduling algorithm's performance in terms of test time and temperature modelling.

Chapter 2 provides literature review prior to engaging the mentioned scope of work. Several topics related to this research are reviewed to give an overall picture of the background knowledge involved. Summary of the literature review is given to clarify the research rationale. The literature review covers the previous significant researches for thermal model and test scheduling techniques

Chapter 3 discusses research process on developing the proposed thermal model with metal interconnect and test scheduling technique with thermal constraint using DVFS technique which are the two main core algorithms in this thesis. The first

part covers the proposed thermal model technique that has been implemented in test scheduling. This proposed algorithm is adopted in test scheduling as thermal simulator. The second part discusses the methodology of our proposed test scheduling technique using DVFS with temperature constraint.

Chapters 4 presents thermal model with metal interconnect effect by enhancing the well known thermal model HotSpot. Moreover, this thermal model allows both steady-state simulation and transient simulation. MATLAB programming is used to develop the thermal model.

Chapter 5 presents proposed DVFS technique to be employed on the test scheduling. It starts with the explanation on ideas of DVFS and demonstrates how DVFS performed frequency scaling up and frequency scaling down. This chapter also demonstrates the flow chart of the test scheduling algorithm. This test scheduling implements DVFS technique and estimate the temperature by thermal model with metal interconnects effect considerations.

Chapter 6 presents the experimental result and analysis of thermal aware test scheduling using DVFS technique. Besides, to validate the accuracy of proposed thermal model, comparison between established thermal model (HotSpot) and finite element software (ANYS) are presented. The effectiveness of the proposed test scheduling that is equipped with DVFS technique is also demonstrated. Finally, the performance comparisons in terms of test time and temperature on SoCs have been done between the proposed technique and other established methods.

In the final chapter of the thesis, the research work is summarized and deliverables of the research are stated. Suggestions for potential extensions and improvements to the research topic are also given.

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APPENDIX A

Overview