DISTANCE-AWARE BIDIRECTIONAL MEDIUM ACCESS CONTROL FOR MESH WIRELESS NETWORK-ON-CHIP ARCHITECTURE

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ABSTRACT

Wireless Network-on-Chip (WiNoC) architectures have recently been proposed to address the scalability limitations of conventional multi-hop wired NoC architectures. The medium access control (MAC) protocol and routing strategy are critical in determining the performance and energy characteristics of a WiNoC. Most conventional WiNoC MAC use a daisy-chained ring topology, which limits the performance benefit of using a wireless channel since daisy-chaining results in a maximum waiting time when a radio hub misses the token before a packet arrives. Furthermore, even when radio hubs are connected to wired paths, all cores connected to the WiNoC radio hub prioritise transmission through the radio hub, resulting in an uncontrolled load on the wireless channel. Therefore, this thesis's main objectives are as follows. The first objective is to propose a Bidirectional MAC (BMAC) strategy for WiNoC while the second objective is to propose a Distance-Aware (DA) routing scheme in conjunction with BMAC (DA+BMAC) to control a single-hop wireless transmission exclusive to far away destination cores. The wired metal planar interconnect has a higher aggregate bandwidth and is dedicated to short-range communication, whereas single-hop wireless channels are dedicated to long-range transmission beyond a certain distance threshold. To determine the effectiveness of the proposed works, a comprehensive validation was performed using the cycle-accurate Noxim simulator. The proposed strategy was tested and validated in terms of latency, throughput, and energy consumption using synthetic traffic distributions (random, shuffle, transpose, and hotspot) and real-application PARSEC (Barnes) and SPLASH-2 (Fluidanimate) traces. Extensive simulation results show that BMAC can achieve up to 1.84 times faster throughput, while DA+BMAC can improve up to 11.49 times faster than the WiNoC baseline daisy-chained architecture. At the same time, the energy improvement over the baseline daisy-chained at the saturated packet injection load is up to 8% for BMAC and 15% for DA+BMAC. The proposed MAC and routing protocols increase wireless channel utilisation and balance wireless-wired load, resulting in significantly improved WiNoC performance over the baseline architecture.

ABSTRAK

Seni bina Rangkaian-atas-cip wayarles (WiNoC) baru-baru ini telah dicadangkan untuk menangani had kebolehskalaan seni bina NoC berwayar berbilang-hop konvensional. Protokol dan strategi penghalaan kawalan capaian media (MAC) adalah penting dalam menentukan prestasi dan ciri tenaga WiNoC. Kebanyakan MAC WiNoC konvensional menggunakan topologi gelang rantai-daisy, yang mengehadkan faedah prestasi menggunakan saluran wayarles memandangkan rantaian-daisy menghasilkan masa menunggu maksimum apabila hab radio terlepas token sebelum paket tiba. Tambahan pula, walaupun hab radio disambungkan ke laluan berwayar, semua teras yang disambungkan ke hab radio WiNoC mengutamakan penghantaran melalui hab radio, mengakibatkan beban tidak terkawal pada saluran wayarles. Oleh itu, objektif utama tesis ini adalah seperti berikut. Objektif pertama adalah untuk mencadangkan strategi MAC Dwiarah (BMAC) untuk WiNoC manakala objektif kedua adalah untuk mencadangkan skim penghalaan sedar-jarak (DA) bersama-sama dengan BMAC (DA+BMAC) untuk mengawal penghantaran wayarles hop tunggal eksklusif untuk teras destinasi yang jauh. Sambungan satah logam berwayar mempunyai lebar jalur agregat yang lebih tinggi yang dikhususkan untuk komunikasi jarak dekat, manakala saluran wayarles hop tunggal dikhususkan untuk penghantaran jarak jauh melebihi ambang jarak tertentu. Untuk menentukan keberkesanan kerja yang dicadangkan, pengesahan komprehensif telah dilakukan menggunakan penyelaku Noxim tepat kitaran. Strategi yang dicadangkan telah diuji dan disahkan dari segi kependaman, daya pemprosesan dan penggunaan tenaga menggunakan taburan trafik sintetik (rawak, kocok, transposisi, dan kawasan panas) dan surih aplikasi sebenar PARSEC (Barnes) dan SPLASH-2 (Fluidanimate). Hasil simulasi yang meluas menunjukkan bahawa BMAC boleh mencapai daya pemprosesan sehingga 1.84 kali lebih pantas, manakala DA+BMAC boleh meningkat sehingga 11.49 kali lebih pantas daripada rangkaian-daisy garis dasar seni bina WiNoC. Pada masa yang sama, peningkatan tenaga ke atas rantaian-daisy garis dasar pada beban suntikan paket tepu adalah sehingga 8% untuk BMAC dan 15% untuk DA+BMAC. MAC dan protokol penghalaan yang dicadangkan meningkatkan penggunaan saluran wayarles dan mengimbangi beban berwayar-wayarles, menghasilkan prestasi WiNoC yang lebih baik berbanding seni bina garis dasar dengan ketara.

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LIST OF ABBREVIATIONS

2D	–	Two Dimension
3D	–	Three Dimension
A-WiNoC	–	Adaptive Wireless NoC
aCDMA	–	Adaptive Code-Division Multiple Access
ADC	–	Analog to Digital Converter
ALASH	–	Adaptive Layered Shortest Path
ASK	–	Amplitude Shift Keying
BPSK	–	Binary Phase Shift Keying
BMAC	–	Bidirectional Medium Access Control
BRS	–	Broadcast Reliability Sensing
CDMA	–	Code-Division Multiple Access
CJA	–	Congestion Judgement Algorithm
CMOS	–	Complementary Metal-Oxide Semiconductor
CMP	–	Chip Multi Processor
CNT	–	Carbon Nano Tube
CPCA	–	Cross-Path Congestion-Aware
CSMA	–	Carrier-Sense Multiple Access
D-SAM	–	Demanded Slot Allocation Mechanism
DA	–	Distance-Aware
DA+BMAC	–	Distance-Aware Bidirectional MAC
Delta MIN	–	Delta Multistage Interconnection Network
FDMA	–	Frequency Division Multiple Access
FIT	–	Floyd-based Inter-chip Traffic

GWNoC	–	Graphene-based Wireless NoC
HDL	–	Hardware Description Language
HiWA	–	Hierarchical Wireless-Based Architecture
HoneyWiN	–	Honeycomb-based Wireless NoC
IC	–	Integrated Circuit
I/O	–	Input/Output
IP	–	Intellectual Property
iWISE	–	Inter-router Wireless Scalable Express Channels
LNA	–	Low Noise Amplifier
LTCA	–	Load-balanced Time-based Congestion Aware
MAC	–	Medium Access Control
MALASH	–	Multicast Adaptive Layered Shortest Path
MROOTS	–	Multiple Tree Roots
McWiNoC	–	Multi-Channel WiNoC
MinBD	–	Minimally Buffered Deflection Routing
MoT	–	Mesh of Tree
mSWNoC	–	Millimeter-wave Small-world Wireless NoC
MWCNT	–	Multi-walled Carbon Nanotube
NACK	–	Negative Acknowledgement
NI	–	Network Interface
NePA	–	Network-Based Processor Array
NoC	–	Network-on-Chip
OOK	–	On-Off Keying
OOP	–	Object-oriented Programming
PA	–	Power Amplifier
PARSEC	–	Princeton Application Repository for Shared Memory Computer

PDF	–	Probability Density Function
PE	–	Processing Element
PIR	–	Packet Injection Rate
RF	–	Radio Frequency
RMS	–	Recognition, Mining and Synthesis
RTL	–	Register Transfer Level
SoC	–	System-on-Chip
SPH	–	Smoothed Particle Hydrodynamics
SPLASH-2	–	Standford ParalleL Applications for SHared memory 2
STL	–	Standard Template Library
TDMA	–	Time-Division Multiple Access
TLM	–	Transcation Level Model
UWB	–	Ultra Wideband
WiNoC	–	Wireless Network-on-Chip
YAML	–	YAML Ain't Markup Language

LIST OF SYMBOLS

mm	–	millimeter
nm	–	nanometer
Gb/s	–	giga bit per second
GHz	–	giga hertz
pJ	–	pico joule
THz	–	terahertz

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CHAPTER 1

INTRODUCTION

1.1 Introduction

In the era of Chip Multi Processor (CMP), modern processors contain an ever increasing number of integrated cores, and network-on-chip (NoC) architectures have gained a strong establishment as a solution for future on-chip interconnect networks [1–9]. NoC adapts the application of networking theory, which is based on packet-switching and consists of a number of routers interconnected with point-to-point links that are arranged to form a specific topology. Currently, NoC is the preferred choice for chip multiprocessors interconnected networks because it not only provides substantial enhancements to on-chip interconnect scalability, but also in fault tolerance and modularity with appropriate design of the routing protocol or the flow control mechanism [10–15].

In general, the scaling of parallel applications increases the communication-to-computation ratio when the computation is distributed over a large number of cores [16]. The increase in core density implies a broader selection of possible destinations, making the traffic more dynamic with a higher amount of communication and a higher degree of traffic heterogeneity [7, 17]. As the number of cores grows, the performance benefit of the conventional NoC is restricted by the high latency together with high power dissipation due to long-distance multi-hop communication. Moreover, among the critical challenges of the growing number of processing cores is the average packet traversal, which affects the time and energy required for data movement across the chip die. This calls for an innovative alternative architecture that can offer the shorter distance between large processing cores.

Nonetheless, as integration levels continue to rise, these NoC interconnects face serious scalability constraints, inspiring researches into new emerging interconnect

technologies such as optical NoC (oNoC) [18–22], three-dimensional (3D) NoC [23–28], RF-interconnection (RF-I) [29–32], and Wireless NoC (WiNoC) [33–37]. Each of these on-chip interconnect alternatives has its own unique features as well as their advantages and disadvantages [34, 38, 39]. Among others, WiNoC communication has garnered interest in recent research due to its several interesting capabilities [33–37]. First, this interconnect is Complementary Metal-Oxide Semiconductor (CMOS) compatible [40] and can be employed for transmission of data across the chip via a one-hop wireless link with low energy while providing high bandwidth with low latency at low energy. Furthermore, because wireless transmission does not require a wireline metal wire or a waveguide, the WiNoC platform provides architectural flexibility, reducing area overhead and chip design complexity.

WiNoC is the NoC architecture that hybridises wired and wireless interconnects to alleviate the long latency of wired planar communication through an express long-range wireless channel [34, 36, 40–46]. Advances in integrated transceivers [47, 48] and millimetre-wave antennas [49, 50] have motivated the development of WiNoC as a possible complement to conventional NoC [51]. A set of processing cores are integrated with antennas and transceivers that are able to modulate and transmit data packets for wireless on-chip transmission. With WiNoC, the long-distant cores can communicate with one-hop low latency. In addition, beyond a certain source-to-destination distance, the performance enhancement using the WiNoC wireless channel is greater because the wireless channel consumes less energy as compared with the multi-hop traditional metal wires [52–56].

1.2 Problem Statement

The design of low area overhead and efficient MAC protocol are regarded as some of the important challenges for WiNoC technology [34, 57, 58]. In WiNoC, most existing MAC approaches is the daisy-chained based ring topology, which uses token passing procedure as an access mechanism to wireless medium due to its simplicity and collision-free protocol [34, 46, 59–62]. In the token-passing method, the radio hub that holds the token is permitted to exclusively utilize the channel for present wireless transmission. After that, the token is handed off to the following radio hub nodes in an

ordered sequence according to the logical ring manner. However, the shortcoming of this approach is the wireless link access delay caused by token circulation among radio hub nodes. The token-passing based MAC protocol grants the radio hub that has the token for exclusively access to the wireless data transmission channel. This restricts the performance advantages of adopting the wireless channel for the WiNoC architecture since the flow of token is in a unidirectional manner that is based on circular token passing for granting the particular radio hub for using wireless communication. As a consequence, this can cause low network utilization for the WiNoC architecture due to its restricted wireless channel access. Regardless of the scalability concern, this token round-trip persists as the cost of additional latency. This is because when the scale of the daisy-chained ring becomes bigger, it directly implies a longer MAC delay and token waiting time for circulating the token holder among radio hubs. Nevertheless, the MAC delay is one of the dominant factors in the overall delay in WiNoC [57, 63–65]. Therefore, reducing the MAC delay for WiNoC is important to sustain the latency advantage of the one-hop wireless approach.

Because no wired path infrastructure is needed between processing cores, the flexible architecture of WiNoC makes it an attractive option for future CMPs to tackle a large number of cores [38, 39, 58, 66]. Most of the WiNoC architectures proposed in the literature have adopted regular topological structures to take advantage of their modularity, scalability, and simplicity [37, 40, 44, 67–70]. Each radio hub is composed of an antenna and a transceiver that are clustered with a set of processing cores with shared wireless bandwidth among them. However, due to the limited wireless channel bandwidth, the radio hubs are susceptible to congestion as the wireless channel is shared with all processing cores [61, 69–74]. The waiting time to get access to wireless channels is the main factor of congestion in radio hubs. This leads to possibility of radio hub overloading and causing network contention due to multiple access requests to the wireless channel at the upper layer of WiNoC. Consequently, this deprecates the benefit of high-speed wireless links offered by WiNoC [68–70, 75]. In addition, from the parallelism standpoint, the bandwidth for a wireless channel is much less than the aggregate bandwidth of all wired metal interconnects. Hence, to achieve the best WiNoC performance, there is a necessity to devise a routing mechanism that can select the use of either wired or wireless channel bandwidth for data packet transmission.

1.3 Objectives

The aim of this thesis is to improve the network performance of the mesh-WiNoC architecture by improving the MAC protocol and WiNoC packet routing. The specific research objectives are as follows:

1. To propose a bidirectional medium access control protocol to improve wireless access performance at the upper-layer of the mesh-WiNoC architecture. The bidirectional MAC provides bidirectional links with the control mechanism in the radio hub that allow the token to turn to its previous adjacent radio hub to reduce the full round maximum waiting time.
2. To formulate the distance-aware routing mechanism to improve network performance at the lower-layer of the mesh-WiNoC architecture. This approach uses a distance-aware routing technique to allow a single-hop wireless transmission exclusive to source and destination cores beyond a certain distance threshold for the long-range cores communication.

1.4 Scope of Work

The WiNoC performance validation at the system level requires simulating CMP with WiNoC interconnection. However, due to the expensive costs involved in prototyping the WiNoC Integrated Chip (IC), the hardware implementation of the proposed work is outside the scope of this thesis. Therefore, as the norm in the computer architecture research, a cycle-accurate full system WiNoC architecture simulation is employed as evaluation of the proposed works. The scope of work for this thesis is summarized as follows:

- The investigated architecture is mesh-WiNoC with a system size of 64 cores, as it is a sufficient size to demonstrate NoC based multicore system-on-chip (SoC). [2, 3, 76–80].
- Since the investigation in this thesis emphasised on the MAC protocol and routing techniques, all NoC routers have access to both wired and wireless

channels as part of the WiNoC topological structure. Single-channel wireless access is assumed to be available for WiNoC integration.

- The dimension-order XY routing algorithm is adopted because it can provide the shortest path routing with respect to the mesh-WiNoC topology. In addition, XY deterministic routing gurantees deadlock and livelock freedom [11–13].
- The proposed designs are developed in C++ and SystemC with an object-oriented programming (OOP) approach in the Noxim [81] NoC simulator that supports wireless communication.
- Validation of the proposed works presented in the thesis is evaluated on the Noxim [81] NoC simulator with synthetic traffic distributions (random, shuffle, transpose and hotspot) and existing application specific benchmark suites (PARSEC [82] and SPLASH-2 [83]) namely Barnes (high-performance application) and Fluidanimate (interactive animation application) respectively.
- The works are evaluated based on common evaluation metrics analysis [13, 84, 85] for on-chip network system in term of transmission latency, network throughput and energy consumption .

1.5 Expected Contributions of this Thesis

This work proposes two strategies dedicated for mesh-WiNoC architecture to accomplish the thesis objectives that can improve the WiNoC performance. The expected research contributions are as below.

1. Bidirectional MAC protocol for the mesh-WiNoC wireless channel

   In this thesis, a bidirectional MAC protocol is proposed as the first contribution aiming at reducing the maximal token waiting time for the case of token full round-trip time. At the upper-layer, the MAC mechanism plays an essential role in ensuring the correct operation of the mesh-WiNoC architecture. This approach is aimed at improving the MAC delay with the bidirectional links that enable the token to be given to its preceding hub node rather than completing a full round of the daisy-chained token ring. A lightweight bidirectional MAC

protocol is designed, modeled, and evaluated with the baseline implementation with a set of common traffic scenarios, seeking to prove the better performance of the proposed approach over the baseline model.

2. Distance-aware routing scheme for the mesh-WiNoC architecture

   As a continuation of the first objective, this thesis formulates the distance-aware routing scheme at the network layer. Based on the hop distance between the source and destination pair, this scheme selectively decides the use of either wired or wireless communication for packet transmission. By implementing the distance aware routing, a single-hop wireless transmission can be exploited for far-away cores as an express communication to bypass the multi-hop transmission between processing cores. Nevertheless, short-range communications are served through wired metal communication to accommodate its much greater aggregate communication bandwidth as compared with a wireless link. As a result, by appropriately balancing the network workload between wired and wireless paths, the WiNoC performance is expected to be improved. Furthermore, this work performs a thorough analysis of the proposed design with a set of synthetic and benchmark (PARSEC [82] and SPLASH-2 [83]) traffic workload. It is expected that the integration of both strategies, bidirectional MAC and distance-aware routing, can provide profound benefits in terms of the execution speed and a better energy profile for the mesh-WiNoC architecture.

1.6 Thesis Organization

The remainder of the thesis is structured as follows.

- **Chapter 2** provides the fundamental background of WiNoC communication and taxonomizes the existing literature's emphasis on MAC protocol and WiNoC routing before detailing the proposed works and its contributions. This chapter first describes a brief overview of NoC architecture technologies and the foundation background of WiNoC. This chapter also discusses the related

work on the adopted MAC mechanisms and routing strategies in the WiNoC architecture.

- **Chapter 3** presents the bidirectional MAC with the distance-aware routing mechanism as the thesis's proposed works. This chapter describes the top-down perspective of the proposed designs and the research workflow carried out in this research. This chapter also covers the design platform, software tools, and performance metrics employed for this thesis.
- **Chapter 4** discusses the experimental results with comparative performance analysis between baseline architecture against the proposed works. This chapter describes the evaluation environment and analyses the performance of the proposed works under both synthetic and application specific benchmark traffic distributions.
- **Chapter 5** concludes the thesis with a summary of lessons learned and pathways that could be explored as future research work.

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