DEVICE SIMULATION OF THE ELECTRICAL CHARACTERISTICS IN 14NM GAUSSIAN CHANNEL JUNCTIONLESS FINFET

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DEDICATION

This thesis is dedicated to my father, who taught me that the best kind of knowledge to have is that which is learned for its own sake. It is also dedicated to my mother, who taught me that even the largest task can be accomplished if it is done one step at a time.

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ABSTRACT

In conventional FinFET, it becomes difficult to define the doping concentration of material over a distance shorter than 10nm and produce high-quality junctions for sub 20nm regime which leads to short channel effects. Hence, Junctionless FinFET which offers architecture, free from any p-n junction is able to overcome the short channel effects. JL FinFET acts like a gated resistor and it has uniform high doping ($\sim 10^{19}$ to 10^{20} cm^{-3}) from source to drain throughout the silicon channel to maintain a high drive current in ON state. The prominent advantages of this device include low leakage current, low parasitic capacitance, reduced Drain Induced Barrier Lowering (DIBL), and excellent I_{on}/ I_{off} ratio which made them a viable option for low-power logic applications. Apart from their advantages, the most important issue for the fabrication of Junctionless devices is achieving a uniform doping concentration in the device layer, especially in non-planar structures like FinFET. In FinFET, doping of the fin region has to be performed in a 3D fashion which results in non-uniform doping around the fin. Hence the most general doping profile is the Gaussian which is considered as a solution for this doping concern. This work presents the design and optimization of the 14nm Gaussian Channel Junctionless FinFET (GC-JLFinFETs) using Silvaco TCAD simulator. In this study, the results are validated using the conventional FinFET and the structure is optimized to improve the ON current (I_{on}) with a simultaneous decrease in the OFF current (I_{off}), Subthreshold Swing (SS), and Drain-Induced Barrier Lowering (DIBL). Hence the structure is optimized with respect to the device parameters such as high-k spacer dielectric, low-k gate dielectric, and spacer width. The Gaussian doping profile in JL-FinFET structure is analyzed with the peak of 4×10^{19} cm^{-3} placed at the sidewalls of Fin and gets reduced gradually towards the center of the Fin with the standard deviation of 1nm/dec. The gate work function of all the configurations of FinFET was adjusted to obtain a 400mV threshold voltage for a meaningful comparison. In order to further reduce the leakage current of the device, Punch Through Stop Layer (PTS layer) has been added beneath the channel. The IV characteristics are simulated for both n- and p-type FinFET exhibits good compliance with the experimental results of Intel. For a fair device simulation, the device is carefully calibrated using the experimental results thus validating the simulation results. The simulated values interpret that the $I_{on}=101.5\mu A/\mu m$ is obtained for the simulated device structure. The simulated design shows better efficiency in terms of short channel characteristics namely DIBL= 25.3 mV/V, SS = 63.88 mV/dec, Transconductance =3.621x10^5S/μm, and the overall efficiency of the device is improved by 25.63%. The work is further extended to its application in inverter circuits using the SPICE simulator to analyze the circuit level performance of the simulated structure. In SPICE level, the circuit is subjected to DC and transient analysis for its feasibility in real-time application of the device, and the obtained improvement is 42.58%.

ABSTRAK

Dalam FinFET konvensional, agak sukar untuk menentukan bahan kepekatan dopan bagi jarak saluran kurang daripada 10nm dan sukar untuk menghasilkan simpang berkualiti tinggi untuk rejim sub-20nm yang membawa kepada kesan saluran pendek. Oleh itu, FinFET tanpa simpang (JL) yang menawarkan struktur peranti yang bebas dari simpang p-n mampu mengatasi kesan saluran pendek ini. JL FinFET bertindak seperti perintang berpagar dan ia mempunyai dopan tinggi yang seragam ($\sim 10^{19}$ hingga 10^{20} cm^{-3}) dari source to drain di sepanjang lapisan silikon untuk mengekalkan arus pemacu tinggi bagi keadaan ON. Kelebihan utama peranti ini termasuk arus bocor dan kapasitans parasit yang rendah, pengurangan terhadap salir teraruh sawar menurun (DIBL) dan nisbah Ion/Ioff yang sangat baik yang menjadikannya sebagai pilihan yang sesuai untuk aplikasi logik berkuasa rendah. Bagaimanapun, proses fabrikasi untuk peranti tanpa simpang adalah bagi mendapatkan kepekatan dopan yang seragam pada lapisan silikon bukanlah perkara mudah terutamanya pada struktur bukan satah seperti FinFET. Di dalam FinFET, pengedopan di sekitar kawasan sirip harus dilakukan dengan cara 3D yang akan mengakibatkan pengedopan menjadi tidak seragam di seluruh kawasan sirip. Oleh itu, profil pengedopan berbentuk Gaussan diperkenalkan bagi menyelesaikan permasalahan ini. Di dalam kerja ini, simulator rekabentuk-berbantukan- teknologi komputer (Silvaco TCAD) digunakan untuk kerja-kerja reka-bentuk dan pengoptimuman 14nm FinFET tanpa simpang dengan Saluran Gaussan (GC-JLFinFETs). Di dalam kajian ini, hasil dapatan dari simulasi ini dibanding dan disahkan dengan FinFET konvensional dan struktur peranti dioptimumkan bagi meningkatkan arus ON, secara serentak menurunkan arus OFF, sub-ambang berayun (SS) dan salir teraruh sawar menurun (DIBL). Oleh itu, struktur dioptimumkan berkenaan dengan parameter peranti seperti dielektrik peruang k tinggi, dielektrik get rendah k dan lebar peruang. Profil pengedopan Gaussan dalam struktur JL-FinFET dianalisis dengan kemuncak 4 x 10^{19} cm^{-3} diletakkan pada dinding sisi sirip dan dikurangkan secara beransur-ansur ke arah tengah sirip dengan sisihan piawai 1nm/dec. Fungsi kerja get semua konfigurasi FinFET telah dilaraskan untuk mendapatkan voltan ambang 400mV untuk perbandingan yang bermakna. Untuk mengurangkan lagi arus kebocoran peranti, lapisan tebuk tembus penghenti (lapisan PTS) telah ditambah di bawah saluran. Ciri IV disimulasikan untuk FinFET jenis n- dan p- menunjukkan pematuhan yang baik dengan keputusan hasil eksperimen Intel. Untuk simulasi peranti yang adil, peranti dikalibrasi dengan teliti menggunakan hasil eksperimen seterusya mengesahkan hasil simulasi. Hasil simulasi menunjukkan I_{on} = 101.5µA / µm diperoleh untuk struktur peranti yang telah direka bentuk. Reka bentuk yang dicadangkan menunjukkan kecekapan yang lebih baik dari segi ciri saluran pendek iaitu DIBL = 25.3 mV/V, SS = 63.88 mV/dec, Transconductance = 3.62×10^5 S/µm dan kecekapan keseluruhan peranti meningkat sebanyak 25.63%. Kerja ini diperluaskan lagi kepada aplikasinya dalam litar penyongsang menggunakan simulator SPICE untuk menganalisis prestasi tahap litar struktur simulasi. Dalam peringkat SPICE, litar tertakluk kepada analisis DC dan analisis fana untuk kebolehlaksanaannya dalam aplikasi masa nyata peranti, dan peningkatan yang diperolehi ialah 42.58%.

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LIST OF ABBREVIATION

BGN	–	Band-Gap-Narrowing
BOX	–	Buried Oxide Layer
BTBT	–	Band-to-Band-Tunneling
CMOS	–	Complementary-Metal-Oxide-Semiconductor
DC	–	Direct Current
DGJLT	–	Double-Gate Junctionless Transistor
UD-DGJLT	–	Uniformly Doped Double-Gate Junctionless Transistor
DG-DGJLT	–	Differentially Graded Double-Graded Junctionless Transistor
JL-FinFET	–	Junctionless Fin-Field-Effect Transistor
GC-JLFinFET	–	Gaussian Channel Junctionless Fin-Field-Effect Transistor
DIBL	–	Drain Induced Barrier Lowering
EDA	–	Electronic Design Automation
EOT	–	Effective Oxide Thickness
FET	–	Field-Effect-Transistor
FinFET	–	Fin-Field-Effect Transistor
GAA	–	Gate All Around
IM	–	Inversion Mode
ITRS	–	International Technology Roadmap for Semiconductor
JNT	–	Junctionless Nanowire Transistor
LUT	–	Look-Up-Table
MOSFET	–	Metal Oxide Semiconductor Field-Effect-Transistor
NMOS	–	n-channel Metal Oxide Semiconductor
PDP	–	Power-Delay-Product
PMOS	–	p-channel Metal Oxide Semiconductor
PTM	–	Predictive Technology Model

PTS Layer	–	Punch-Through-Stop Layer
SCE	–	Short Channel Effects
SNM	–	Static Nosie Margin
SoC	–	System-On-Chip
SOI	–	Silicon-On-Insulator
SRAM	–	Static Random-Access Memory
SS	–	Subthreshold Swing
TCAD	–	Technology Computer Aided Design
UD-JLFinFET	–	Uniformly Doped Junctionless FinFET
WF	–	Work Function

LIST OF SYMBOLS

σ_n	–	Straggle Length
μ_{eff}	–	Effective Mobility
V_{th}	–	Threshold Voltage
$I_D V_G$	–	Drain Current Versus Gate Voltage
I_{on}	–	Drain Saturation current
I_{off}	–	Leakage current
I_{on}/I_{off}	–	On-to-Off Current Ratio
g_m	–	Transconductance
k_{sp}	–	Spacer Dielectric Constant
N_{CH}	–	Channel Doping Concentration
HfO_2	–	Hafnium Dioxide
L_g	–	Gate Length
L_{sp} or L_{SP}	–	Spacer Length
W_{top}	–	Top-fin width
W_{bottom}	–	Bottom-fin width
H_f	–	Fin Height
F_w	–	Fin Width
F_h	–	Fin Height
N_{sd}	–	Source/Drain Doping
SiO_2	–	Silicon Dioxide
t_{si}	–	Channel Layer Thickness
t_{sub}	–	Substrate Layer Thickness
t_{box}	–	BOX Layer Thickness
t_{ox}	–	Oxide Thickness
V_{DD}	–	Small Supply Voltage
V_{DS}	–	Source Drain Voltage
V_g	–	Gate Voltage
V_{th}	–	Threshold Voltage
W/L	–	Width to Length Ratio

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1   Research Background

In 1965, Gordon Moore, the co-founder of Intel introduced Moore's law which states that the since the discovery of transistors, the number of transistors present in a single chip had been doubled every two years as interpreted in Figure 1.1. This is the reason which made Moore anticipate that the same trend would continue for a long run. The trajectory of electronics has been transformed radically in the day-to-day operations of users for the past 50 years.
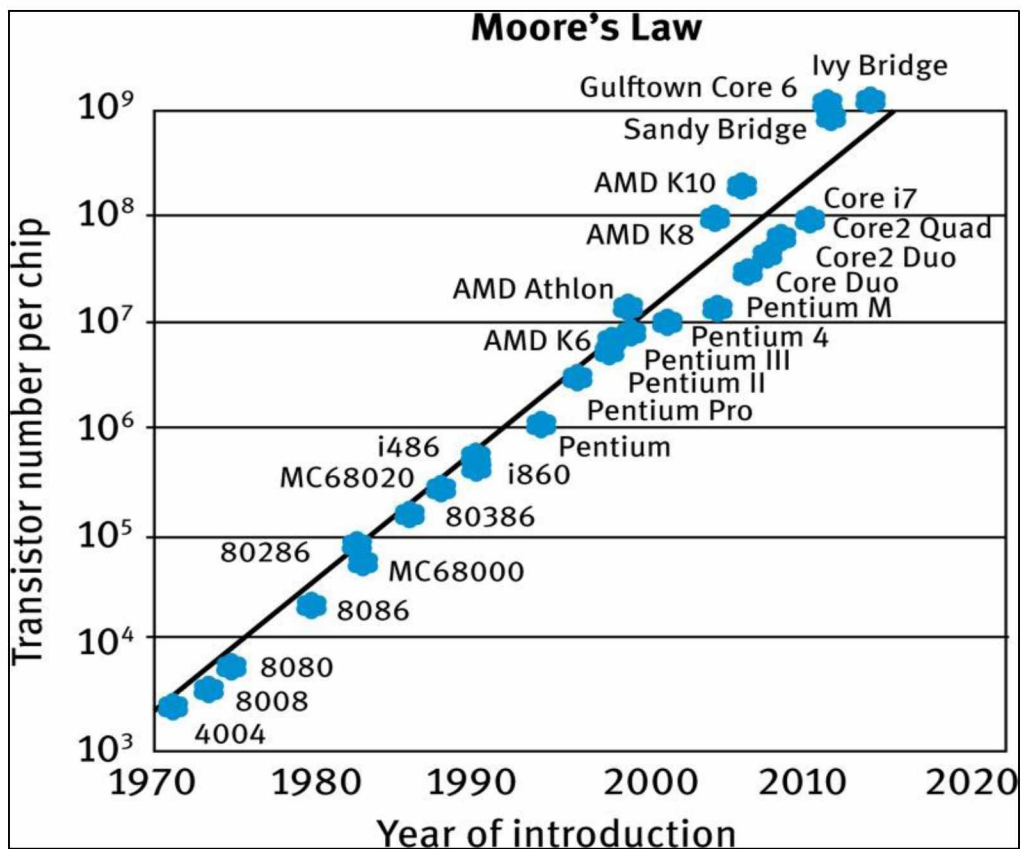
Figure 1. 1   Trend of Moore's law [1]

The prophesy of many experts is that due to the economical and physical constraints of shrinking the transistors would come to an end by 2017, whereas many other experts predict that Moore's law will hold true for another one or two decades [1]. According to ITRS estimations, the 3nm node should be accessible in 2022, but the industry is still a long way off. Intel recently disclosed in July 2020 that its plan to manufacture the 7 nm node have been postponed until at least 2022. The basic solution for consistent progress in the Semiconductor industry based on silicon devices is CMOS scaling. As many numbers of transistors can be incorporated on to a single chip, more complex computational performance will be enabled with improved circuit density and performance.

However, the scaling of the device continues even in the 21st century, it turns out that the Moore's law can't be maintained by typical device scaling theory. The demand in the Silicon-based semiconductor industries is to produce a high performing transistor with high drain current and lower consumption of power. Thus, it can be achieved by dimensions of the Metal-Oxide-Semiconductor transistor. However, the constant reduction in the dimension will not always adhere to the efficiency, performance of the device, instead it rises issues. As the size of the transistor is sized down to sub 20nm technology, there rises many concerns related to the manufacturing and efficiency.

As the transistor is gradually scaled down to sub 20nm regime, it becomes difficult to fabricate and various device processing issues arises. These issues are arised because of the presence of metallurgical junctions in the transistors with the gate length less than 20nm [1-3]. In addition to the above-mentioned problems, the transistor is subjected to various Short Channel Effects. Transistors are the main components in electronic applications such as calculators, personal computers, smartphones etc. The demand for these electronic applications had increased from time to time. Therefore, it is crucial to reduce the size of the transistors in order to increase the number of transistors on one silicon wafer, leading to high-speed integrated circuits. However, by reducing the size of the metal-oxide semiconductor field-effect transistors (MOSFETs) into nanoscale regime, the traditional silicon bulk suffers from

several short-channel effects such as high leakage current, increased Drain-Induced Barrier Lowering and Subthreshold Swing, reduced ON current etc.

1.2   MOSFET Scaling and Limitations

The scaling of transistors is going down to nanometer range from sub-micron scale as illustrated in Figure 1.2. However, the substantial reduction in size may not always be compatible with device performance, posing issues that have yet to be resolved [2]. In order to keep the active power and electric field of the device within the optimum range, there is a corresponding rebate in supply voltage, V_{DD}. The constraint in the reduction of threshold voltage below a certain limit is that the parasitic current contributes a considerable level of power dissipation in the CMOS based HP devices. As formerly mentioned, the V_{DD} of the transistor cannot be reduced below a certain limit corresponding to the gate length, across the gate oxide region there is a surge in electric field. This could possibly cause damage to the device and thus leads to the increase in OFF current.
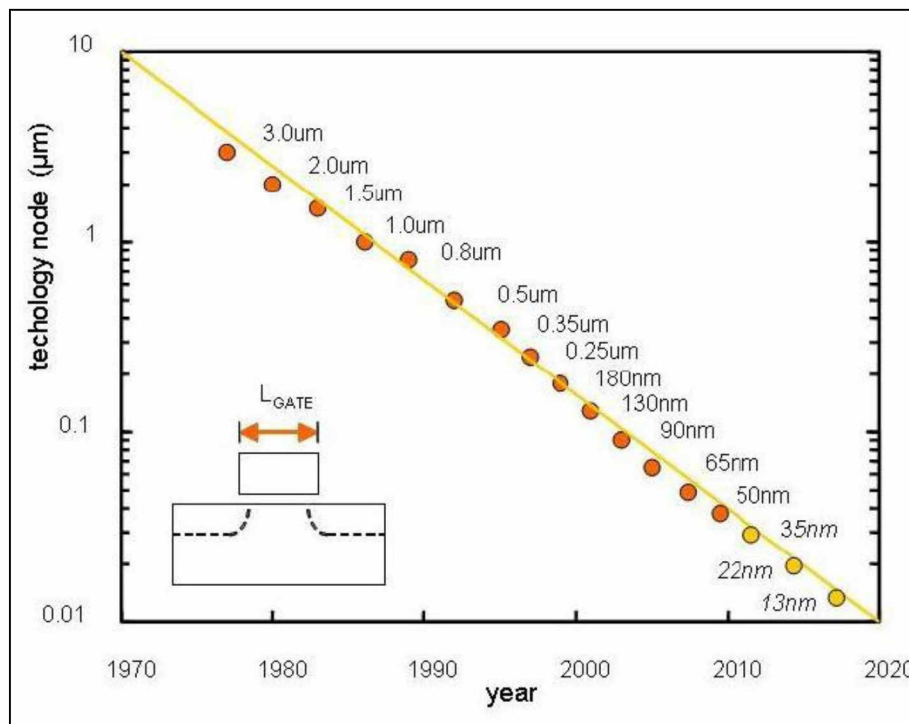
Figure 1. 2   Scaling of MOSFET gate length [2]

The reduction in the size of the transistor unfavorably affects the parasitic or passive capacitance and resistance with the cutback in pitch. This in turn affects the performance gain of the transistor. Furthermore, the high channel doping required poses substantial problems, including as mobility degradation and threshold voltage variations caused by random dopants. When the size of the transistor is scaled down to nanometer regime it will be a tough task to establish the dopant atoms at the specified points. Other problems related to the planar transistors like MOSFET is the dissipation of heat due to the creation of hot spots caused by improper dissipation of heat from the circuit, interconnect delays [2]. Though several methods like high-k dielectric, metal gate and strained silicon are subsequently introduced to overcome the previously mentioned problems in MOSFET, the requirement for additional transistor scaling will necessitate the evolution of the transistor structure itself. This paves way for the introduction of non-planar transistors (such as multiple gates) from planar transistors as depicted Figure 1.3.
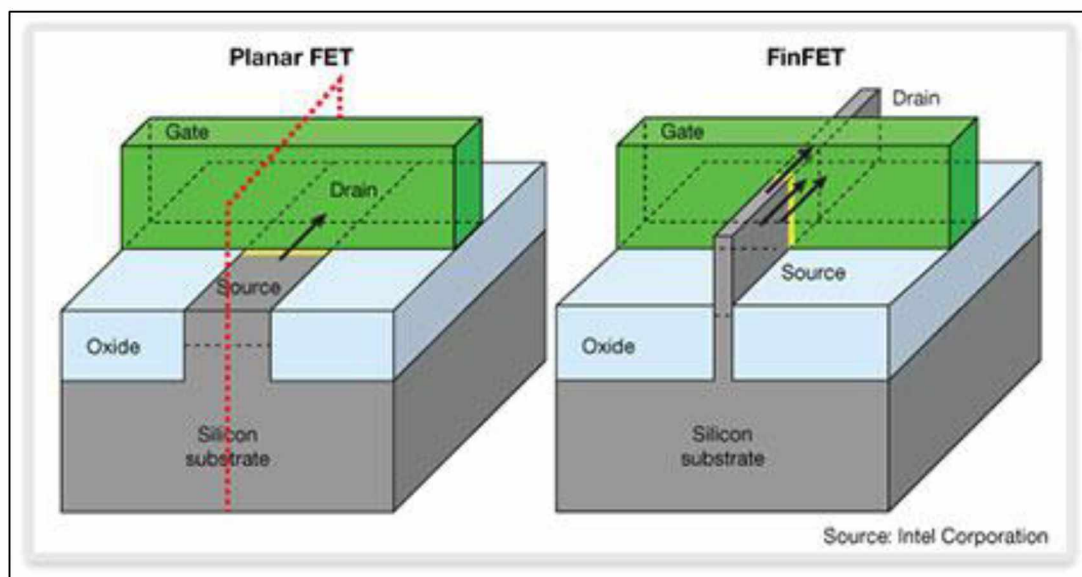
Figure 1. 3   Planar to non-planar structure [3]

The term non-planar defines that the device is not restricted to only one plane. It is also said to be 3-Dimensional in shape as it has a third dimension (z-plane). FinFET technology derived its name from the fact that the FET structure that looks like a set of fins when viewed. The term FinFET was coined by Chenming Hu et.al [3] at the University of California, Berkeley as a result of the shape of the structure. FinFETs are non-planar structure that rises above the substrate and resemble a fin. The

'fins' form the source and drain to enable more volume than the traditional planar transistor for the same area [3].

Figure 1.4 shows the technology trends of MOSFET [4]. In the recent trends, new device structures such as fin-shaped field-effect transistors (FinFETs) and gate-all-around field-effect transistors (GAAFETs) are implemented. These device structures are introduced to overcome the short channel effects that are found in the sub 20nm regime MOSFET structures. In a brief, FinFET devices outperform conventional MOSFET technology in terms of short-channel characteristics, density of current and time taken for switching.
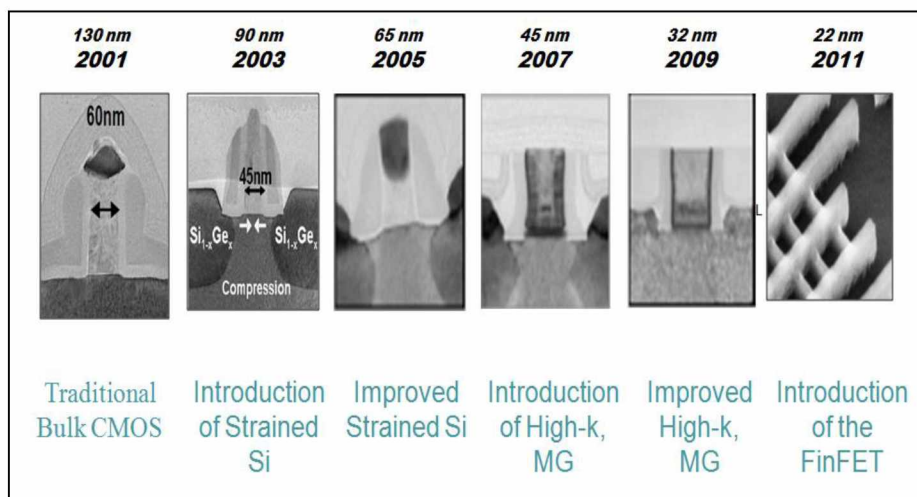
Figure 1. 4   Technology trends of MOSFET [4]

1.3   Problem Statement

In conventional FinFET it becomes difficult to change the doping concentration of a material over distance shorter than 10nm and produce high quality junctions for sub 20nm regime which leads to short channel effects [5]. The fact that Junctionless FinFET contain no junction, it helps the chipmakers to create smaller devices. It has less mobility degradation with temperature and gate voltage than the classical MOSFET. SCEs appeared as a result of the device's constant shrinking dimensions. The drain voltage has no effect on the maximum value of the voltage barrier of the pn junction at the source contact in long channel devices. However, as

the channel lengthens, the barrier becomes more dependent on the drain voltage, affecting all subthreshold device parameters. JL FinFET has better Subthreshold Swing and more effectively suppresses short-channel effects (SCEs) than the conventional bulk FinFET [5]. It acts as a gated resistor and it has a uniform high doping (~ 10^{19} to 10^{20} cm^{-3}) from source to drain throughout the silicon channel to maintain high drive current in ON state. This device is termed as a Junctionless FinFET because it uses bulk conduction when compared to surface conduction in conventional MOSFETs. Apart from their advantages, the most important issue for fabrication of Junctionless devices is achieving uniform doping concentration in the device layer especially in the non-planar structures like FinFET [6].

In FinFET, doping of the fin region has to be performed as a non-uniform doping all around the fin. Hence the most general doing profile is the Gaussian which is considered as a solution for this doping concern [7]. In addition to the aforementioned problems, the device is still affected by the increase in the leakage current. It is to be noted that there is no sufficient research work done on the Gaussian Channel Junctionless FinFET in SPICE level for evaluating its performance in regards to the real time application.

1.4   Research Objectives

The main goal of this research work is to augment the performance of 14nm Junctionless FinFET with Gaussian Doped Channel based on the scaling limitations and trade-offs in the existing FinFET structure, the research objectives are concluded as below

1.   To simulate 14nm Gaussian Channel Junctionless FinFET (GC-JLFinFET) using Silvaco Atlas Tool.

2.   To characterize the electrical properties of 14nm GC-JLFinFET such as Subthreshold Swing, Drain-Induced Barrier Lowering, ON current, OFF current and ON-OFF current ratio.

3.   To analyse the circuit design parameters such as Power, Delay and Power Delay Product for the characterized structures and implement in CMOS inverter using Synopsys HSPICE.

1.5   Research Scopes

This research focuses on the design and optimization of 14nm Junctionless FinFET with Gaussian doped channel. The design parameters and electrical characteristics of the device were calibrated as per International Technology Roadmap for Semiconductors (ITRS) specifications. This research scopes are as follows:

1.   *Simulation Work:* The simulation work is divided into two sections; Device simulation of 14nm Junctionless FinFET with Gaussian doped channel with PTS layer in Technology-Computer-Aided-Design (TCAD) simulator and Device level circuit simulation of the 14nm GC-JLFinFET in an inverter using Hewlett Simulation Program with Integrated Circuit Emphasis (HSPICE). For 14nm Gaussian Channel Junctionless FinFET, conventional FinFET with ITRS set physical parameters for 14nm technology. Later the device is modified to make it Junctionless structure. Afterwards, the device simulation of the GC-JLFinFET with PTS layer is conducted to analyse the performance of the simulated structure. This is further extended to the transistor level implementation in an inverter to evaluate the feasibility in complex digital circuits.

2.   *Analysis Work:* The physical parameters and dimension of the 14nm GC-JLFinFET structure are taken from the previous experimental work performed by [23]. However, the gate length of 14nm is chosen to provide a valid verification of results against the existing structure [23]. The electrical parameters such as ON current, OFF current, SS and DIBL are analysed for the simulated work. The analysis work in TCAD level will be carried out to compare between the performance of the simulated 14nm GC-JLFinFET with PTS layer and previously published work [23]. In order to analyse the

feasibility of the simulated structure at the circuit level, DC analysis and transient analysis is conducted in SPICE.

1.6   Thesis Organization

Chapter 1 is the most important part of this research where the MOSFET structure background and its development are discussed. The Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) scaling and challenges are highlighted. Then, the various types of non-planar structures are introduced and the importance of FinFET is found as the demand to the technology advancement in which the research's problem statements are determined. Based on the problem statements, the research objectives are simulated and the scope of the research work has been identified. Finally, the research contributions have been accentuated.

Chapter 2 discussed the Fin-Field-Effect Transistors where multiple structures are identified and its important characteristics are being highlighted. Furthermore, the concept of Gaussian doped channel with uniform doping in S/D region is explored. Then the SPICE model for Inversion-Mode FinFET and Double-Gate MOSFET structure is analyzed for the circuit level implementation.

Chapter 3 covers the research methodology of the work from the general flowchart, continued by the specific work flow chart for TCAD and SPICE simulations. All the research activities are indexed in this chapter along with tools that were used in this research work are highlighted. In addition to the above-mentioned points, the details related to the approach of the research simulation work are presented. Further the device physical dimensions and parameters in conjunction with the device models are also specified. Lastly, the research work is summarized and discussed analytically.

In Chapter 4, the simulated results are conferred with the characterization of 14nm Gaussian Channel JL-FinFET in TCAD and SPICE level. The electrical parameters such ON current, OFF current, Drain-Induced-Barrier-Lowering (DIBL),

Subthreshold Swing (SS), Transconductance are analyzed in TCAD tool. The simulation results of the 14nm GC-JLFinFET in an inverter circuit is also presented at SPICE level.

Finally, Chapter 5 concludes with all the research findings and research contribution of this work. Besides this, the future extension of this work is also presented to ensure that the research is continued further for an enhanced contributions to this society.

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LIST OF PUBLICATIONS

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1. R. Mathangi, N. E. Alias, A. Hamzah, M. L. P. Tan and N. Mathan, "Performance Analysis of an Efficient Montgomery Multiplier using 7nm FinFET and Junctionless FinFET," 2021 International Conference on Electrical, Communication, and Computer Engineering (ICECCE), 2021. (Oral Presentation)

2. Sule MA, Ramakrishnan M, Alias NE, Paraman N, Johari Z, Hamzah A, Tan ML, Sheikh UU. Impact of Device Parameter Variation on the Electrical Characteristic of N-type Junctionless Nanowire Transistor with High-k Dielectrics, (2020), 4th International Conference on Electrical, Electronic, Communication and Control Engineering (2019). (Oral Presentation)

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1. R.Mathangi, N. Ezaila Alias, Afiq Hamzah, M.L. Peng Tan and Mathan.N. "Design and Analysis of Electrical Characteristics of 14nm Gaussian Channel Junctionless FinFET with Punch Through Stop Layer.", Solid-State Electronics (Submitted to the journal)

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1. R. Mathangi, N. E. Alias, A. Hamzah, M. L. P. Tan and N. Mathan, "Performance Analysis of an Efficient Montgomery Multiplier using 7nm FinFET and Junctionless FinFET," 2021 International Conference on

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