DAMAGE MECHANICS-BASED MODEL FOR RELIABILITY ASSESSMENT OF THROUGH-SILICON VIA INTERCONNECTS

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ABSTRACT

Through-silicon via (TSV) is one of the emerging technology enablers for the 3D Interconnects. TSV configuration consists of conductive materials, such as copper or tungsten, dielectric liner, which is silicon dioxide and silicon as the semi-conductive material. The difference in thermal expansion rates between those integrated materials will cause accumulation of plastic strain at the interface of Cu/SiO_2 during the operation. The research aims to develop a damage mechanic-based model for reliability assessment of through-silicon via interconnects. During thermal excursions, extensive plastic strain is likely to form between materials with different coefficients of thermal expansion. It leads to the accumulation of voids and subsequently, fracture occurs in the critical section. In this development, the response of *Cu* coating with a thickness of 8 μm in a typical package with TSV interconnects is examined. Finite element (FE) analysis is employed along with experiments and published experimental data in establishing a thorough understanding of the mechanics and failure processes of copper interconnects. The accuracy of FE results of TSV model is greatly dependent on the behaviour prescribed for the *Cu* interconnects in the analysis. In this respect, the Johnson-Cook constitutive equation is employed with the material model constants extracted from a series of nanoindentation test data at different displacement rates. The temperature-dependent data are obtained from published nanoindentation test results at varying temperatures. The TSV Interconnects subjected to temperature cycles are examined. Material parameters for cyclic properties are established based on published data on copper coating cyclic test. Johnson-Cook Damage model was utilized to demonstrate the damage characteristic of metallic vias. The FE model is then used to perform the design sensitivity analysis of the TSV. It was found that the plastic strain-based damage model adequately predicts the damage and fracture processes of *Cu*-filled via under temperature changes. Based on the design sensitivity analysis, the minimum radial stress magnitude for TSV array with 15 and 20 μm pitch length is lower than the threshold keep-out-zone (KOZ) stress of σ_{rr} = 69.6 MPa. Thus, the staggered array of 5 μm-diameter TSVs with pitch lengths of 15 and 20 μm could accommodate transistor devices without adversely affecting its performance.

ABSTRAK

Laluan melalui-silikon (TSV) adalah salah satu pemboleh teknologi yang digunakan di dalam penyambungan Tiga Dimensi (3D). Konfigurasi TSV terdiri daripada bahan pengalir, seperti tembaga atau tungsten, lapisan dielektrik iaitu silikon dioksida dan silikon sebagai bahan semikonduktor. Perbezaan antara kadar pengembangan terma antara bahan bersepadu akan menyebabkan pengumpulan terikan tak anjal di bahagian antara muka tembaga/silicon dioksida sewaktu operasi. Tujuan penyelidikan ini adalah bagi membangunkan model berdasarkan mekanik kerosakan bagi penilaian kebolehpercayaan penyambungan laluan melalui-silikon (TSV). Semasa kehadiran terma, terikan tak anjal yang tinggi terbentuk di antara bahan yang berlainan yang setiap satunya mempunyai pekali pengembangan terma yang berbeza yang akan didahului dengan pengumpulan lompang dan kemudiannya, keretakan penuh berlaku pada kawasan setempat di bahagian kritikal. Di dalam pembangunan ini, tindak balas salutan tembaga dengan 8 μm tebal pada pakej tipikal TSV telah diperiksa. Analisis unsur terhingga (FE) digunakan bersama eksperimen dan data eksperimen yang telah diterbitkan bagi meningkatkan pemahaman yang menyeluruh dalam mekanik dan proses kegagalan penyambungan tembaga. Ketepatan keputusan FE bagi TSV sangat bergantung kepada perilaku konstitutif penyambungan tembaga yang digunakan di dalam analisis. Dalam hal ini, persamaan konstitutif tak anjal Johnson-Cook digunakan dengan pemalar model bahan yang tersari daripada data yang diambil hasil dari ujian bersiri lekukan nano pada kadar anjakan yang berbeza. Data bagi kebergantungan bahan terhadap suhu dicapai daripada data yang telah diterbitkan dalam ujian lekukan nano pada suhu yang berbeza. Penyambungan TSV tertakluk kepada kitaran suhu telah diperiksa. Parameter bagi sifat kitaran bahan diambil berdasarkan data daripada ujian kitaran ke atas salutan tembaga yang telah diterbitkan. Model kerosakan Johnson-Cook (JC) telah digunakan bagi menunjukkan ciri kerosakan pada laluan logam. Model FE kemudiannya digunakan untuk menganalisa kepekaan rekabentuk TSV. Daripada kajian ini, telah didapati bahawa model kerosakan berdasarkan terikan tak anjal boleh digunakan untuk meramal kerosakan dan proses keretakan pada isian-tembaga di bawah perubahan suhu. Berdasarkan analisis kepekaan rekabentuk, nilai tegasan radial 15 dan 20 micrometer jarak antara TSV lebih rendah daripada nilai tegasan zon simpan (KOZ) dengan nilai 69.6 MPa. Oleh itu, TSV dengan diameter 5 μm dan jarak antara TSV, 15 μm dan 20 μm boleh memuatkan peranti transistor di sekitarnya tanpa mempengaruhi prestasi TSV.

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LIST OF ABBREVIATIONS

2D	-	Two-Dimensional
3D	-	Three-Dimensional
3DIC	-	Three-Dimensional Integrated Circuit
3D-LSI	-	Three-Dimensional Large Scale Integration
AFC	-	Armstrong-Frederick-Chaboche
ASTM	-	American Society for Testing and Materials
BGA	-	Ball Grid Array
CDM	-	Continuum Damage Model
CFDM	-	Central Finite Difference Method
CMOS	-	Complementary Metal Oxide Semiconductor
CS	-	Cowper-Symonds
CTE	-	Coefficient of Thermal Expansion
DC	-	Direct Current
DOE	-	Design of Experiment
DRAM	-	Dynamic Random Access Memory
EDX	-	Energy-Dispersive X-ray
EM	-	Electromagnetic
FE	-	Finite Element
FEM	-	Finite Element Method
HIR	-	High Impact Research
IC	-	Integrated Circuit
ITRS	-	International Technology Roadmap for Semiconductors
JC	-	Johnson-Cook
JEDEC	-	Joint Electron Device Engineering Council
KOZ	-	Keep-Out-Zone
LEFM	-	Linear Elastic Fracture Mechanics
PEEQ	-	Equivalent Plastic Strain
RF	-	Radio Frequency
RSM	-	Reference Surface Method
SEM	-	Scanning Electron Microscopy

SPICE	-	Simulation Program with Integrated Circuit Emphasis
SPM	-	Scanning Probe Microscopy
TSV	-	Through-Silicon Via
VCCT	-	Virtual Crack Closure Technique
VIA	-	Vertical Interconnect Access
ZA	-	Zerili-Armstrong

LIST OF SYMBOLS

A	-	Johnson-Cook yield stress at reference condition
A_p	-	Projected contact area
B	-	Johnson-Cook strain hardening coefficient
b	-	Speed of stabilization
C	-	Johnson-Cook dimensionless strain rate hardening
C_A	-	Armstrong-Frederick-Chaboche hardening modulus
C_{Ai}	-	Armstrong-Frederick-Chaboche initial hardening modulus
D	-	Damage variable
$\dot{D}$	-	Damage rate
E	-	Young's modulus
E_c	-	Young's modulus of coating
E_D	-	Damaged state after loading
E_i	-	Young's modulus of indenter
E_o	-	Young's Modulus of the material in the initial undamaged state
E_r	-	Reduced modulus
F	-	Plastic potential of associated flow rule
G_f	-	Fracture energy
H	-	Hardness value
h_c	-	Contact depth
h_{max}	-	Maximum height
L	-	Characteristic length of the element
m	-	Johnson-Cook temperature sensitivity
n	-	Johnson-Cook power exponent of strain rate hardening
P_{max}	-	Maximum load
Q_∞	-	Saturation value of the yield surface
R	-	Drag stress (expansion size of yield surface)
R_i	-	Range of strain rates during nanoindentation test
S	-	Slope at the peak load

T^*	-	Johnson-Cook homologous temperature
T_{melt}	-	Melting temperature
$T_{\text{reference}}$	-	Reference temperature
$\bar{u}^{pl}$	-	Equivalent plastic displacement
$\bar{u}_f^{pl}$	-	Equivalent plastic displacement at failure (damage evolution)
v_c	-	Poisson's ratio of coating
v_i	-	Poisson's ratio of indenter
v	-	Poisson's ratio
W	-	Work done by nanoindentation test
α	-	Coefficient of Thermal Expansion
$\alpha'_\circ$	-	Initial value of backstress
$[\alpha']$	-	Deviatoric back stress tensor
$[\alpha]$	-	Backstress tensor
β	-	Constant for Berkovich indenter
γ	-	Rate of displacement for hardening modulus
ΔA	-	Apparent area (undamaged surface)
ΔA_{void}	-	Area with micro-voids
$\Delta\tilde{A}$	-	Changes of the effective area
ΔF	-	External loading force
Δt	-	Temperature different
ε	-	Strain
$\dot{\varepsilon}^*$	-	Johnson-Cook dimensionless strain rate
$\dot{\varepsilon}_\circ$	-	Johnson-Cook normalize reference strain rate
$\varepsilon_{pl,a}$	-	Plastic strain amplitude
$\varepsilon_e^{pl,0}$	-	Initial value of equivalent plastic strain
$\bar{\varepsilon}_f^{pl}$	-	Equivalent plastic strain at fracture
$\bar{\varepsilon}_D^{pl}$	-	Effective plastic strain at the damage initiation
$\dot{\bar{\varepsilon}}^{pl}$	-	Equivalent plastic strain during the damage evolution stage
$[\varepsilon_{pl}]$	-	Plastic strain tensor
η	-	Stress triaxiality
$\sigma_\circ$	-	Initial yield stress

σ_a	-	Stress amplitude
$\tilde{\sigma}$	-	Effective stress
σ_m	-	Mean stress
$\bar{\sigma}$	-	Equivalent stress
σ_Y	-	Yield stress
$\sigma_{Y_\circ}$	-	Value of yield stress when damage criterion is met
φ	-	Direction of the flow
ω_D	-	Internal state variable

CHAPTER 1

INTRODUCTION

1.1 Research Background

Through-silicon via (TSV) is the current emerging 3D interconnect enabler that uses the vertical connection of conductive material that passes through a silicon wafer in order to complete the electrical circuit for stacking devices in three dimensions (3D) system [1, 2]. This technology was first adapted for complementary metal-oxide-semiconductor (CMOS) image sensor. TSVs were fabricated on the back of the image sensor wafer to form interconnects and eliminate wire bonds. The advantages of applying this type of interconnection application to 3D stacked chip are it can improve electrical performance with very small serial inductance of less than 30 picohenry (pH) as well as achieving higher space efficiency comparable to wire bond technology [3, 4]. These can be seen from Figure 1.1 where the short length of TSV and no spacer required. Its lead to the small electric delay from the package substrate to the top chip. In addition, the chips can be mounted very near between power and the ground vias without additional traces on package substrate resulting in smaller package size. This new emerging practice of interconnection will give a new dimension to the micro and nano-electronic field in terms of applications and in pursuing minute device in the global market.

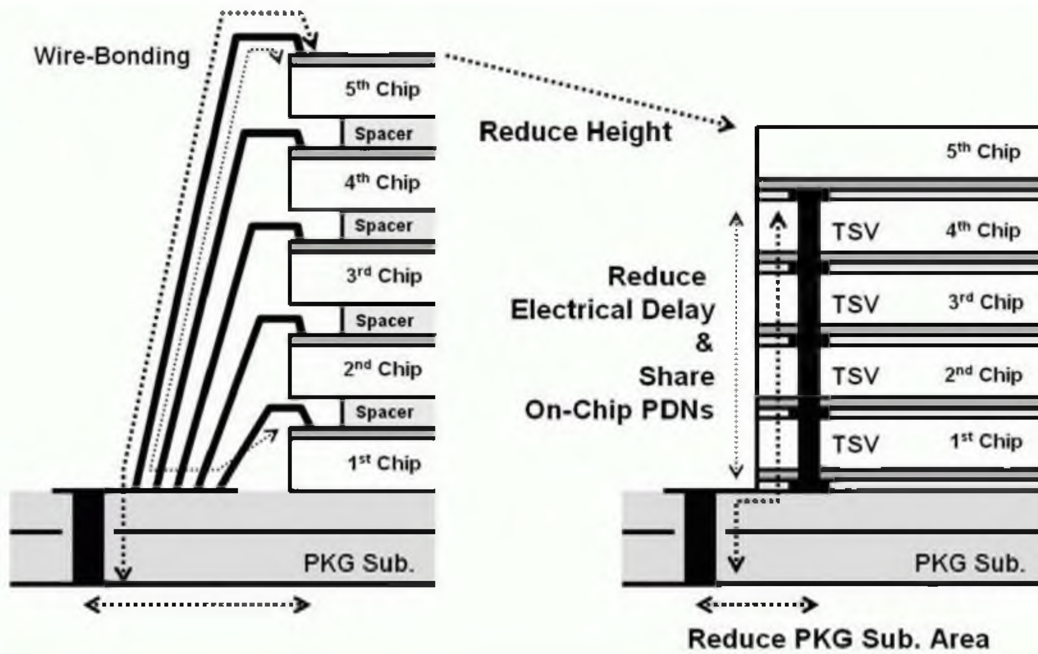

Figure 1.1 Advantages of TSV for 3DIC interconnect application [3]

The technology had moved into the commercialization phase at which the economic realities will determine which interconnect technology will be adopted. TSV is one of the solutions seek by most of the microelectronic industries for their higher integration. Almost 50 organizations identified working in this area of study [5]. Table 1.1 shows the company that used 3D TSV in the microelectronic packaging market. The earliest commercialization date was in 2011 which pioneered by Nanya Technology based in Taiwan.

Table 1.1 3D TSV commercialization [4]

Company	3D with TSV (Commercialization Year)
TSMC	2012-2013
UMC	2nd Half of 2011
Global Foundries	2013
Samsung	2012
Elpida	2nd Half of 2011
Micron	2012
Nanya	2011-2012
STATSChipPAC	2013
SPIL	2012
Qualcomm	2013
Nokia	2012-2013
Dell	2012

The size of the TSV is usually depicted using pitch distance. Pitch distance is measured between the centres of vias to its neighbouring vias. It is found that the trend of pitch distance is reduced throughout the years and the technology roadmap is shown in Figure 1.3. Two technologies are illustrated in this figure, which is current three-dimensional large-scale integration (3D-LSI) and advanced 3D-LSIs where represented by upper line and the lower line respectively. LSI defines the technology used to build microchips or integrated circuits (IC) in a very small form factor. LSI consists of thousands of transistors that are closely embedded and integrated with a very small microchip. Current 3D-LSI is the technology which the TSVs are formed under the peripheral bond pads while for advanced 3D-LSI, the circuit blocks in stacked chips need to connect directly with fine pitch TSVs and microbumps. Figure 1.2 shows the schematic view of chip size package (CSP) structure for sensor application with current 3D-LSI technology. The pitch distance for current 3D-LSI is in the range of 10 to 50 μm since it is designed based on bond pad pitch without any size modification on the original LSI chip layout. The size range for advanced 3D-LSIs pitch distance is less than 5 μm due to the direct connection between circuit block with fine pitch TSVs and microbumps.

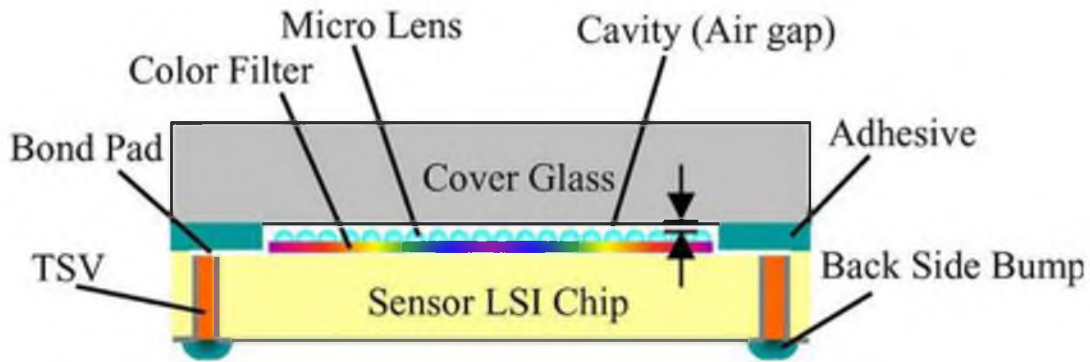

Figure 1.2 Schematic view of a CSP structure for sensor application

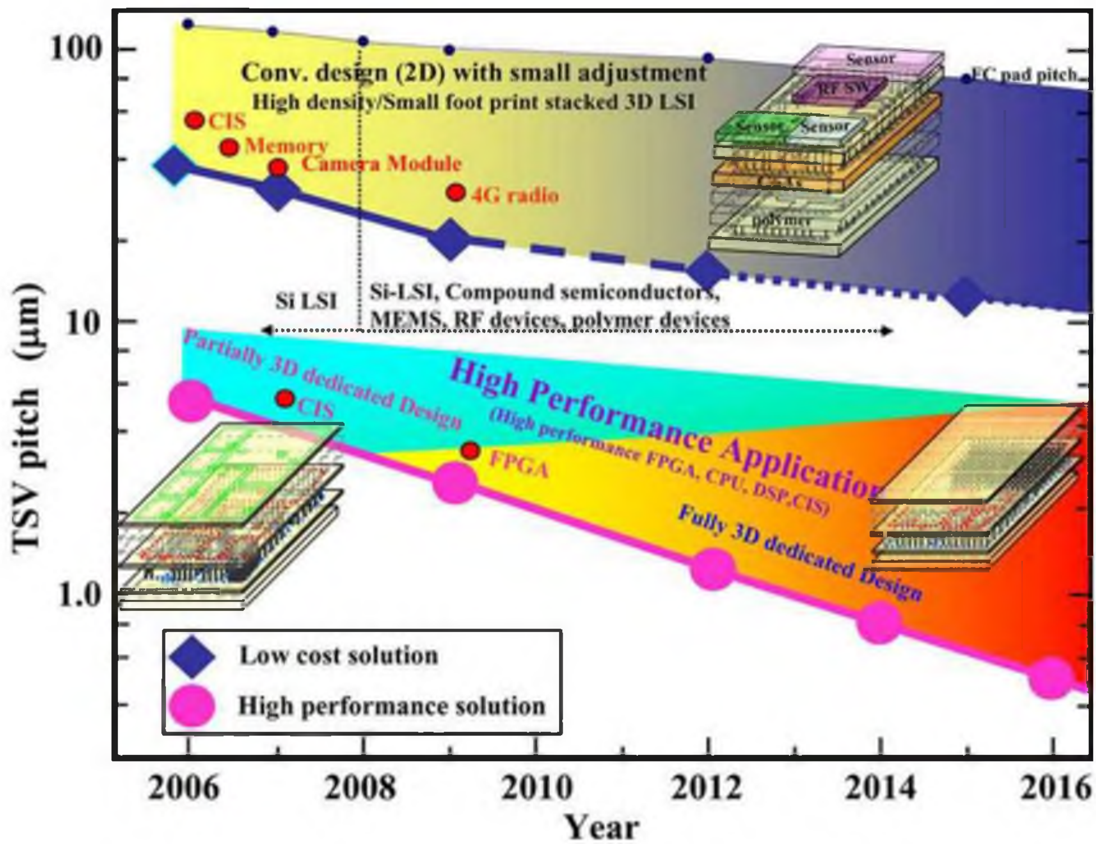

Figure 1.3 TSV for 3D-LSI technology roadmap [6]

Various different materials are involved in the production of TSV namely conductive/filler material, for example, copper (*Cu*) or tungsten (*W*), an insulator to form a barrier layer to avoid diffusion of metal into *Si*-substrate, for instance, silicon dioxide, and silicon wafer. These materials are embedded together to form the TSV which gives a pathway for electrical current to pass through a number of silicon dies layers. Figure 1.4 shows the schematic diagram for the full model interconnection, including ball grid array (BGA) and TSV. The huge challenge faced by the

researcher which relates to the failure of TSV due to the thermal strain on the filler metals adjacent to the interface. Temperature excursions during cyclic temperature loading of reliability test as well as the operating environment will induce strains (consequent stress as a product) at critical point caused by mismatches of the coefficient of thermal expansion (CTE) between two distinct adjacent materials.

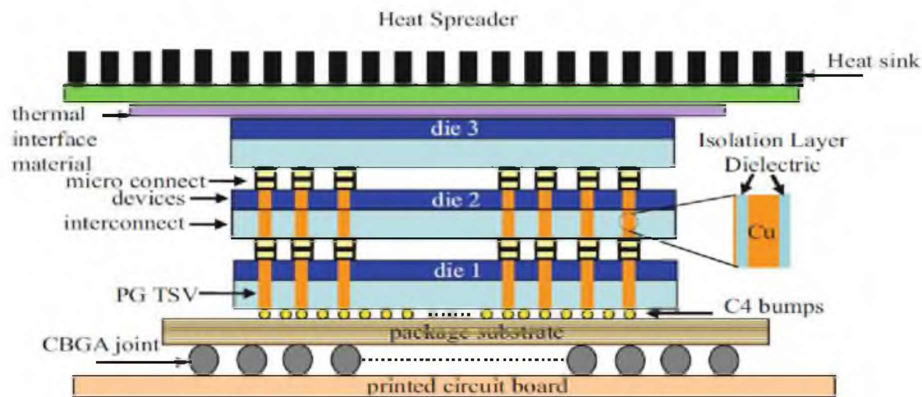

Figure 1.4 Schematic diagram of 3-D Integrated Circuit (IC) [4]

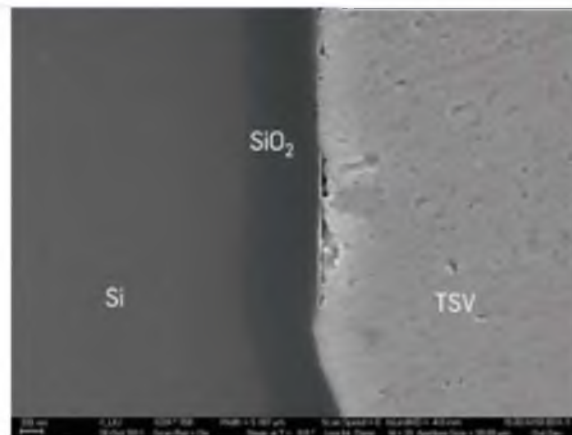

Figure 1.5 Occurrence of failure in TSV [7]

The voids formed in TSV material due to the accumulated strains has been reported in the previously published journal [7] as shown in Figure 1.5. Once there are voids inside TSV material, the effective electric current flow will be affected and hence reduce the reliability of the device. The list of critical issues facing TSV have been discussed by Lau et al. [1] One of the points is the usage of copper fillings helps in reducing thermal problems but increases the thermal coefficient of expansion. This will result in TSV wafer warpage problem owing to the CTE mismatch between silicon and copper.

Thus, a validated framework for reliability assessment of TSVs interconnects is required. The model that can predict the failure occurred on the TSV is expected at the end of this research. The material properties of coating filler are extracted using nanoindentation test and used as an input in the verified model.

This study discusses a framework for the TSV reliability finite element (FE) model, including constitutive and damage response of TSV material. Most of the researchers have yet to acknowledge the continuum damage mechanics approach in the model, although the interface failure model describes in their study [8, 9]. Numerous researchers have highlighted the conventional way of simulating the case up to the elastic-plastic case only rather than move into damage model [10-12]. In comparisons to those previous works, several improvements have been made. These include the establishment of a methodology for determining the constitutive response of coating material using nanoindentation test, development of through-silicon via reliability model utilizing the material model established in the current study and employing a continuum damage model (CDM) for simulating the failure of TSV structure.

1.2 Statement of the Research Problem

A decent design of electronic packaging and material selection can ensure the circuit works properly and hence increasing the reliability of the products. One of the microelectronic company, namely Micron has accept that thermo-mechanical stresses need to be determined in terms of TSV diameter, aspect ratio, and pitch distance [13]. Thus, in this case, an approach to determine the stress level in the electronic component are needed. To date, the modelling approach for the reliability of microelectronic components had been studied especially for a solder joint. The model of solder joint reliability had been vastly studying from linear elastic, plastic until damage. To the author knowledge, existing studies on FE analysis of through-silicon via under thermal-mechanical modelling are limited to plasticity without considering the damage behaviour of the material [7, 14, 15]. Thus, in this study, author would extend the modelling of TSV reliability model by implement a

damage-based approach into the model. In addition to these primary data, the systematic studies on the constitutive response of coatings materials are still needed for better understanding of the characteristics behaviour of coating material in the TSV.

1.3 Objectives

The aim of the research is to develop a damage mechanic-based approach for reliability assessment of TSV interconnects. Specific objectives are:

1. To establish a combined experimental-computational procedure for the determination of mechanical properties of *Cu*-coating.
2. To develop and examine the FE model of TSV for use in reliability prediction.
3. To generate information/ data on the sensitivity of TSV design parameters to local stress distribution in the TSV utilizing the FE model.

1.4 Scope of Study

The present study focuses on development of the FE model of TSV for use in reliability prediction, and is limited to the following scope of work:

1. Copper coated on silicon dioxide/silicon substrate as the demonstrator material. There are two types of deposition process employed which are physical vapor deposition (PVD) and electroless plated method.
2. Metallurgical study including microstructure and chemical composition analysis of the materials. Scanning electron microscopy and optical micrograph are used to analyse the microstructure and measure the thickness, respectively.
3. Perform nanoindentation tests to extract mechanical properties of the copper coating. Different indentation depth ranging from 80 to 320 nm with varying

displacement rates of 80 nm/s to 320 nm/s are employed. Load-displacement response is recorded.

4. The stress-strain equations of the copper coating is represented by the Johnson-Cook model. Johnson-Cook damage model is employed as the criterion for damage initiation of the coating. The cyclic behaviour of the copper layer is modelled using the Armstrong-Frederick-Chaboche material model.
5. FE simulations are performed using the commercial SIMULIA Abaqus ver. 6.12 software. The simulation covers :
    a) Nanoindentation test for the inverse analysis approach.
    b) Sensitivity analysis on TSV and parametric study.

1.5 Significance of Study

Through-silicon via as a 3D interconnect enabler is currently in production. The reliability issue arising from difference thermal loading exposes to the materials always facing by the manufacturers. Therefore, a prediction model through a damage mechanic-based is offered by this thesis. The model effective to use in generating reliability data to develop optimum features of TSV. This is significant for all industrial sectors more importantly in the electronic packaging field. The establishment of reliable predictive models will offer an alternate design and analysis tool for low cost and reduced number of experimental testing.

1.6 Thesis Layout

This thesis consists of seven chapters. It starts with Chapter 1 which discuss in the background of the research and it's complimentary. The issues of reliability for Through-silicon Via and the progress of 3D interconnect technology development in the microelectronic global industry are briefly described. In addition, the objectives, scopes of works and significance of the research are also defined.

Next, Chapter 2 gives a critical review of the current world emerging trends of 3D Interconnect Technology, mechanics of coating material deformation, nanoindentation test, finite element method, temperature- and strain rate-dependent models, continuum damage mechanics, and FE simulation of TSV and summary of the literature review. In fact, this chapter is focused on previous works by other researchers detailing on aforementioned items.

In Chapter 3, the research methodology is present. The method of determining the details of the research material model, experimental setup and FE simulation models are clarified. The input required for FE simulation is discussed. Constitutive response using Johnson-Cook model is employed in monotonic temperature ramp case. Then, for cyclic model, Armstrong-Frederick-Chaboche (AFC) model integrated with the damage model to capture the cyclic behaviour and accumulation of plastic strain inducing damage to the Copper coating in TSV reliability simulation.

The results and discussion are presented in 3 chapters which are chapter 4, 5 and 6.

In Chapter 4, the assessment of deformation processes in nanoindentation test in the form of the typical load-unload graph are presented and discussed. Effects of process and structure on material properties are observed. The elastic modulus and hardness are characterized based on load-depth response through the nanoindentation test.

In Chapter 5, the application of FE simulation to assess the mechanics of deformation in nanoindentation testing is addressed. A computational inverse analysis approach which used to determine inelastic properties of coating materials is introduced. Constitutive curve required for the simulation is obtained through inverse analysis approach.

In Chapter 6, the application of FE to assess the damage mechanics is addressed. By using 3D TSV model, the damage mechanics are examined by

incorporating the JC temperature- and strain-rate dependent criteria for monotonic case, while for cyclic case using Armstrong-Frederick-Chaboche model combines with damage model. The calculated localized stress and strain are characterized. Using the verified FE model, sensitivity parametric analysis has been executed.

In Chapter 7, the main conclusions of the research are present. Finally, future works for refining the research are recommended.

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LIST OF PUBLICATIONS

Indexed Conference Proceedings

1. Afripin MAA, Fadil NA, Hamid MFA, Yoon CK, Cheah BE, Razak BBA, Tamin MN. Rate-dependent responses of electroless plated and sputtered copper layer during nanoindentation loading. 2016 IEEE 37th International Electronics Manufacturing Technology (IEMT) & 18th Electronics Materials and Packaging (EMAP) Conference. 2016 Sept. **(Indexed by SCOPUS)**

2. Afripin MAA, Yoon CK, Tamin MN. Methodology for thermal-mechanical modeling of damage and failure processes in through-silicon-vias. 2017 12th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT); 2017 Oct.7 **(Indexed by SCOPUS)**

Non-indexed Journal

1. Afripin MAA, Yoon CK, Tamin MN. An inverse approach for strain rate-dependent constitutive responses of copper layers. South East Asia, SIMULIA Regional Users Conference. 2016 Oct.