CHARACTERISATION OF ELECTROLESS DEPOSITION PARAMETER OF COPPER ON SILICON WAFER FOR THROUGH SILICON VIA APPLICATION

SHAZATUL AKMALIAH BINTI MIOR SHAHIDIN

A thesis submitted in fulfilment of the
requirements for the award of the degree of
Master of Philosophy

School of Mechanical Engineering
Faculty of Engineering
Universiti Teknologi Malaysia

NOVEMBER 2019

DEDICATION

This thesis is dedicated to my mom and dad, who taught me never to give up and always keep trying.

It is also dedicated to my dearest husband for his patience and support through the years.

And to my little kiddos…
(Umar Aiman, Hamzah Akmal, Maryam Aisyah and baby to born),
thank you for being my angel.

ACKNOWLEDGEMENT

In preparing this thesis, I was in contact with many people, researchers, academicians, and practitioners. They have contributed towards my understanding and thoughts. In particular, I wish to express my most sincere appreciation to my main thesis supervisor, Dr. Nor Akmal binti Fadil, for encouragement, guidance, critics and friendship. I am also very thankful to my co-supervisor Dr. Mohd Zamri bin Mohd Yusop and Ir. Dr. Saliza Azlina binti Osman for their guidance, advices and motivation. Without their continued support and interest, this thesis would not have been the same as presented here.

I am also indebted to the Minister of Education (MOE) for its fundamental research grant scheme (FRGS) that help to fund my Master study. Technicians from material laboratories at School of Mechanical Engineering as well as from central laboratories (UPMU) in UTM, also deserve special thanks for their assistance in helping me conducting the experiments.

My fellow postgraduate student should also be recognised for their support. My sincere appreciation also extends to all my colleagues and others who have provided assistance at various occasions. Their views and tips are useful indeed. Unfortunately, it is not possible to list all of them in this limited space. Last but foremost, I am grateful to all my family member, especially my parents, my beloved husband and lovely kids, for their kind, patience and believe towards me.

Thank you.

ABSTRACT

Through silicon via (TSV) is a structure through entire Si substrate that enables vertical electrical connections between chips. Recently, the electroless deposition of Cu using a chemical bath has received considerable attention as a promising technique for the TSV filling process. Even the advantages of electroless deposition process is well known by the researchers, further investigation is still needed in order to fully optimise electroless deposition process in TSV fabrication. The main objective of this research is to develop Cu deposition on Si substrate by means of electroless deposition method with optimum parameters for the TSV application. Variable pressure scanning electron microscope (VPSEM) was used to observe the morphology of Cu coated on Si substrate. Besides that energy dispersive X-ray (EDX) was used to determine chemical composition and image analyser was used to measure coating thickness of Cu coated layer based on micrographs obtained from VPSEM. Deposition rate was analysed using the coating thickness or weight gain analysis. The adhesion between Cu and Si substrates was tested using cross hatch test. The results showed that each step in electroless deposition method including pretreatment process (etching and activation processes) as well as the electroless deposition process itself affects the result of Cu coated layer conditions. It was found that the pre-treated Si substrate via etching for 5 minutes in 50% volume of hydrofluoric acid solution had a stronger adhesion compared to etched samples in 25% volume of hydrofluoric acid solution. For the activation process during pre-treatment, single step provides greater effectiveness due to better adhesion of Cu coating on Si substrate compared to double step process. The electroless deposition process, at pH 11.5, temperature of 70°C and 1:5 $CuSO_4$ to formaldehyde ratio was selected as the fixed parameters because the chemical formulation studied in this research shows that electroless Cu coating process is a possible method for the TSV filling process. Through this research, the Cu thin layer was able to be deposited up to 3.334 µm thick on the TSV.

ABSTRAK

Laluan melalui silikon (TSV) adalah struktur yang melalui seluruh substrat Si yang membolehkan sambungan elektrik secara menegak antara cip. Baru-baru ini pemendapan elektrolisis Cu menggunakan mandian kimia telah mendapat perhatian sebagai teknik untuk proses pengisian TSV. Walaupun kelebihan proses pemendapan elektrolisis secara umumnya telah diketahui oleh para penyelidik, penyelidikan lanjut masih diperlukan untuk mengoptimumkan proses pengendapan tanpa elektrod sepenuhnya dalam proses penghasilan TSV. Objektif utama kajian ini adalah untuk menghasilkan pemendapan Cu pada substrat Si melalui kaedah pemendapan tanpa elektrod dengan parameter yang optimum bagi aplikasi TSV. Mikroskop imbasan elektron bolehubah tekanan (VPSEM) digunakan untuk memerhati morfologi Cu yang disadur pada substrat Si. Selain dari itu, serakan tenaga sinar-X (EDX) digunakan untuk menentukan komposisi kimia dan penganalisis imej digunakan untuk mengukur ketebalan lapisan Cu berdasarkan mikrograf yang diperolehi dari VPSEM. Kadar pemendapan dianalisis menggunakan data ketebalan saduran atau analisis berat. Lekatan antara substrat Cu dan Si telah diuji menggunakan ujian silang hac. Hasil kajian menunjukkan bahawa setiap langkah dalam kaedah pemendapan tanpa elektrod termasuk proses pra-rawatan (punaran dan proses pengaktifan) serta proses pemendapan tanpa elektrod sendiri mempengaruhi saduran Cu yang terhasil. Didapati bahawa substrat Si yang melalui pra-rawatan secara punaran selama 5 minit dalam 50% isipadu larutan asid hidrofluorik mempunyai lekatan yang lebih kuat berbanding dengan sampel punaran dalam 25% isipadu larutan asid hidrofluorik. Untuk proses pengaktifan semasa pra-rawatan, langkah tunggal memberikan keberkesanan yang lebih besar kerana pelekatan saduran Cu yang lebih baik pada substrat Si berbanding dengan proses dua langkah. Proses pemendapan tanpa elektrod, pada pH 11.5, suhu 70 ° C dan 1: 5 nisbah $CuSO_4$ kepada formaldehid telah dipilih sebagai parameter tetap bagi ujikaji ini kerana perumusan kimia yang dikaji dalam penyelidikan ini menunjukkan bahawa proses saduran Cu tanpa elektrod adalah satu kaedah yang boleh digunakan untuk proses pengisian TSV. Melalui kajian ini, lapisan Cu yang nipis dengan ketebalan sehingga 3.334 µm dapat dimendapkan di dalam TSV.

TABLE OF CONTENTS

	TITLE	PAGE
	DECLARATION	**iii**
	DEDICATION	**iv**
	ACKNOWLEDGEMENT	**v**
	ABSTRACT	**vi**
	ABSTRAK	**vii**
	TABLE OF CONTENTS	**ix**
	LIST OF TABLES	**xiii**
	LIST OF FIGURES	**xiv**
	LIST OF ABBREVIATIONS	**xix**
	LIST OF SYMBOLS	**xx**
CHAPTER 1	**INTRODUCTION**	**1**
1.1	Introduction	1
1.2	Research Background	4
1.3	Problem Statement	6
1.4	Objectives of the Research	7
1.5	Scopes of the Research	8
1.6	Importance of the Research	8
CHAPTER 2	**LITERATURE REVIEW**	**9**
2.1	Through Silicon Via (TSV)	9
	2.1.1 Introduction	9
	2.1.2 TSV Application	9
	2.1.3 TSV Fabrication	11
2.2	Cu Via Filling	18
	2.2.1 Overview	18

2.2.2 Fabrication of Cu Via Filling by Current Practice 18

2.2.3 Critical Issue in Via Filling Process 20

2.2.4 Recent Studies Conducted on Via Filling Process 21

2.3 Electroless Cu Deposition on Si Wafer 23

2.3.1 Overview 23

2.3.2 Electroless Cu Deposition Process Procedure 24

2.3.3 Electroless Cu Deposition Process Mechanism 25

2.3.4 Electroless Cu Deposition Bath Components 27

2.3.5 Effect of Etching Process 30

2.3.6 Effect of Electroless Deposition Process Parameters 32

2.3.7 Summary of Literature Review 35

CHAPTER 3 RESEARCH METHODOLOGY 37

3.1 Introduction 37

3.2 Substrate Material 37

3.3 TSV Fabrication 40

3.4 Electroless Cu Deposition Process 40

3.4.1 Experiment 1: Effect of Etching Process 43

3.4.2 Experiment 2: Effect of Surface Activation Process 44

3.4.3 Experiment 3: Effect of pH and Temperature of Cu Bath 45

3.4.4 Experiment 4: Effect of Cu Bath Concentration 46

3.4.5 Experiment 5: Electroless Cu Deposition on TSV 47

3.5 Adhesion Test 48

3.6 Materials Characterisation 50

3.6.1 Sample Preparation 50

3.6.2 Surface Morphology Analysis 50

3.6.3 Weight Gain Analysis 51

3.6.4 Deposition Rate Analysis 51

3.6.5 Chemical Composition Analysis 52

3.6.6 Visual Analysis 52

3.7 Summary of Research Methodology 52

CHAPTER 4 RESULT AND DISCUSSION 53

4.1 Introduction 53

4.2 Effect of Pre-treatment Process (Etching in Hydrofluoric Acid) 53

4.2.1 Surface Morphology Analysis 54

4.2.2 Cross-sectional Analysis 57

4.2.3 Effect of Etching towards Thickness of the Cu Deposition 62

4.2.4 Cross Hatch Test Analysis 63

4.2.5 Effect of Etching Process on Cu Deposition Mechanism 64

4.2.6 Conclusion 66

4.3 Effect of Pre-treatment Process (Surface Activation) 67

4.3.1 Surface Morphology Analysis 67

4.3.2 Cross-sectional Analysis 71

4.3.3 Effect of Activation Process on Electroless Cu Deposition Mechanism 72

4.3.4 Conclusion 74

4.4 Effect of Electroless Cu Deposition Process (pH and Temperature) 75

4.4.1 Visual Analysis of Electroless Cu Deposited Sample 75

4.4.2 Surface Morphology and Cross-sectional Analysis 79

4.4.3 Electroless Cu Deposition Mechanism 84

4.4.4 Cross Hatch Test 85

4.4.5 Conclusion 87

4.5 Effect of Electroless Cu Deposition Process (Bath Concentration) 88

4.5.1 Surface Morphology Analysis 88

4.5.2 Cross-sectional Analysis 91

4.5.3 Cross Hatch Test 93
4.5.4 Effect of Cu Bath Concentration on Electroless Cu Deposition Mechanism 93
4.5.5 Conclusion 96

4.6 Electroless Cu Deposition on Through Silicon Via (TSV) 96
4.6.1 Cross-sectional Analysis 97
4.6.2 Conclusion 99

CHAPTER 5 CONCLUSION AND FUTURE WORKS 101
5.1 Conclusions 101
5.2 Future Works 102

REFERENCES 103

LIST OF PUBLICATIONS 111

LIST OF TABLES

TABLE NO.	TITLE	PAGE
Table 2.1	Electrochemical reaction for electroless Cu deposition process	26
Table 2.2	Standard Redox Potential at 25° C	28
Table 3.1	Experimental Procedures	38
Table 3.2	Parameters for surface activation process	45
Table 3.3	Variation of parameters observed in pH bath and temperature effect	46
Table 3.4	Ratio of Cu to the reducing agent (formaldehyde)	47
Table 3.5	Electroless Cu Deposition Procedures	48
Table 3.6	Classification of adhesive test results (ASTM D3359)	49
Table 4.1	Optimised parameters selected for electroless Cu deposition on TSV	97

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
Figure 1.1	The packaging technology evolution	2
Figure 1.2	Electronic device that use TSV technology: (a) High bandwidth memory (HBM), and (b) HBM schematic diagram showing interconnection of DRAM using TSV and microbump	3
Figure 2.1	a) TSV, b) wire bonding, c) flip chip, and d) simplified TSV structure	10
Figure 2.2	Application for TSV	11
Figure 2.3	Via first approach in the fabrication of TSV	13
Figure 2.4	Via last approach in the fabrication of TSV	13
Figure 2.5	Bosch process used in DRIE process for TSV fabrication	15
Figure 2.6	FIB for TSV Fabrication; a) Deposition process, and b) FESEM of TSV produced	15
Figure 2.7	Types of via deposition process; a) lining, b) full lining, and c) full lining with stud formation	17
Figure 2.8	Types of profile evolution during Cu filling by electrodeposition: (a) subconformal deposition, (b) conformal deposition, (c) superfilling	19
Figure 2.9	Via filling defects. (a) Voids at the bottom of the via and (b) necking of the via	20
Figure 2.10	The schematic diagram of electrochemical reaction for electroless Cu deposition on catalyst surface.	27
Figure 2.11	Schematic diagram on surface wettability depends on the contact angle; a) hydrophilic surface and b) hydrophobic surface	31
Figure 2.12	Variation of surface roughness and contact angle via the generalised function	32
Figure 2.13	Effect of pH and temperature for EDTA and tartare bath	33
Figure 2.14	The effect of pH on a) the plating rate, and b) the surface morphology	34

Figure 3.1	Flowchart of the Research Work	39
Figure 3.2	Si wafer sample, b) the cut sample for Cu deposition process, and c) surface morphology of Si wafer	39
Figure 3.3	Nd:YAG laser for TSV fabrication; a) schematic diagram, b) surface morphology, and c) cross-sectional images of TSV	41
Figure 3.4	Schematic diagram illustrating the whole processes of electroless Cu deposition on Si wafer	42
Figure 3.5	Experimental setup of electroless Cu deposition process	44
Figure 4.1	FESEM micrograph of the Si substrates directly after the etching process, at different etching concentrations and times; (a) without etching, (b) etching for 1 minutes in 25% volume of HF solution, (c) etching for 5 minutes in 25% volume of HF solution, (d) etching for 1 minutes in 50% volume of HF solution, and (e) etching for 5 minutes in 50% volume of HF solution	55
Figure 4.2	FESEM micrograph of electroless Cu plated samples, with various etching concentrations and times; (a) without etching, (b) etching for 1 minutes in 25% volume of HF solution, (c) etching for 5 minutes in 25% volume of of HF solution, (d) etching for 1 minutes in 50% volume of HF solution, and (e) etching for 5 minutes in 50% volume of HF solution	56
Figure 4.3	Cross sections of the Si substrates directly after the etching process, at different etching concentrations and times; (a) without etching, (b) etching for 1 minutes in 25% volume of HF solution, (c) etching for 5 minutes in 25% volume of of HF solution, (d) etching for 1 minutes in 50% volume of HF solution, and (e) etching for 5 minutes in 50% volume of HF solution	58
Figure 4.4	FESEM micrograph of cross sections of electroless Cu plated samples, at different etching concentrations and times; (a) without etching, (b) etching for 1 minutes in 25% volume of HF solution, (c) etching for 5 minutes in 25% volume of HF solution, (d) etching for 1 minutes in 50% volume of HF solution, and (e) etching for 5 minutes in 50% volume of HF solution	60

Figure 4.5	EDX mapping for the cross-sectional morphologies of electroless Cu plated samples at different etching times; (a) without etching, (b) the EDX mapping for Figure 4.5(a); (c) etching for 1 minute, (d) the EDX mapping for Figure 4.5(c); (e) etching for 5 minutes, and (f) the EDX mapping for Figure 4.5(e)	61
Figure 4.6	Energy dispersive X-ray spectroscopy (EDX) line scanning for the cross-sectional morphology of 5 minutes-etched electroless Cu deposit sample	62
Figure 4.7	Plots of average Cu thickness (µm) vs etching time (min) for Si substrate etched in 25% and 50% volume of HF solution	63
Figure 4.8	Photograph images of Cu deposited samples after cross hatch test, with 10 minutes of electroless deposition time with different etching concentration; (a) 25% vol. of HF solution, and (b) 50% vol. of HF solution.	64
Figure 4.9	Schematic diagram of the Cu deposition mechanism of the etched samples	65
Figure 4.10	Photograph images of electroless Cu deposited samples, with different activation process, (a) single step process with 10 and 20 minutes of electroless deposition time, and (b) double step process with 10 and 20 minutes of electroless deposition time	68
Figure 4.11	SEM micrograph of electroless Cu deposited samples and chemical composition of Cu deposits for activation using; (a) single step process at 10 minutes of electroless deposition time, (b) single step process at 20 minutes of electroless deposition time, (c) double step process at 10 minutes of electroless deposition time, and (d) double step process at 20 minutes of electroless deposition time	70
Figure 4.12	Cross section of electroless Cu deposited samples, with different activation process, (a) single step process with 20 minutes of electroless deposition time, and (b) double step process with 20 minutes of electroless deposition time	72
Figure 4.13	Schematic diagram of the growth mechanism using single step activation process	73
Figure 4.14	Schematic diagram of the growth mechanism using double step activation process	74
Figure 4.15	Photograph images of electroless Cu deposited samples, with various electroless deposition temperature and time	76
Figure 4.16	Photograph images of electroless Cu deposited samples, with various electroless deposition pH and time. T = 70ºC	78

Figure 4.17 SEM micrograph of electroless Cu deposited samples at pH 11.5 and temperature of 70°C, with different electroless deposition time; (a) 5 minutes, (b) 10 minutes, (c) 20 minutes, and (d) 30 minutes 80

Figure 4.18 SEM micrograph of cross section of electroless Cu deposited samples at pH 11.5 and temperature of 70°C, with different electroless deposition time; (a) 5 minutes, (b) 10 minutes, (c) 20 minutes, and (d) 30 minutes 81

Figure 4.19 Energy dispersive X-ray spectroscopy (EDX) line scanning for the cross-sectional morphology of electroless Cu deposited samples at pH 11.5 and temperature of 70°C, with different electroless deposition time; (a) 5 minutes and (b) 10 minutes 82

Figure 4.20 Energy dispersive X-ray spectroscopy (EDX) line scanning for the cross-sectional morphology of electroless Cu deposited samples at pH 11.5 and temperature of 70°C, with different electroless deposition time; (a) 20 minutes and (b) 30 minutes. 83

Figure 4.21 Schematic diagram of Cu nucleation and growth on Si substrate surface during electroless deposition process 84

Figure 4.22 Photograph and optical images of Cu deposited samples after cross hatch test, with 30 minutes of electroless deposition time and pH of 11.5 and with different deposition temperature; (a) 50ºC, (b) 60ºC, and (c) 70ºC 86

Figure 4.23 Photograph and optical images of Cu deposited samples after cross hatch test, with 30 minutes of electroless deposition time and temperature of 70°C, and with different pH; (a) 10.5, (b) 11.0, (c) 11.5 and (d) 12.0 87

Figure 4.24 SEM micrograph of electroless Cu deposited samples on Si wafer, with various molar ratio of $CuSO_4$ to formaldehyde and deposition time; (a) 1:2 for 5 minutes, (b) 1:2 for 20 minutes, (c) 1:3 for 5 minutes, (d) 1:3 for 20 minutes, (e) 1:4 for 5 minutes, (f) 1:4 for 20 minutes, (g) 1:5 for 5 minutes, and (h) 1:5 for 20 minutes 89

Figure 4.25 Plots of weight gain (g) vs electroless Cu deposition time (minute) on Si wafer at various molar ratio of $CuSO_4$ to formaldehyde 90

Figure 4.26 Plots of deposition rate (g/min) vs electroless Cu deposition time (minute) on Si wafer for various molar ratio of $CuSO_4$ to formaldehyde 91

Figure 4.27	SEM images of cross-sectional samples of electroless Cu deposited on Si wafer at 20 minutes of electroless deposition time for various ratio concentrations ($CuSO_4$: formaldehyde); (a) 1:2, (b) 1:3, (c) 1:4 and (d) 1:5	92
Figure 4.28	EDX elemental mapping of cross-sectional samples of electroless Cu deposited on Si wafer at 20 minutes of electroless deposition time for various molar ratio of $CuSO_4$ to formaldehyde; (a) 1:2, (b) 1:3, (c) 1:4 and (d) 1:5.	92
Figure 4.29	Photograph and optical microscope images of Cu deposited on Si samples after cross hatch test, with 20 minutes of electroless deposition time and various molar ratio concentrations ($CuSO_4$: Formaldehyde); (a) 1:2, (b) 1:3, (c) 1:4 and (d) 1:5	94
Figure 4.30	Schematic diagram of electroless Cu deposition process mechanism with different molar ratio concentration ($CuSO_4$:Formaldehyde); (a) 1:2, and (b) 1:x with $x > 2$	95
Figure 4.31	SEM micrograph of cross sections of electroless Cu deposited on TSV samples with various electroless deposition time, a) 3 hours, b) 4 hours, c) 5 hours, and d) 20 hours	98
Figure 4.32	Plots of a) Cu thickness (μm) vs deposition time (hr) and b) deposition rate (μm/hr) vs deposition time (hr) for electroless Cu deposition on TSV at the substrate surface and the inner TSV	100

LIST OF ABBREVIATIONS

Si	-	silicon
IC	-	integrated circuit
2D	-	two-dimensional
3D	-	three-dimensional
TSV	-	through silicon via
TGV	-	through glass via
Cu	-	copper
DRAM	-	dynamic random access memory
HBM	-	high bandwidth memory
RAM	-	random access memory
CVD	-	chemical vapor deposition
Pd-NPs	-	palladium nanoparticles
VPSEM	-	variable pressure scanning electron microscopy
EDX	-	energy dispersive X-ray
MEMS	-	micro-electro-mechanical systems
CIS	-	contact image sensor
DRIE	-	deep reactive ion etch
FIB	-	focused ion beam
EDTA	-	ethylenediaminetetraacetic
Nd:YAG	-	neodymium-doped yttrium aluminium garnet
PECVD	-	plasma-enhanced chemical vapor deposition
HF	-	hydrofluoric acid
RDL	-	redistribution layer
CMP	-	chemical and mechanical polishing
PVD	-	physical vapor deposition
W	-	tungsten
SSEP	-	seed step-coverage enhancement process
Sn	-	tin
Pd	-	palladium

LIST OF SYMBOLS

°C	-	degree celsius
g	-	gram
μm	-	micrometer
mL	-	mililiter
nm	-	nanometer
w	-	weight
T	-	thickness
t	-	deposition time

CHAPTER 1

INTRODUCTION

1.1 Introduction

An integrated circuit (IC) is a set of an electronic circuit that comprising numerous functional elements on one piece of semiconductor material such as silicon (Si). All the components in IC are integrated from a single piece of Si, compared to a discrete circuit in which the components are assembled together from different types of materials. Semiconductor integration technology has instigated a technical revolution in human history. Over the past three decades, two-dimensional (2D) semiconductor integration technology has spurred in various fields of electronics-related industries such as electronics analysis, optoelectronics, bioelectronics, computer systems, medical systems, satellite systems, submarine systems, and many others (Tan *et al*, 2017 and Akinwande *et al.*, 2014).

However, inflated demands for a higher density integration, superior performance, miniaturisation size features with a cheaper cost of the modern electronic devices are recently increased (Maluf and William, 2004, Yang, 2018, and Lah *et al.*, 2018). Traditional 2D semiconductor integration approaches have been shown to reach its practical limits to fulfil these demands (Iwai *et al.*, 2005). Advanced three-dimensional (3D) packaging technologies are undoubtedly gaining momentum and become a solution for significant advantages in performance functionality.

A three-dimensional integrated circuit (3D IC) is a chip consists of active electronic components that stacked on two or more layers that are integrated both horizontally and vertically forming a single circuit (Shen and Chen, 2017). In contrast with 2D integrated circuit (2D IC), the chips or wafers are stacked vertically with the shortest interconnection, so that they behave as a single device but with improved performance. Figure 1.1 shows the semiconductor integration technology evolution

through the years. The size, speed and capacity of the chips from solid state discrete transistors have progressed enormously and transform into 2D IC and starting the 20th centuries, the trend continues to upgrade into 3D IC.

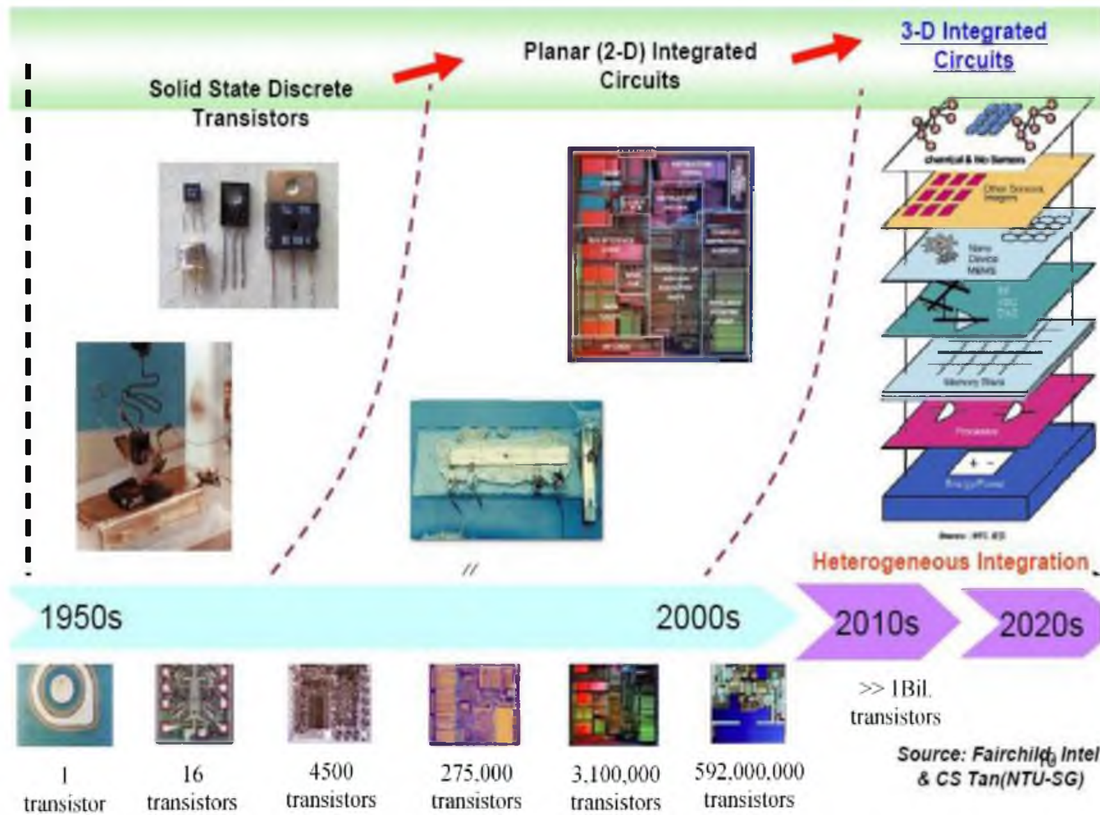
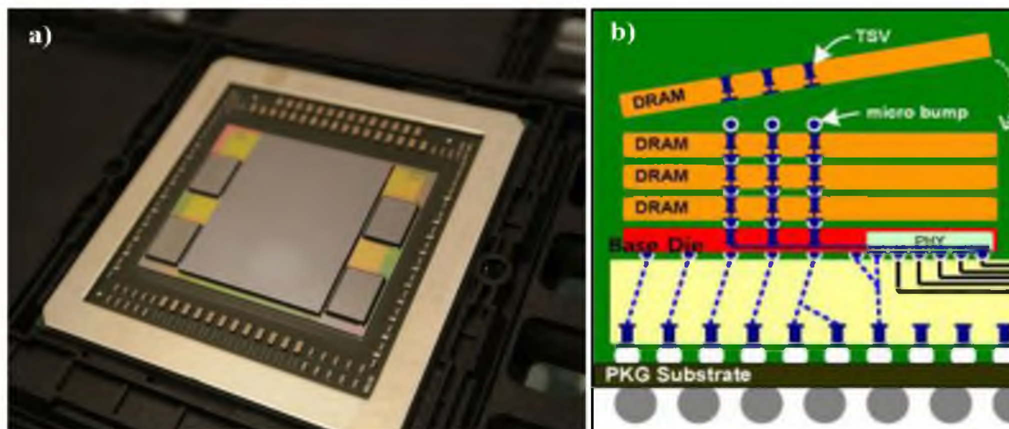


Figure 1.1: The packaging technology evolution

Several approaches for short distance interconnections between stacked chips have been developed through the years by using different techniques such as wire-bonding, edge connect, capacitive or inductive coupling method, and direct contact using through silicon via (TSV) (Law *et al.*, 2012, Makoto M, 2009, and Neugebauer *et al.*, 1987). TSV is a structure through entire Si substrate that provides a vertical area-array connection between the devices and addresses many of the limitations by other chip-stacking methods (Pancholi A., 2013). Single crystal Si is commonly used as a substrate material for TSV, however other material such as glass also has properties that make it as an intriguing material for through substrate via application, known as through glass via (TGV) (Takahashi *et al.*, 2013 and Sukumaran *et al.*,

2010). TSV has numerous benefits that are needed in 3D packaging technology including high density and heterogeneous integration (reduction in packaging volume), high performance, high signal speed, enhanced power consumption and overall cost reduction (Knikerbocker *et al.*, 2006). Copper (Cu) is most commonly used as a filling material for TSV due to its high electrical conductivity, good resistance against electromigration and stress migration, cost effective and good compatibility with integrated circuit modules (Wolf *et al.*, 2008, and Shi *et al.*, 2013). The application of Cu as a conductive material is well developed and established since decades.

One of the great examples of electronic devices that use TSV technology is high bandwidth memory (HBM). Figure 1.2.a is AMD Fiji chip own by a well-known semiconductor manufacturer, Advanced Micro Devices (AMD) that used HBM technology. HBM is a high-performance random access memory (RAM) interface for 3D-stacked dynamic random access memory (DRAM) from AMD and Hynix. HBM has the ability to achieve higher bandwidth while using less power by stacking all the DRAM dies including the base die, interconnected by TSV and microbumps (Figure 1.2.b). The technology is proven has greater performance through its precedent, a wire-bond and flip-chip bond connected RAMs.



Source: https://en.wikipedia.org/wiki/High_Bandwidth_Memory and http://pc.watch.impress.co.jp/img/pcw/docs/646/660/html/09.jpg.html

Figure 1.2: Electronic device that use TSV technology: (a) High bandwidth memory (HBM), and (b) HBM schematic diagram showing interconnection of DRAM using TSV and microbump

1.2 Research Background

In electronic engineering, TSV is a vertical electrical connection that passes completely through a Si wafer or die by vias. It is a high-performance interconnection technique used as an alternative to wire-bond and flip chips techniques. TSV is a high-performance technique used to create 3D IC that provides shortest interconnect length among chips that will reduce interconnect delay and increase speed, thus improve the circuit functionality and performance (Pangracious *et al.*, 2015, Salah *et al.*, 2010 and Salah *et al.*, 2014). Moreover, by the TSV implementation, the stacked dies or wafers can behave as a single device with complex and multi-chip systems with highest density connections and achieved performance improvement at reduced power (Knickerbocker *et al.*, 2008 and Lee *et al.*, 2011).

Via filling process has been addressed as one of the core and critical procedure during TSV manufacturing. The process to metalise via filling which is in a nanoscale via is very challenging, as the TSV diameters can range from a few microns to >100 µm in diameter and from <10 µm to a few hundreds of microns in depth, depends on its application (Malta *et al.*, 2009). The desired properties of the filling include void-free, low resistivity, high reliability and good thermal performance (Spiesshoefer *et al.*, 2005). Recently, there are a few different techniques used for via filling, such as chemical vapor deposition (CVD) and electroplating as the most commonly applied in industrial.

CVD is a chemical process which is often used in semiconductor industry to produce a thin film. CVD uses chemical concentration and temperature gradients as the main driving force causing transfer of metal to the surface. In this process, a source of metal is heated to promote vaporisation and the vaporised atoms are transported and deposited on the surface where metallisation is desired (Lidong Wang, 2005). The CVD process is well suited for small size vias (3µm to 5 µm) with high aspect ratios up to 20, but are limited in the deposited layer thickness and high-temperature process (Ramm *et al.*, 2008).

Electroplating or electrodeposition is a well-studied method and currently is the most commonly used for via filling technique as reported by Kobayashi *et al.* (2001), Ko and Chen (2010), Shi *et al.* (2013), Fang *et al.* (2011) and Luhn *et al.* (2008). In this process, a deposition of a thin via liner or seed layer is necessary after the via formation process. The substrate is placed in an electrolytic plating bath and electrical current is applied to reduce metal ions on the substrate and create a thicker layer of metal in the vias. However, Cu electroplating process becoming more difficult to achieve a nanoscale level for deep TSV with high aspect ratios, and it is very challenging to obtain layers with good dimensional and electrical characteristic from top to the bottom of the via and avoid excess metal developed locally (Horváth *et al.*, 2014).

Recently the electroless deposition of Cu on Si substrate has emerged as an effective solution and promising technique for the TSV filling process. On the contrary from electroplating, electroless deposition relies on chemical interactions on the surface without the need of an external electrical field. The metal ions contained in a plating solution is reduced onto the catalytic surface of the substrate by the addition of a reducing agent into the bath (Srividov *et al.*, 2003).

Electroless deposition possesses several advantages compared to the electroplating process. Since electroless deposition is based on a chemical reaction instead of electrical process, the rate of Cu deposition is uniform in thickness all over the surface with negligible variation of thickness. It gives complete coverage on any shape and size, including on the inner surface of via with high aspect ratio such as TSV. Furthermore, electroless deposition eliminated the need of a power supplies that are necessary for electroplating process. High-quality aspects of Cu deposits obtained from electroless Cu deposition process also becomes the significant advantages and provide a motivation to pursue research to develop this technique for TSV via filling processes.

1.3 Problem Statement

Early work in 1995, Shacham-Diamand *et al.* (1995) had conceded that electroless Cu deposition process can produce high-quality Cu filling of high aspect ratio via, even though there were still many challenges in the development of the technology during that time. The researches continued by Kim *et al.* (2015) where he performed the formation of seed layer in TSV by using electroless Cu deposition and continued with electroplating to fill the via. Meanwhile, Inoue *et al.* (2012) had formed a conformal diffusion barrier and seed layers by electroless deposition using palladium nanoparticles (Pd-NPs) catalyst in high aspect ratio TSVs. Later in 2013, he continued the study with feasibility of a TSV filling process using electroless deposition of Cu on atomic layer deposition of ruthenium (Inoue *et al.*, 2013).

Even the advantages of the electroless deposition process are well known by the researchers, however, the process has been applied in the TSV that focuses on the pre-deposition treatment of the surfaces which is the deposition of barrier layer or seed layer only. This is because the maximum thickness of electroless Cu deposition coating is limited to approximately 25µm (Deckert CA, 1994). In fact, to achieve its maximum thickness, the deposition rate will decrease with deposition time which resulting in slower production rate. Therefore, the electroplating process is usually chosen as the only way to achieve greater thickness for the via size larger than 50µm in diameter. However, considering that the TSV diameter will continuously decrease to less than 50µm as this application is suitable for small electronic devices, filling TSV by electroless deposition will not be an issue, because such process can be tuned to be very conformal.

To date, only one research had attempted to study a fully back-end TSV process by Cu electroless plating on activated TiN surfaces for 3D smart sensor systems, which was by Santagata et al. (2013). The result proved that the electroless deposition process of Cu in the via has uniform thickness. The uniform deposition layer is very important to avoid the formation of void in the filling. However, the work done in the research showed that the electroless process conducted on the TSV was unable to completely filled the vias. The maximum thickness of uniform Cu deposited by

electroless process in their study was only 0.6μm. Even the electroless Cu deposited sample was not completely filled with Cu, its electrical resistance performance was comparable with the electrodeposited Cu sample. This indicates that the electroless deposition process is possible to replace the electrodeposition process for Cu filling of TSV. The outcome from this study may contribute to the growing area of electroless Cu deposition on Si wafer for TSV application.

In this research, some preliminary experiments were conducted to fix the controlled parameters starting from the pre-treatment process (etching and surface activation process) as well as the electroless deposition parameters (pH, temperatures and bath concentration). These preliminary experiments were conducted on flat surface of Si wafer, rather than directly on the TSV sample since the electroless deposition process is expected to form a very conformal deposit on the substrate surface, regardless the form of substrate surface. On the second phase, electroless deposition process with a fixed controlled parameter gained from the preliminary experiments were conducted on TSV as the substrate.

1.4 Objectives of the Research

The objectives of this research are;

a) To identify the pre-treatment processes (etching process and surface activation process) prior electroless Cu deposition on Si wafer;

b) To fix the controlled parameters for electroless Cu bath operation on Si wafer in terms of temperature, pH and concentration;

c) To deposit Cu in the vias by using electroless Cu deposition process based on identified pre-treatment and fixed controlled parameters obtained.

1.5 Scopes of the Research

The scopes of this project consist of;

a) Optimising the plating parameters of electroless Cu deposition on flat surface of Si wafer;

   i) Pre-treatment process; etching and surface activation process.

   ii) Electroless Cu deposition; pH, temperature, and concentration of Cu and the reducing agent.

b) Fabricate the vias with 50μm in diameter on Si wafer by using Nd:YAG laser process;

c) Deposition of Cu in the vias;

d) Characterise the deposited Cu on Si wafer using variable pressure scanning electron microscopy (VPSEM), energy dispersive X-ray (EDX) and optical microscopy; and

e) Test the adhesion performance of deposited Cu through cross hatch test (ASTM D3359).

1.6 Importance of the Research

A 3D integration technology is seen as necessary to maintain the integrated circuit performance on the path described by Moore's law (Yu CH, 2006). Despite the potential benefits it had associated, the incorporation of TSVs poses significant challenges to the performance and reliability. Therefore, the development of an alternate technology to design and construct TSV for microelectronic systems as 3D devices has become essential.

REFERENCES

Akinwande, D., Petrone, N., & Hone, J. (2014). Two-dimensional flexible nanoelectronics. *Nature communications*, *5*, 5678.

Anik, T., Touhami, M. E., Himm, K., Schireen, S., Belkhmima, R. A., Abouchane, M., & Cissé, M. (2012). Influence of pH solution on electroless copper plating using sodium hypophosphite as reducing agent. *Int. J. Electrochem. Sci*, *7*(3), 2009-2018.

ASTM D3359 (Measuring Adhesion by Tape Test) Standard.

Bae, J. W., Lim, J. W., Mimura, K., & Isshiki, M. (2004). Agglomeration of copper thin film in Cu/Ta/Si structure. *Materials Transactions*, *45*(3), 877-879.

Bindra, P., & White, J. R. (1990). Fundamental aspects of electroless copper plating. *Electroless Plating Fundamentals & Applications (Jan. 1990) pp*, 289-375.

Brenner, A., & Riddell, G. E. (1998). Nickel plating on steel by chemical reduction. *Plating and surface finishing*, *85*(8), 54-55.

Brogan, L., Mayer, S. T., Thorum, M., Richardson, J., Porter, D. W., & Fu, H. (2017). *U.S. Patent No. 9,689,083*. Washington, DC: U.S. Patent and Trademark Office.

C.F. Coombs (1988), *Printed Circuit Handbook*, 3rd ed., McGraw-Hill, New York, pp. 12.1 – 45 and 13.1 – 18.

Craigie, C.J.D., Sheehan, T., Johnson, V.N., Burkett, S.L., Moll, A.J. and Knowlton, W.B. (2002). Polymer thickness effects on Bosch etch profiles. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, *20*(6), pp.2229-2232.

Cui, X., Hutt, D.A. and Conway, P.P. (2012). Evolution of microstructure and electrical conductivity of electroless copper deposits on a glass substrate. *Thin Solid Films*, *520*(19), pp.6095-6099.

Daryaei, E., Tabar, M.R.R. and Moshfegh, A.Z. (2013). Surface roughness analysis of hydrophilic SiO2/TiO2/glass nano bilayers by the level crossing approach. *Physica A: Statistical Mechanics and its Applications*, *392*(9), pp.2175-2181.

Davis, J.R. ed. (2001). Copper and copper alloys. *ASM international*, pp 140.

Deckert, C.A. (1994). Electroless Copper Plating. *ASM Handbook*, *5*, pp.311-322.

Fang, C., Le Corre, A., & Yon, D. (2011). Copper electroplating into deep microvias for the “SiP” application. *Microelectronic Engineering*, *88*(5), 749-753.

Feng, Y., & Burkett, S. L. (2015). Fabrication and electrical performance of through silicon via interconnects filled with a copper/carbon nanotube composite. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, *33*(2), 022004

Gadkari, P.R., Warren, A.P., Todi, R.M., Petrova, R.V. and Coffey, K.R. (2005). Comparison of the agglomeration behavior of thin metallic films on Si O 2. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, *23*(4), pp.1152-1161.

Garrou, P., Bower, C., & Ramm, P. (Eds.). (2011). *Handbook of 3D Integration, Volume 1: Technology and Applications of 3D Integrated Circuits*. John Wiley & Sons.

Grdanovska, S. (2015). Characterization of Radiation Damage to a Novel Photonic Crystal Sensor (Doctoral dissertation).

Gupta, T. (2010). *Copper interconnect technology*. Springer Science & Business Media.

Hanna F, Hamid ZA, Aal AA. (2001) Direct electroplating on printed circuit boards. *Metal Finishing*. 99(4):51-4.

Hasegawa M. (2007) Fundamental analysis of electrochemical copper deposition for fabrication of submicrometer interconnects (Doctoral dissertation, Thesis, Waseda University, Jepang: 18 pH= 5 pH= 9).

Hidemi Nawafune, Shingo Higuchi, Kensuke Akamatsu and Ei Uchida (2003). Improvement of Via-Filling in Neutral Electroless Copper Plating for ULSI Metallization. *Journal of the Surface Finishing Society of Japan*. 54 (10): 683-688.

Horváth B, Kawakita J, Chikyow T. (2014) Through silicon via filling methods with metal/polymer composite for three-dimensional LSI. *Japanese Journal of Applied Physics*. 12;53(6S):06JH01.

Hu M, Su YF, Wu MZ. (2009) Influences of pretreatment solution concentrations on copper-doped SiC particles made through electroless plating technique. *InAdvanced Materials Research* Trans Tech Publications.79, pp. 1739-1742.

Huang, T., (2017). Studies of interfacial adhesion and copper plating chemistry for metallization of through-package-vias in glass interposers (Doctoral dissertation, Georgia Institute of Technology).

Inoue, F., Philipsen, H., Radisic, A., Armini, S., Civale, Y., Leunissen, P., Kondo, M., Webb, E. and Shingubara, S. (2013). Electroless Cu deposition on atomic layer deposited Ru as novel seed formation process in through-Si vias. *Electrochimica Acta*, *100*, pp.203-211.

Inoue, F., Shimizu, T., Miyake, H., Arima, R., Ito, T., Seki, H., Shinozaki, Y., Yamamoto, T. and Shingubara, S. (2012). Adsorption of Pd nanoparticles catalyst in high aspect ratio through-Si vias for electroless deposition. *Electrochimica Acta*, *82*, pp.372-377.

Iwai, Hiroshi & Kakushima, Kuniyuki & Wong, Hei. (2005). Challenges for future semiconductor manufacturing. International Journal of High Speed Electronics and Systems. XX. 1-39. 10.1142/9789812773081_0004.

Jaehui Ahn, Hong-Yeol Kim, Hyo-Chol Koo, Jae Jeong Kim, Jihyun Kim, (2009) Characterization and Cu electroless plating of laser-drilled through-wafer via-holes in GaN/Al_2O_3, *Thin Solid Films* 517. 3841–3843.

Jin S, Lee D, Lee WY, Lee S, Lee MH. (2015) Seed step-coverage enhancement process for a high-aspect-ratio through-silicon via using a pyrophosphate solution. *Metals and Materials International*. 21(4):775-9.

Joo S, Baldwin DF. (2009) Adhesion mechanisms of nanoparticle silver to substrate materials: identification. *Nanotechnology*. 21(5):055204.

Kaushik, B. K., Kumar, V. R., Majumder, M. K., & Alam, A. (2016). *Through Silicon Vias: Materials, Models, Design, and Performance*. Crc Press.

Kim B, Ritzdorf T. (2006) High aspect ratio via filling with copper for 3D integration. *Semiconductor Equipment and Materials International*.

Kim, B., Sharbono, C., Ritzdorf, T., & Schmauch, D. (2006). Factors affecting copper filling process within high aspect ratio deep vias for 3D chip stacking. In *56th Electronic Components and Technology Conference 2006* (pp. 6-pp). IEEE.

Kim, K. H., Lim, T., Park, K. J., Koo, H. C., Kim, M. J., & Kim, J. J. (2015). Investigation of Cu growth phenomena on Ru substrate during electroless deposition using hydrazine as a reducing agent. *Electrochimica Acta*, *151*, 249-255.

Knickerbocker, J.U., Andry, P.S., Dang, B., Horton, R.R., Interrante, M.J., Patel, C.S., Polastre, R.J., Sakuma, K., Sirdeshmukh, R., Sprogis, E.J. and Sri-Jayantha, S.M. (2008). Three-dimensional silicon integration. *IBM Journal of Research and Development*, *52*(6), pp.553-569.

Knickerbocker, J.U., Patel, C.S., Andry, P.S., Tsang, C.K., Buchwalter, L.P., Sprogis, E.J., Gan, H., Horton, R.R., Polastre, R.J., Wright, S.L. and Cotte, J.M. (2006). 3-D silicon integration and silicon packaging technology using silicon through-vias. *IEEE Journal of Solid-State Circuits*, *41*(8), pp.1718-1725.

Ko, C. T., & Chen, K. N. (2010). Wafer-level bonding/stacking technology for 3D integration. *Microelectronics reliability*, *50*(4), 481-488.

Kobayashi, T., Kawasaki, J., Mihara, K., & Honma, H. (2001). Via-filling using electroplating for build-up PCBs. *Electrochimica Acta*, *47*(1-2), 85-89.

Koechner, W. (2013). *Solid-state laser engineering* (Vol. 1). Springer.

Kumar, V., Bhat, K.N. and Nipun Sharma, N. (2015). Surface modification of textured silicon and its wetting behaviour. *Journal of Adhesion Science and Technology*, *29*(4), pp.308-318.

Lah NA, Zubir MN, Mahendran A, Samykano L. (2018) Engineered Nanomaterial in Electronics and Electrical Industries. *InHandbook of Nanomaterials for Industrial Applications*. Elsevier. pp. 324-364.

Lahiri, A., Pulletikurthi, G. and Endres, F. (2019). A Review on the Electroless Deposition of Functional Materials in Ionic Liquids for Batteries and Catalysis. *Frontiers in chemistry*, *7*.

Lau J, Tzeng P, Lee C, Zhan C, Li M, Cline J, Saito K, Hsin Y, Chang P, Chang Y, Chen J. (2014) Redistribution layers (RDLs) for 2.5 D/3D IC integration. *Journal of Microelectronics and Electronic Packaging*. 11(1):16-24.

Laviron C, Dunne B, Lapras V, Galbiati P, Henry D, Toia F, Moreau S, Anciant R, Brunet-Manquat C, Sillon N. (2009) Via first approach optimisation for through silicon via applications. *InElectronic Components and Technology Conference, IEEE*. pp. 14-19

Law, K.Y. (2014). Definitions for hydrophilicity, hydrophobicity, and superhydrophobicity: getting the basics right.

Law, O. M., Wu, K. H., & Yeh, W. C. (2012). *U.S. Patent No. 8,264,067*. Washington, DC: U.S. Patent and Trademark Office.

Lee, K. W., Noriki, A., Kiyoyama, K., Fukushima, T., Tanaka, T., & Koyanagi, M. (2010). Three-dimensional hybrid integration technology of CMOS, MEMS, and photonics circuits for optoelectronic heterogeneous integrated systems. *IEEE Transactions on Electron Devices*, *58*(3), 748-757.

Levy-Clement, C., Lagoubi, A., Tenne, R. and Neumann-Spallart, M. (1992). Photoelectrochemical etching of silicon. *Electrochimica acta*, *37*(5), pp.877-888.

Li LS, Li XR, Zhao WX, Ma Q, Lu XB, Wang ZL (2013) A study of low temperature and low stress electroless copper plating bath. *Int. J. Electrochem. Sci*. 8(4).

Lidong Wang (2005). *Chemical Vapor Deposition of Thin Films for ULSI Interconnect Metallization.* Doctor of Philosophy. Louisiana State University, United State.

Lühn, O., Van Hoof, C., Ruythooren, W., & Celis, J. P. (2008). Barrier and seed layer coverage in 3D structures with different aspect ratios using sputtering and ALD processes. *Microelectronic Engineering*, *85*(10), 1947-1951.

Makoto Motoyoshi. (2009) Through Silicon-Via (TSV). *Proceeding of IEEE.* 97 (1): 43-48.

Malta D, Gregory C, Temple D, Knutson T, Wang C, Richardson T, Zhang Y, Rhoades R. (2010) Integrated process for defect-free copper plating and chemical-mechanical polishing of through-silicon vias for 3D interconnects. *InElectronic Components and Technology Conference (ECTC)*, 2010 Proceedings 60th IEEE. pp. 1769-1775.

Malta, D., Gregory, C., Temple, D., Wang, C., Richardson, T., & Zhang, Y. (2009). Optimization of chemistry and process parameters for void-free copper electroplating of high aspect ratio through-silicon vias for 3D integration. In *2009 59th Electronic Components and Technology Conference* (pp. 1301-1306). IEEE.

Maluf, N., & Williams, K. (2004). *Introduction to microelectromechanical systems engineering*. Artech House.

Masuko N., Ōsaka T. and Itō Y. (1996). Electrochemical Technology: Innovation and New Developments. Kodansha, 1996.

Matijevic, E., Poskanzer, A.M. and Zuman, P., (1975). Characterization of the stannous chloride/Palladium chloride catalysts for electroless plating. *Plating and Surface Finishing*, *62*(10), pp.958-965.

Mattila TT, Paulasto-Kröckel M. (2011) Towards comprehensive reliability assessment of electronics by a combined loading approach. *Microelectronics Reliability*. 51(6):1077-91.

Mitsukura K, Makino T, Hatakeyama K, Rebibis KJ, Wang T, Capuz G, Duval F, Detalle M, Miller A, Beyne E. (2016) Packaging Material Evaluation for 2.5 D/3D TSV Application. *Transactions of The Japan Institute of Electronics Packaging*. 9:E16-011.

Moniruzzaman, M. and Roy, S. (2011). Effect of pH on electroless Ni-P coating of conductive and nonconductive materials. *International Journal of Automotive and Mechanical Engineering*, *4*, pp.481-489.

Nakahara, S. (1988). Microscopic mechanism of the hydrogen effect on the ductility of electroless copper. *Acta Metallurgica*, *36*(7), pp.1669-1681.

Neugebauer C, Carlson R. (1987) Comparison of wafer scale integration with VLSI packaging approaches. *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*. 10(2):184-9.

Pancholi A. (2013) 3-Dimensional Integrated Circuits. International Journal of Scientific & Engineering Research. 4(6).

Pangracious V, Marrakchi Z, Mehrez H. (2015) Three-dimensional Integration: a more than Moore technology. *InThree-dimensional design methodologies for tree-based FPGA architecture* (pp. 13-41). Springer, Cham.

Pavlidis VF, Savidis I, Friedman EG. (2017) Three-dimensional integrated circuit design. *Newnes*.

Prušinskas, K., Norkus, E., Stalnionienė, I., & Stankevičienė, I. (2013). Application of ultrasound for the systems of electroless copper plating: Influence of ultrasonic irradiation on the plating rate and the surface of coatings. *Chemija*, *24*(1).

Ramm P, Wolf MJ, Klumpp A, Wieland R, Wunderle B, Michel B, Reichl H. (2008) Through silicon via technology—processes and reliability for wafer-level 3D system integration. *InElectronic Components and Technology Conference*, pp. 841-846. IEEE.

Salah K, El Rouby A, Ragai H, Ismail Y. (2010) 3D/TSV enabling technologies for SOC/NOC: Modeling and design challenges. *InMicroelectronics (ICM), 2010 International Conference* pp. 268-271. IEEE.

Salah K, Ismail Y, El-Rouby A. (2014) Arbitrary modeling of TSVs for 3D integrated circuits. *Springer*.

Santagata, F., Farriciello, C., Fiorentino, G., Van Zeijl, H. W., Silvestri, C., Zhang, G. Q., & Sarro, P. M. (2013). Fully back-end TSV process by Cu electro-less plating for 3D smart sensor systems. *Journal of Micromechanics and Microengineering*, *23*(5), 055014.

Sard, R. (1970). The nucleation, growth, and structure of electroless copper deposits. *Journal of The Electrochemical Society*, *117*(7), pp.864-870.

Sarkar, J. (2010). Sputtering materials for VLSI and thin film devices. William Andrew.

Shacham-Diamand Y, Dubin V, Angyal M. (1995) Electroless copper deposition for ULSI. *Thin Solid Films*. 262(1-2):93-103.

Shen WW, Chen KN. (2017) Three-dimensional integrated circuit (3D IC) key technology: through-silicon via (TSV). *Nanoscale research letters*. 12(1):56.

Shi S, Wang X, Xu C, Yuan J, Fang J, Liu S. (2013) Simulation and fabrication of two Cu TSV electroplating methods for wafer-level 3D integrated circuits packaging. Sensors and Actuators A: Physical. 203:52-61.

Spiesshoefer S, Rahman Z, Vangara G, Polamreddy S, Burkett S, Schaper L. (2005) Process integration for through-silicon vias. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films.* 23(4):824-9.

Sukumaran V, Chen Q, Liu F, Kumbhat N, Bandyopadhyay T, Chan H, Min S, Nopper C, Sundaram V, Tummala R. (2010) Through-package-via formation and metallization of glass interposers. *InElectronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*. pp. 557-563. IEEE.

Sun R, Yu G, Xie Z, Hu B, Zhang J, He X, Zhang X. (2015) Influence of hypophosphite on efficiency and coating qualities of electroless Ni-P deposits on magnesium alloy AZ91D. *Int. J. Electrochem. Sci*. 10:7893-904.

Sviridov, V. V., Gaevskaya, T. V., Stepanova, L. I., & Vorobyova, T. N. (2003). Electroless deposition and Electroplating of Metals.

Takahashi S, Horiuchi K, Tatsukoshi K, Ono M, Imajo N, Mobely T. (2013) Development of through glass via (TGV) formation technology using electrical discharging for 2.5/3D integrated packaging. *InElectronic Components and Technology Conference (ECTC),* 2013 IEEE 63rd. pp. 348-352. IEEE.

Tan C, Cao X, Wu XJ, He Q, Yang J, Zhang X, Chen J, Zhao W, Han S, Nam GH, Sindoro M. (2017) Recent advances in ultrathin two-dimensional nanomaterials. *Chemical reviews.* 117(9):6225-331.

Tilli M. (2015) Silicon wafers: preparation and properties. InHandbook of Silicon Based MEMS Materials and Technologies (Second Edition). pp. 86-103.

Trucks, G.W., Raghavachari, K., Higashi, G.S. and Chabal, Y.J., (1990). Mechanism of HF etching of silicon surfaces: A theoretical understanding of hydrogen passivation. *Physical Review Letters*, *65*(4), p.504.

Tsai TK, Chao CG. (2004) The growth morphology and crystallinity of electroless NiP deposition on silicon. *Applied surface science*. 233(1-4):180-90.

Tsui KY, Yau SK, Leung VC, Sun P, Shi DX. (2009) Parametric study of electroplating-based via-filling process for TSV applications. *InElectronic Packaging Technology & High Density Packaging, 2009*. pp. 23-27. IEEE.

Viljanto H. (2015). Reliability and Lifetime Assessment of Through-Silicon Vias Under Thermal Cycling.

Wang, G., Zhang M, Dong G, Jing X (2006) Effect of stabilizers on depositing rate and morphology of electroless Ni-Cu-P alloy, *Journal of Rare Earths*, 24 (Suppl.3), pp. 233-237.

Wolf MJ, Dretschkow T, Wunderle B, Jurgensen N, Engelmann G, Ehrmann O, Uhlig A, Michel B, Reichl H. (2008) High aspect ratio TSV copper filling with different seed layers. *InElectronic Components and Technology Conference,* 2008. pp. 563-570. IEEE.

Wurtz A. (1844) C.R. Hebd Seances Acad. Sci. 18. 702.

Yamagishi, K., Okamoto, N., Mitsumata, N., Fukumuro, N., Yae, S. and Matsuda, H., (2004). Reaction process of two-step catalysation pre-treatment for electroless plating on non-conducting substrates. *Transactions of the IMF*, *82*(3-4), pp.114-117.

Yang Y, Li F. (2018) Recent Advances in 3D Packaging for Medical Applications. *In2018 19th International Conference on Electronic Packaging Technology (ICEPT)*. pp. 1193-1197. IEEE.

Yu CH. (2006) The 3rd dimension-more life for Moore's Law. *InMicrosystems, Packaging, Assembly Conference Taiwan*. pp. 1-6. IEEE.

Zaveri J. (2011) *Electrical and fluidic interconnect design and technology for 3D ICS* (Doctoral dissertation, Georgia Institute of Technology).

LIST OF PUBLICATIONS

Indexed Conference Proceedings

1. Shahidin, S.A.M, Fadil, N.A, Zamri Yusop, M, Tamin, M. N, and Osman, S.A. (2018). Optimization of formaldehyde concentration on electroless copper deposition on alumina surface. *AIP Conference Proceedings 1963, 020014.* https://doi.org/10.1063/1.5036860 **(Indexed by SCOPUS)**

Indexed Journal

1. Shahidin, S.A.M, Fadil, N.A, Zamri Yusop, M, Tamin, M. N, and Osman, S.A. (2017). Effect of etching as pre-treatment for electroless copper plating on silicon wafer. *Jurnal Teknologi EISSN 2180-3722, 79:7, 61-69.* https://doi.org/10.11113/jt.v79.10640 **(Indexed by SCOPUS)**

Non- Indexed Conference Proceedings

1. Shahidin, S.A. Mior, and Fadil, N.A. (2016). Comprehensive review of different methods for via filling process in through silicon via (TSV) fabrication. *Journal of Advanced Review on Scientific Research ISSN (online): 2289-7887, 17:1, 8-12.*