SINGLE PHASE ASYMMETRICAL MULTILEVEL INVERTER TOPOLOGY WITH REDUCED DEVICE COUNT

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ABSTRACT

Multilevel Inverters (MLIs) are vital components for medium voltage and high-power applications. However, the number of components will increase with increased output voltage levels. It leads to high power losses. In this thesis, a new single-phase asymmetrical multilevel inverter topology used for medium and high voltage applications is proposed. The topology is capable of producing n-level output voltage with reduced device counts. It is achieved by arranging available switches and direct current (dc)-sources to obtain the maximum combinations of addition and subtraction of the input dc-sources. A comprehensive literature review has been carried out, and the proposed topology is compared with the topologies available in the literature. Comparison based on the number of switches utilized, the number of dc sources used, and the total number of devices is made. To verify the viability of the proposed topology, circuit models for 9-level, 25-level, and 67-level inverters are developed and simulated in Matlab-Simulink software first. Voltage and current waveforms and THD for resistive and inductive loads are obtained from the simulation model and validated with the experimental setup. Experimental results of the proposed inverter prototype for 9-level and 25-level output, developed in the laboratory, are presented. A low-frequency and high-frequency switching strategy for the proposed inverter topology are also presented in this work. Thermal modelling of the proposed topology is done in PLECS software, and detailed loss analysis for 9-level as well as 25-level topologies is carried out. The fundamental topology utilizes 9 switches with a total standing voltage (TSV) of 6.75 per unit while the 25-level topology structure has 12 switches with the TSV of 6.92 per unit only. Comparison with the other multilevel topologies shows that the proposed circuit requires fewer power switches and dc-sources to produce the same output levels. Due to the low switching frequency requirement, the proposed topology is applicable for high and medium voltage applications, resulting in lower switching losses.

ABSTRAK

Penyongsang berbilang aras (MLI) ialah komponen penting untuk aplikasi voltan sederhana dan berkuasa tinggi. Walau bagaimanapun, bilangan komponen akan meningkat dengan peningkatan tahap voltan keluaran. Ia akan menyebabkan kehilangan kuasa yang tinggi. Di dalam tesis ini, topologi penyongsang tidak simetri berbilang aras fasa tunggal untuk aplikasi voltan sederhana dan tinggi dicadangkan. Topologi ini berupaya menghasilkan n-aras voltan keluaran dengan penggunaan bilangan komponen yang rendah. Keupayaan ini dicapai dengan menyusun semua suis dan sumber kuasa arus terus (dc) yang ada untuk mendapatkan kombinasi maksimum penambahan dan penolakan sumber kuasa dc. Kajian literasi secara menyeluruh telah dijalankan dan topologi yang dicadangkan telah dibandingkan dengan topologi yang sedia. Perbandingan dijalankan dengan melihat bilangan suis, bilangan sumber arus terus dan jumlah keseluruhan komponen yang digunakan. Bagi mengesahkan daya maju topologi yang dicadangkan, model litar untuk penyongsang 9-aras, 25-aras dan 67-aras telah dibangunkan dan disimulasi menggunakan perisian Matlab-Simulink terlebih dahulu. Bentuk gelombang voltan dan arus bersama analisa jumlah herotan harmonik untuk beban perintang dan peraruh yang didapatkan daripada hasil simulasi akan disahkan dengan hasil eksperimen. Keputusan eksperimen penyongsang 9-aras dan 25-aras keluaran, yang prototaipnya di bina di dalam makmal akan dibentangkan dalam tesis ini. Strategi pensuisan berfrekuensi rendah dan frekuensi tinggi untuk penyongsang yang dicadangkan juga dibentangkan di dalam kerja ini. Model terma topologi yang dicadangkan ini dihasilkan menggunakan perisian PELCS dan analysis terperinci berkenaan kehilangan kuasa untuk penyongsang 9-aras dan 25-aras telah dijalankan. Topologi asas yang mempunyai sembilan suis didapati mempunyai jumlah voltan pegun (TSV) sebanyak 6.75 per unit manakala struktur topologi 25-aras yang mempuyai 12 suis sebanyak TSV 6.92 per unit sahaja. Perbandingan di antara topologi penyongsang yang sedia ada menunjukkan bahawa penyongsang yang dicadangkan memerlukan bilangan suis kuasa dan sumber dc yang sedikit tetapi dapat menjana keluaran aras yang sama. Disebabkan keperluan frekuensi pensuisan yang rendah, topologi yang dicadangkan adalah terpakai untuk aplikasi voltan tinggi dan sederhana, menyebabkan kehilangan pensuisan yang lebih rendah.

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LIST OF ABBREVIATIONS

ac	-	Alternative Current
APOD	-	Alternative Phase Opposite Disposition
CHB	-	Cascaded H-Bridge
CSC	-	Crossover Switches Cell
dc	-	Direct Current
DSP	-	Digital signal processor
EMI	-	Electromagnetic Interference
EV	-	Electric Vehicles
FACTS	-	Flexible ac Transmission System
FB	-	Full Bridge
FC	-	Flying Capacitor
FFT	-	Fast Fourier Transform
GPIO	-	General-purpose input/output
HPWM	-	Hybrid PWM
IPD	-	In-Phase Disposition
LSPWM	-	Level Shifted PWM
MLI	-	Multilevel Inverter
NLC	-	Nearest Level Control
NPC	-	Neutral Point Clamped
NVC	-	Nearest Vector Control
PD	-	Phase disposition
PF	-	Power Factor
PIV	-	Peak Inverse Voltage
POD	-	Phase Opposite Disposition
PSPWM	-	Phase Shifted PWM
PWM	-	Pulse Width Modulation
PUC	-	Packed U Cell
RMS	-	Root Mean Square
SHE	-	Selective Harmonic Elimination
SHM	-	Selective Harmonic Mitigation

SVM	-	Space Vector Modulation
SVPWM	-	Space Vector PWM
THD	-	Total Harmonic Distortion
TSV	-	Total Standing Voltage
VSC	-	Voltage Source Converters
VSI	-	Voltage Source Inverter

LIST OF SYMBOLS

$\alpha_1, \alpha_2, \alpha_{3,\ldots}$	-	Switching angles
V_{in}	-	Input Voltage
V_{in}	-	Output Voltage
T_s	-	Modulating period
N_{dc}	-	Number of dc-sources
N_{sw}	-	Number of switches
N_L	-	Number of levels
M	-	Modulation Index
f	-	Frequency
R	-	Resistance
L	-	Inductance

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

With the ever-increasing population, the demand for power consumption increases day by day. The oil crisis of the 1970s was an eye-opening experience for the research community. It made them realize that non-renewable or conventional resources were depleting. That motivated the industries and scientists to move towards renewable resources and explore their possibilities. Renewable energy sources provide unregulated electricity that may not be compatible with industrial and household appliances, necessitating power converters. Other low and medium-voltage applications require power electronics converters for renewable energy-based resources due to their enhanced power quality and improved efficiency. Highly efficient converters are required in electric vehicles (EVs) to regulate the drive's power flow and control. Moreover, a flexible ac transmission system (FACTS) requires multilevel converters to regulate and control the power flow. Thus, given all this wide range of applications, multilevel converters need to be studied, and their issues need to be explored. Photovoltaics, batteries, and fuel cells are sources that provide dc electricity. Such sources require an inverter to convert generated dc power into ac.

As the name suggests, inverter refers to the process of power inversion. In this case, the power inversion is from dc to ac. The concept of power inversion in an inverter can be broadly divided into two-level primitive inverters and multilevel inverters. The primitive two-level inverters produced only two levels $+V_{in}$ and $-V_{in}$, where V_{in} is the input dc voltage. [1]. They were also of two types; the simplest was where the output voltage continuously switched between the positive and negative input voltage with switching frequency. They were referred to as bipolar inverters as the output continuously fluctuated between both the polarities. The second type of the two-level inverters was referred to as unipolar. During half of the fundamental

frequency, the output voltage fluctuated between 0 and V_{in} while fluctuating between 0 and $-V_{in}$ during the second half. If a delay is provided at the 0 levels, then the unipolar inverter turns into three-level inverters with the output $+V_{in}$, 0, and $-V_{in}$ levels. This type is termed a quasi-square wave inverter. The increase in one level significantly reduces the THD in the output voltage waveform. Despite their simple and easy operation, two-level inverters suffer from several disadvantages: high total harmonics distortion (THD) content in the output voltage waveform, electromagnetic interference (EMI), high stress on the semiconductor devices, high power losses, and as a result, lower efficiency. Due to these disadvantages, the researcher starts focusing on developing multilevel inverters.

Multilevel inverters combine semiconductor devices/switches sequentially switched on and off in a predefined manner to give a staircase voltage waveform at the output [2]. Stepped waveform help reduce the voltage stress on the switches involved. The dv/dt ratio is also reduced, and the EMI will be reduced. The power quality increases as the stepped waveform are similar to the sinusoidal waveform, thus lowering harmonic content. The losses are reduced due to lower stress, and thus efficiency is improved [3]. The first attempt to generate more than one level was made in 1975 when the authors introduced a dead time at zero levels in the H-Bridge inverter to produce three-level output (quasi-square wave) [1]. After that, there were three topologies proposed in the beginning. They were neutral point clamped (NPC-MLI), flying capacitor (FC-MLI), and cascaded H-Bridge (CHB-MLI). These were termed conventional MLIs [4]. The recent increase in the demand for semiconductor devices has led to their fast development progression. This development has made it possible and feasible to use semiconductor devices for medium and high voltage and high-power applications [5, 6]. This has led to many multilevel inverter topologies suitable for medium and high voltage, high power applications [7, 8].

An NPC-MLI comprises two traditional two-level voltage source converters (VSCs) stacked one over the other with some minor modifications. For the NPC-MLI, only two switches are conducted to avoid the short through. The NPC-MLI is extended to a high power rating and more output voltage levels by adding additional power switches and clamping diodes [7]. The NPC-MLI's main advantage is that it utilizes a

single dc source. Still, the complexity increased due to the involvement of capacitors. Moreover, it requires a large number of passive components where the diodes are of different ratings. The FC-MLI topology is somewhat similar to the NPC-MLI. The main difference is that the clamping diodes are replaced by the flying capacitors [9]. In this topology, the load is not directly connected to the neutral point of the converter to generate zero levels. Instead, the zero levels are obtained by connecting the load to the positive or negative bar through the flying capacitors with opposite polarity concerning dc-link. The capacitor is floating instead hence, the name flying capacitor. The concept of FC-MLI can be extended to the desired number of levels. Utilizing a single dc source is still the main advantage for FC-MLI. Another positive aspect of this topology is the availability of redundant states. The problem in FC-MLI will be visible when used for 5-level MLI and higher. The charge of the capacitors is not easy to balance for a high-level MLI.

Based on the magnitude of the dc-sources/dc-links in the topology, MLIs can be classified into symmetric topologies or asymmetric topologies. They are termed symmetric topologies when all the dc-sources/dc-links are equal in magnitude. If the magnitude of the sources is unequal, it is termed asymmetric topologies. Symmetric topologies offer simplicity in control with low voltage stress on switches. However, asymmetric topologies can offer higher output voltage level generation than symmetric topologies for the same number of device counts. The magnitude of the dc-sources/dc-link is essential in determining the number of levels generated and the maximum voltage stress to endure by the switches.

The main problem to address in the topology design is to keep track of its feasibility in terms of device count, volume size, and circuit complexity. The asymmetrical topologies are mostly designed with this view. The earliest work for asymmetrical inverters can be traced back to Manjrekar et al. [10, 11]. In their work, the authors proposed a new binary method of choosing the magnitude of dc-sources for cascaded H-bridge topology. The output level dramatically increased with the same number of components compared to the symmetrical counterpart. The author in [12] proposed a novel topology to produce stepped output; it employs a principal dc source bus. The rest of the dc buses were capacitor banks. The converter control algorithm

stabilized the voltage across capacitors. This topology offered a reduction in devices, but it required a complex algorithm for voltage balancing.

In reference [13], the author proposes a novel topology that employs a single dc source and three capacitors to produce a seven-level output. The topology is suitable for solar photovoltaic-grid applications. Nonetheless, the topology suffers from a high total component count. Babei in [14] proposes a capacitor-based asymmetric MLI topology. The topology has better THD performance and employs fewer components, increasing the output level considerably. However, it suffers from the voltage balancing issue for the capacitors. The topology requires special attention for capacitor balancing, increasing the complexity of the control algorithm. Gautam et al. in [15] proposed another hybrid topology that employed two dc-sources with capacitors. The number of capacitors depends on the output level required. The topology offers fundamental switching and equal power-sharing among the cells but requires different power rating switches. However, the capacitors are not self-balancing, making the control algorithm too complex for development. Jain et al. in [16] present a topology specifically for solar photovoltaic-based applications. The topology utilizes an equal number of dc-sources and capacitors. The topology offers reduced conduction losses as the number of switches in the conduction path is reduced and has a lower common-mode current, making it highly suitable for solar photovoltaic applications.

The symmetric topologies require more components to generate more voltage levels. It results in low efficiency, increased size, and low reliability. However, asymmetric topologies solve this issue. It maintains the number of switches but can increase the output voltage level by unequal dc-sources. The problem that asymmetric topologies might face is increased control complexity if the capacitors as dc links are involved. Not every capacitor can be self-balancing; some of the capacitors may require an extra algorithm for charge balancing. Thus, the issue in asymmetrical topologies is designing the topology without capacitor involvement and reduced device count. This thesis has proposed asymmetrical topologies that do not require any capacitor in their operation, thus reducing the control complexity. Moreover, the proposed work requires a lower device count in comparison with the other asymmetrical topologies.

1.2 Features and Applications of MLI

The previous section discussed the fundamental of MLIs, the main three conventional MLI topologies, and some significant recent topologies. From that discussion, many shortcomings of the conventional MLI came into the picture, which led to the development of various other recent topologies for MLI. One of the major disadvantages of the conventional MLI is the high device count. The higher the device count, the lesser will be efficiency. Moreover, a higher device count means increased cost and less compact operation. In addition, for FC-MLI, the involvement of a flying capacitor leads to the addition in the control complexity as the capacitor requires extra attention for charge control and voltage balancing. The problem is inherent in high-level MLI. Thus, keeping in sight these problems, many different topologies of MLI have been proposed. Major features of the newly developed MLI topologies will be at least to have these:

Reduction in Device Count: As discussed above, conventional topologies require higher semiconductors and active and passive devices. This leads to higher costs and less feasibility. Moreover, higher semiconductor devices mean higher losses and less efficiency. Modern topologies require a lower number of devices and thus are more feasible and efficient. Lower device count also means compact nature [17].

Reduction in Control Complexity: Conventional topologies, especially FC-MLI, operate on the flying capacitor. The voltage balance issue of the capacitor involved can persist if not appropriately addressed and causes control complexity. Modern topologies focus on lesser use of capacitors. If the capacitors are utilized, they are used in such a manner to get them self-balancing, thus, reducing the control complexity [18].

Improved Efficiency: Conventional topologies have considerably lower efficiency because of higher device count. Modern topologies offer higher efficiency as they lower the device count [19].

Compact Structure: Modern topologies are compact and less bulky. Meanwhile, conventional topologies require larger space because of the high device count [20].

Improved Feasibility: Modern topologies have higher feasibility as compared to conventional ones. This is because modern topologies have reduced components, thus having lower losses and higher efficiency [21].

Low Electromagnetic Interference (EMI): Electromagnetic Interference (EMI) causes losses in the converter and causes problems with the various communication lines. The high dv/dt ratio causes this. As the number of levels/steps increases in the output waveform, the dv/dt ratio decreases. Thus, the EMI is also reduced.

Low Total Harmonic Distortion (THD): Higher the steps in the output waveform, the more closely it will imitate the ideal sinusoidal waveform. Thus, lesser would be the harmonic content, and better would be the power quality. IEEE has set up various standards for injecting power into the electric grid, which help maintain the utility grid's stability. These power quality standards must be strictly followed while setting up the converter to grid interfacing. Increasing the number of levels can help improve the power quality and meet the IEEE standards.

1.3 Problem Statement

Multilevel inverters have become an important aspect of the electrical power generation industry. Several shortcomings of the classical two-level inverters, namely poor output voltage quality, high switching stress on the semiconductor devices, etc., were solved by the MLIs. In MLI research, the ultimate goal is to generate a high-level output voltage with minimum components count. Hence, countless MLI topologies have been introduced with absurd high output levels for the past few decades.

An increased components count, meaning a higher development cost, added volume size, increment in control complexity, and reduced efficiency. Moreover, it can unnecessarily cause an increased and unequal voltage stress on the power semiconductors. The voltage stress on semiconductor devices is also an important criterion for determining the topology's feasibility. It helps determine the required component rating. The higher the stress to be endured, the higher the rating, and as a result, the higher the cost. The stress is measured in terms of total standing voltage (TSV). It is the sum of the maximum stress on every switch in its OFF state. A possible solution to this problem is asymmetric topologies. Careful selection of the magnitude of dc-sources can increase the output levels with the same number of semiconductor devices as their symmetrical counterparts.

Asymmetrical MLIs are capable of generating higher output levels with reduced device count thus are given preference over symmetrical topology in many applications. To reduce the number of sources in asymmetrical topologies, capacitors are often used, requiring appropriate voltage balancing for the proper operation of the circuit. Adding capacitors is a plausible option to reduce the number of dc-sources, increasing the control complexity. Considering the above discussion, attempts are being made to overcome these problems. Many of these are producing unnecessarily higher levels utilizing too many components. Although some of the topologies significantly address the issues, all of these required a higher number of sources and switches than the asymmetrical trinary CHB-MLI. Designing a topology capable of producing significantly higher levels utilizing a lower number of component count without using capacitors remains a challenge.

1.4 Research Objectives

Based on the above discussion and problem mentioned above statement, the specific objectives of this research work are listed as follows:

(a) To develop an efficient asymmetric multilevel inverter topology with reduced power semiconductor switches and dc-sources.

(b) To propose a dc-source selection algorithm for the proposed topology and develop the expressions of different parameters of the extended structure.

(c) To construct the prototype and validate the performance under different loading conditions.

1.5 Organization of Thesis

This thesis is organized into six chapters. This chapter provided the introduction to the multilevel converters and the objective of this thesis. The problem statement clearly states that this thesis will handle issues for multilevel converters. The remaining chapters are briefly outlined as follows.

Chapter 2 demonstrates a comprehensive overview of the existing literature. In the literature review, the classification of MLI topologies is first presented, and then recently, proposed asymmetrical topologies were discussed. Based on different parameters, a detailed analysis of different topologies was discussed.

Chapter 3 will depict the circuit structure of the proposed topology. It will also describe the working principle of the topology. Different modes of operation will be discussed and shown through a series of figures. A proposal on the dc-source selection algorithm and generalized expressions were also presented. Various topology characteristics will be calculated mathematically, and the relevant equations will be formed.

Chapter 4 will then deal with the modelling and simulation of the proposed topologies in the Matlab/Simulink environment. The performance of the topology will be verified through Matlab modelling. Constant R and RL load will emulate the constant load operation, while the sudden change of load in R and RL conditions will check the dynamic performance of the proposed converter. Another important thing to check is if the proposed topology is susceptible to control algorithm fault. This

capability will be checked through modulation index change during the simulation. It will check the same parameters for a low switching control strategy for nearest level control (NLC). For level-shifted sinusoidal PWM (LS-PWM), high switching frequency control strategy. Power losses and efficiency will be evaluated by developing a thermal model of the proposed inverter using PLECS software.

Chapter 5 will deal with the hardware implementation of the proposed topology. First, the nine-level topology simulation results will be verified through experimental testing, and then the 25-level topology is validated.

Finally, chapter 6 will conclude the research work and present a critical discussion of the results and comparative analysis of the proposed topology, along with the recommendation for future work.

REFRENCES

1. Lipo, T.A. and F.G. Turnbull, *Analysis and comparison of two types of square-wave inverter drives.* IEEE Transactions on Industry Applications, 1975(2): p. 137-147.
2. Cho, G.-H. *A general circuit topology of multilevel inverter*. 1991. IEEE.
3. Panagis, P., et al. *Comparison of state of the art multilevel inverters*. in *2008 IEEE Power Electronics Specialists Conference*. 2008. IEEE.
4. Lai, J.-S. and F.Z. Peng, *Multilevel converters-a new breed of power converters.* IEEE Transactions on industry applications, 1996. **32**(3): p. 509-517.
5. Dieckerhoff, S., S. Bernet, and D. Krug, *Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications.* IEEE Transactions on power electronics, 2005. **20**(6): p. 1328-1336.
6. Wu, L., et al., *Efficiency evaluation of the modular multilevel converter based on Si and SiC switching devices for medium/high-voltage applications.* IEEE Transactions on Electron Devices, 2014. **62**(2): p. 286-293.
7. Gupta, K.K., et al., *Multilevel inverter topologies with reduced device count: A review.* IEEE transactions on Power Electronics, 2015. **31**(1): p. 135-151.
8. Fang, J., et al., *A Review of Multilevel Converters with Parallel Connectivity.* IEEE Transactions on Power Electronics, 2021.
9. Rodríguez, J., et al., *Multilevel voltage-source-converter topologies for industrial medium-voltage drives.* IEEE Transactions on industrial electronics, 2007. **54**(6): p. 2930-2945.
10. Manjrekar, M.D. and T.A. Lipo. *A hybrid multilevel inverter topology for drive applications*. in *APEC'98 Thirteenth Annual Applied Power Electronics Conference and Exposition*. 1998. IEEE.
11. Manjrekar, M.D., P.K. Steimer, and T.A. Lipo, *Hybrid multilevel power conversion system: A competitive solution for high-power applications.* IEEE transactions on industry applications, 2000. **36**(3): p. 834-841.
12. Ounejjar, Y., K. Al-Haddad, and L.-A. Gregoire, *Packed U cells multilevel converter topology: theoretical study and experimental validation.* IEEE Transactions on Industrial Electronics, 2010. **58**(4): p. 1294-1306.
13. Ebrahimi, J., E. Babaei, and G.B. Gharehpetian, *A new multilevel converter topology with reduced number of power electronic components.* IEEE Transactions on industrial electronics, 2011. **59**(2): p. 655-667.
14. Babaei, E., M. Farhadi Kangarlu, and M. Sabahi, *Extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters.* IET Power Electronics, 2014. **7**(1): p. 157-166.
15. Gautam, S.P., L. Kumar, and S. Gupta, *Hybrid topology of symmetrical multilevel inverter using less number of devices.* IET Power electronics, 2015. **8**(11): p. 2125-2135.
16. Jain, S. and V. Sonti, *A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems.* IEEE transactions on industrial electronics, 2016. **64**(4): p. 2865-2875.

17. Kangarlu, M.F., E. Babaei, and S. Laali, *Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources.* IET Power Electronics, 2012. **5**(5): p. 571-581.
18. Corzine, K.A., et al., *Control of cascaded multilevel inverters.* IEEE transactions on power electronics, 2004. **19**(3): p. 732-738.
19. Perantzakis, G.S., et al., *Comparison of power losses, current and voltage stresses of semiconductors in voltage source transformerless multilevel inverters.* IET Power Electronics, 2014. **7**(11): p. 2743-2757.
20. Tolbert, L.M. and F.Z. Peng. *Multilevel converters as a utility interface for renewable energy systems*. in *2000 Power Engineering Society Summer Meeting (Cat. No. 00CH37134)*. 2000. IEEE.
21. Sridhar, V. and S. Umashankar, *A comprehensive review on CHB MLI based PV inverter and feasibility study of CHB MLI based PV-STATCOM.* Renewable and Sustainable Energy Reviews, 2017. **78**: p. 138-156.
22. Malinowski, M., et al., *A Survey on Cascaded Multilevel Inverters.* IEEE Transactions on Industrial Electronics, 2010. **57**(7): p. 2197-2206.
23. Rodriguez, J., et al., *A survey on neutral-point-clamped inverters.* IEEE transactions on Industrial Electronics, 2009. **57**(7): p. 2219-2230.
24. Meynard, T.A. and H. Foch. *Multi-level conversion: high voltage choppers and voltage-source inverters*. in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*. 1992.
25. Peng, F.Z. and J.-S. Lai, *Multilevel cascade voltage source inverter with seperate DC sources*. 1997, Google Patents.
26. Chen, A. and X. He, *Research on Hybrid-Clamped Multilevel-Inverter Topologies.* IEEE Transactions on Industrial Electronics, 2006. **53**(6): p. 1898-1907.
27. Patrao, I., et al., *Transformerless topologies for grid-connected single-phase photovoltaic inverters.* Renewable and Sustainable Energy Reviews, 2011. **15**(7): p. 3423-3431.
28. Edpuganti, A. and A.K. Rathore, *A survey of low switching frequency modulation techniques for medium-voltage multilevel converters.* IEEE Transactions on Industry Applications, 2015. **51**(5): p. 4212-4228.
29. Baker, R.H. and L.H. Bannister, *Electric power converter*. 1975, Google Patents.
30. Latran, M.B. and A. Teke, *Investigation of multilevel multifunctional grid connected inverter topologies and control strategies used in photovoltaic systems.* Renewable and Sustainable Energy Reviews, 2015. **42**: p. 361-376.
31. Gupta, K.K., et al., *Multilevel inverter topologies with reduced device count: a review.* Power Electronics, IEEE Transactions on, 2016. **31**(1): p. 135-151.
32. Babaei, E., et al., *Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology.* Electric Power Systems Research, 2007. **77**(8): p. 1073-1085.
33. Babaei, E., *Optimal topologies for cascaded sub-multilevel converters.* Journal of Power Electronics, 2010. **10**(3): p. 251-261.
34. Ounejjar, Y. and K. Al-Haddad. *A novel high energetic efficiency multilevel topology with reduced impact on supply network*. in *2008 34th Annual Conference of IEEE Industrial Electronics*. 2008.
35. Ounejjar, Y., K. Al-Haddad, and L.A. Dessaint, *A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation.* IEEE Transactions on Industrial Electronics, 2011. **59**(10): p. 3808-3816.

36. Gupta, K.K. and S. Jain, *Multilevel inverter topology based on series connected switched sources.* IET Power Electronics, 2013. **6**(1): p. 164-174.
37. Gupta, K.K. and S. Jain, *A novel multilevel inverter based on switched DC sources.* IEEE Transactions on Industrial Electronics, 2013. **61**(7): p. 3269-3278.
38. Liao, Y. and C. Lai, *Newly-Constructed Simplified Single-Phase Multistring Multilevel Inverter Topology for Distributed Energy Resources.* IEEE Transactions on Power Electronics, 2011. **26**(9): p. 2386-2392.
39. Gupta, K.K. and S. Jain, *Topology for multilevel inverters to attain maximum number of levels from given DC sources.* Power Electronics, IET, 2012. **5**(4): p. 435-446.
40. Gupta, K.K. and S. Jain, *A multilevel Voltage Source Inverter (VSI) to maximize the number of levels in output waveform.* International Journal of Electrical Power & Energy Systems, 2013. **44**(1): p. 25-36.
41. Banaei, M.R., M.R.J. Oskuee, and H. Khounjahan, *Reconfiguration of semi-cascaded multilevel inverter to improve systems performance parameters.* IET Power Electronics, 2014. **7**(5): p. 1106-1112.
42. Oskuee, M.R.J., et al., *An innovative scheme of symmetric multilevel voltage source inverter with lower number of circuit devices.* IEEE Transactions on Industrial Electronics, 2015. **62**(11): p. 6965-6973.
43. Babaei, E. and S.H. Hosseini, *New cascaded multilevel inverter topology with minimum number of switches.* Energy Conversion and Management, 2009. **50**(11): p. 2761-2767.
44. Dixon, J. and L. Moran, *High-level multistep inverter optimization using a minimum number of power transistors.* IEEE Transactions on power electronics, 2006. **21**(2): p. 330-337.
45. Babaei, E., *A cascade multilevel converter topology with reduced number of switches.* IEEE Transactions on power electronics, 2008. **23**(6): p. 2657-2664.
46. Babaei, E., et al., *Cascaded multilevel inverter using sub-multilevel cells.* Electric Power Systems Research, 2013. **96**: p. 101-110.
47. Babaei, E., M.F. Kangarlu, and F.N. Mazgar, *Symmetric and asymmetric multilevel inverter topologies with reduced switching devices.* Electric Power Systems Research, 2012. **86**: p. 122-130.
48. Hinago, Y. and H. Koizumi, *A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources.* IEEE Transactions on Industrial Electronics, 2010. **57**(8): p. 2643-2650.
49. Babaei, E., S.S. Gowgani, and M. Sabahi, *Modified Multilevel Inverters Using Series and Parallel Connection of DC Voltage Sources.* Arabian Journal for Science and Engineering, 2014. **39**(4): p. 3077-3094.
50. Tsunoda, A., Y. Hinago, and H. Koizumi, *Level- and Phase-Shifted PWM for Seven-Level Switched-Capacitor Inverter Using Series/Parallel Conversion.* IEEE Transactions on Industrial Electronics, 2014. **61**(8): p. 4011-4021.
51. Choi, W.-K. and F.-s. Kang. *H-bridge based multilevel inverter using PWM switching function*. in *INTELEC 2009-31st International Telecommunications Energy Conference*. 2009. IEEE.
52. Kangarlu, M.F. and E. Babaei, *Cross-switched multilevel inverter: an innovative topology.* IET power electronics, 2013. **6**(4): p. 642-651.
53. Banaei, M. and A.F. Bakhshayesh, *Selection of DC voltage magnitude using Fibonacci series for new hybrid asymmetrical multilevel inverter with minimum PIV.* Alexandria Engineering Journal, 2014. **53**(3): p. 529-535.

54. Banaei, M. and E. Salary, *New multilevel inverter with reduction of switches and gate driver.* Energy Conversion and Management, 2011. **52**(2): p. 1129-1136.
55. Barzegarkhoo, R., et al., *Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches.* IEEE Transactions on Power Electronics, 2015. **31**(8): p. 5604-5617.
56. Prabaharan, N. and K. Palanisamy, *Investigation of single phase reduced switch count asymmetric Multilevel Inverter using Advanced Pulse Width Modulation Technique.* International Journal of Renewable Energy Research, 2015. **5**(3): p. 879-890.
57. Samadaei, E., et al., *An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters With Reduced Components.* IEEE Transactions on Industrial Electronics, 2016. **63**(11): p. 7148-7156.
58. Vahedi, H., et al. *Crossover Switches Cell (CSC): A new multilevel inverter topology with maximum voltage levels and minimum DC sources*. in *IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society*. 2013. IEEE.
59. Vahedi, H. and K. Al-Haddad, *Real-Time Implementation of a Seven-Level Packed U-Cell Inverter with a Low-Switching-Frequency Voltage Regulator.* IEEE Transactions on Power Electronics, 2016. **31**(8): p. 5967-5973.
60. Trabelsi, M., et al., *Finite-Control-Set Model Predictive Control for Grid-Connected Packed-U-Cells Multilevel Inverter.* IEEE Transactions on Industrial Electronics, 2016. **63**(11): p. 7286-7295.
61. Ebrahimi, J., E. Babaei, and G.B. Gharehpetian, *A New Topology of Cascaded Multilevel Converters With Reduced Number of Components for High-Voltage Applications.* IEEE Transactions on Power Electronics, 2011. **26**(11): p. 3109-3118.
62. Ebrahimi, J., E. Babaei, and G.B. Gharehpetian, *A New Multilevel Converter Topology With Reduced Number of Power Electronic Components.* IEEE Transactions on Industrial Electronics, 2012. **59**(2): p. 655-667.
63. Beser, E., et al. *Design and application of a novel structure and topology for multilevel inverter*. in *2008 International Symposium on Power Electronics, Electrical Drives, Automation and Motion*. 2008.
64. Ramkumar, S., et al., *A new series parallel switched multilevel dc-link inverter topology.* International Journal of Electrical Power & Energy Systems, 2012. **36**(1): p. 93-99.
65. Waltrich, G. and I. Barbi. *Three-phase Cascaded multilevel inverter using power cells with two inverter legs in series*. in *2009 IEEE Energy Conversion Congress and Exposition*. 2009.
66. Babaei, E., A. Dehqan, and M. Sabahi, 2013. **13**.
67. Gautam, S.P., et al. *New topology with reduced number of switches in asymmetrical cascaded multilevel inverter*. in *Fifth International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2013)*. 2013.
68. Babaei, E., M.F. Kangarlu, and M.A. Hosseinzadeh, *Asymmetrical multilevel converter topology with reduced number of components.* IET Power Electronics, 2013. **6**(6): p. 1188-1196.
69. Babaei, E., S. Alilu, and S. Laali, *A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on*

Developed H-Bridge. IEEE Transactions on Industrial Electronics, 2014. **61**(8): p. 3932-3939.
70. Babaei, E. and S. Laali, *Optimum Structures of Proposed New Cascaded Multilevel Inverter With Reduced Number of Components.* IEEE Transactions on Industrial Electronics, 2015. **62**(11): p. 6887-6895.
71. Babaei, E., S. Laali, and S. Alilu, *Cascaded Multilevel Inverter With Series Connection of Novel H-Bridge Basic Units.* IEEE Transactions on Industrial Electronics, 2014. **61**(12): p. 6664-6671.
72. Babaei, E., S. Laali, and S. Bahravar, *A New Cascaded Multi-level Inverter Topology with Reduced Number of Components and Charge Balance Control Methods Capabilities.* Electric Power Components and Systems, 2015. **43**(19): p. 2116-2130.
73. Babaei, E., S. Laali, and Z. Bayat, *A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches.* IEEE Transactions on Industrial Electronics, 2015. **62**(2): p. 922-929.
74. Hsieh, C., et al., *Design and Implementation of a Novel Multilevel DC–AC Inverter.* IEEE Transactions on Industry Applications, 2016. **52**(3): p. 2436-2443.
75. Gautam, S.P., L.K. Sahu, and S. Gupta, *Reduction in number of devices for symmetrical and asymmetrical multilevel inverters.* IET Power Electronics, 2016. **9**(4): p. 698-709.
76. Samanbakhsh, R. and A. Taheri, *Reduction of Power Electronic Components in Multilevel Converters Using New Switched Capacitor-Diode Structure.* IEEE Transactions on Industrial Electronics, 2016. **63**(11): p. 7204-7214.
77. Alishah, R.S., et al., *Optimal Design of New Cascaded Switch-Ladder Multilevel Inverter Structure.* IEEE Transactions on Industrial Electronics, 2017. **64**(3): p. 2072-2080.
78. El-Naggar, K. and T.H. Abdelhamid, *Selective harmonic elimination of new family of multilevel inverters using genetic algorithms.* Energy Conversion and Management, 2008. **49**(1): p. 89-95.
79. Perez, M.A., et al., *Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters.* IEEE Transactions on Power Electronics, 2015. **30**(1): p. 4-17.
80. Rodriguez, J., J.-S. Lai, and F.Z. Peng, *Multilevel inverters: a survey of topologies, controls, and applications.* IEEE Transactions on industrial electronics, 2002. **49**(4): p. 724-738.
81. Dahidah, M.S.A., G. Konstantinou, and V.G. Agelidis, *A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications.* IEEE Transactions on Power Electronics, 2015. **30**(8): p. 4091-4106.
82. Patel, H.S. and R.G. Hoft, *Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I--Harmonic Elimination.* IEEE Transactions on Industry Applications, 1973. **IA-9**(3): p. 310-317.
83. Patel, H.S. and R.G. Hoft, *Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part II --- Voltage Control Techniques.* IEEE Transactions on Industry Applications, 1974. **IA-10**(5): p. 666-673.
84. Franquelo, L.G., et al., *A Flexible Selective Harmonic Mitigation Technique to Meet Grid Codes in Three-Level PWM Converters.* IEEE Transactions on Industrial Electronics, 2007. **54**(6): p. 3022-3029.

85. Jian, S., S. Beineke, and H. Grotstollen, *Optimal PWM based on real-time solution of harmonic elimination equations.* IEEE Transactions on Power Electronics, 1996. **11**(4): p. 612-621.
86. Yang, K., et al., *A Groebner Bases Theory-Based Method for Selective Harmonic Elimination.* IEEE Transactions on Power Electronics, 2015. **30**(12): p. 6581-6592.
87. Yang, K., et al., *Selective Harmonic Elimination With Groebner Bases and Symmetric Polynomials.* IEEE Transactions on Power Electronics, 2016. **31**(4): p. 2742-2752.
88. Barkat, S., E.M. Berkouk, and M.S. Boucherit, *Particle swarm optimization for harmonic elimination in multilevel inverters.* Electrical Engineering, 2009. **91**(4-5): p. 221-228.
89. Hiendro, A., *Multiple switching patterns for SHEPWM inverters using differential evolution algorithms.* International Journal of Power Electronics and Drive Systems, 2011. **1**(2): p. 94-103.
90. Taghizadeh, H. and M.T. Hagh, *Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization.* IEEE Transactions on Industrial Electronics, 2010. **57**(11): p. 3678-3684.
91. Sundareswaran, K., K. Jayant, and T.N. Shanavas, *Inverter Harmonic Elimination Through a Colony of Continuously Exploring Ants.* IEEE Transactions on Industrial Electronics, 2007. **54**(5): p. 2558-2565.
92. Kavousi, A., et al., *Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters.* IEEE Transactions on Power Electronics, 2012. **27**(4): p. 1689-1696.
93. Salehi, R., et al., *Harmonie elimination and optimization of stepped voltage of multilevel inverter by bacterial foraging algorithm.* Journal of Electrical Engineering and Technology, 2010. **5**(4): p. 545-551.
94. Rodriguez, J., et al., *A vector control technique for medium-voltage multilevel inverters.* IEEE Transactions on Industrial Electronics, 2002. **49**(4): p. 882-888.
95. Kouro, S., et al., *Recent Advances and Industrial Applications of Multilevel Converters.* IEEE Transactions on Industrial Electronics, 2010. **57**(8): p. 2553-2580.
96. Jonnala, R.B. and S.B. Choppavarapu, *Modeling hybrid modulation strategy with nearest leveled vector switching pattern in space vector control technique for multilevel inverters.* Turkish Journal of Electrical Engineering and Computer Science, 2017. **25**(2): p. 717-734.
97. Perez, M., et al. *Power Distribution in Hybrid Multi-cell Converter with Nearest Level Modulation*. in *2007 IEEE International Symposium on Industrial Electronics*. 2007.
98. Rodríguez, J., et al., The Age of Multilevel Converters Arrives, 2008: p. 28-39.
99. Edpuganti, A. and A.K. Rathore, *Optimal Low-Switching Frequency Pulsewidth Modulation of Medium Voltage Seven-Level Cascade-5/3H Inverter*. IEEE Transactions on Power Electronics, 2015. **30**(1): p. 496-503.
100. Alishah, R.S., et al., *New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels.* IET Power Electronics, 2014. **7**(1): p. 96-104.
101. Kazmierkowski, M.P., et al., *High-performance motor drives.* IEEE Industrial Electronics Magazine, 2011. **5**(3): p. 6-26.

102. Naderi, R. and A. Rahmati, *Phase-Shifted Carrier PWM Technique for General Cascaded Inverters.* IEEE Transactions on Power Electronics, 2008. **23**(3): p. 1257-1269.
103. Carrara, G., et al. *A new multilevel PWM method: a theoretical analysis*. in *21st Annual IEEE Conference on Power Electronics Specialists*. 1990.
104. Zhao, J., X. He, and R. Zhao, *A Novel PWM Control Method for Hybrid-Clamped Multilevel Inverters.* IEEE Transactions on Industrial Electronics, 2010. **57**(7): p. 2365-2373.
105. Dargahi, V., et al., *Flying Capacitors Reduction in an Improved Double Flying Capacitor Multicell Converter Controlled by a Modified Modulation Method.* IEEE Transactions on Power Electronics, 2012. **27**(9): p. 3875-3887.
106. Boost, M.A. and P.D. Ziogas, *State-of-the-art carrier PWM techniques: a critical evaluation.* IEEE Transactions on Industry Applications, 1988. **24**(2): p. 271-280.
107. Alexander, S.A., *Development of solar photovoltaic inverter with reduced harmonic distortions suitable for Indian sub-continent.* Renewable and Sustainable Energy Reviews, 2016. **56**: p. 694-704.
108. Carrara, G., et al., *A New Multilevel PWM Method: A Theoretical Analysis.* IEEE Transactions on Power Electronics, 1992. **7**(3): p. 497-505.
109. Gandomi, A.A., et al., *Transformer-based inverter with reduced number of switches for renewable energy applications.* IET Power Electronics, 2015. **8**(10): p. 1875-1884.
110. Silva, C.A., et al., *Implementation and Control of a Hybrid Multilevel Converter With Floating DC Links for Current Waveform Improvement.* IEEE Transactions on Industrial Electronics, 2011. **58**(6): p. 2304-2312.
111. Massoud, A.M., S.J. Finney, and B.W. Williams, *Mapped hybrid spaced vector modulation for multilevel cascaded-type voltage source inverters.* IET Power Electronics, 2008. **1**(3): p. 318-335.
112. Kangarlu, M.F. and E. Babaei, *A Generalized Cascaded Multilevel Inverter Using Series Connection of Submultilevel Inverters.* IEEE Transactions on Power Electronics, 2013. **28**(2): p. 625-636.
113. Hinago, Y. and H. Koizumi, *A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources.* Industrial Electronics, IEEE Transactions on, 2010. **57**(8): p. 2643-2650.
114. Choi, W.K. and F.s. Kang. *H-bridge based multilevel inverter using PWM switching function*. in *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International*. 2009.
115. Ounejjar, Y., K. Al-Haddad, and L.A. Gregoire, *Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation.* IEEE Transactions on Industrial Electronics, 2011. **58**(4): p. 1294-1306.
116. Pérez, M., et al. *Power distribution in hybrid multi-cell converter with nearest level modulation*. in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*. 2007. IEEE.
117. Meshram, P.M. and V.B. Borghate, *A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC).* IEEE Transactions on Power Electronics, 2015. **30**(1): p. 450-462.
118. Wang, Y., et al., *A Nearest Level PWM Method for the MMC in DC Distribution Grids.* IEEE Transactions on Power Electronics, 2018. **PP**(99): p. 1-1.

LIST OF PUBLICATIONS

1. Arif, M., S. Ayob, and Z. Salam, *Asymmetrical Nine-Level Inverter Topology with Reduce Power Semiconductor Devices.* TELKOMNIKA (Telecommunication Computing Electronics and Control), 2018. **16**(1).

2. Arif, M.S.b., S.M. Ayob, and Z. Salam. *Asymmetrical multilevel inverter topology with reduced power semiconductor devices*. in *2016 IEEE Industrial Electronics and Applications Conference (IEACon)*. 2016.

3. Arif, M.S.B., S.M. Ayob, and Z. Salam. *A new asymmetrical multilevel inverter topology with reduced device counts*. in *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*. 2016.