GRAPHENE FLOATING GATE FLASH MEMORY PERFORMANCE WITH HIGH-K TUNNEL BARRIER ENGINEERING

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DEDICATION

This thesis is dedicated to my family.

Thank you.

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ABSTRACT

In recent years, due to outstanding properties such as durability material, ultrafast electronic performance and ultrasensitive for sensors, graphene has become a demanded material today and in the future due to its remarkable properties. For transistors, the scaling of component sizes has become a bottleneck for silicon-based materials. This study aims to investigate the memory performances of graphene as a charge storage layer in the floating gate with the different type of high-k materials such as silicon nitride (Si_3N_4), aluminium oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) using Silvaco ATLAS TCAD tool simulation. The simulation work initially is to validate the experimental work with the simulation data and then determine the performance of the flash memory cell with different type of high-k materials in terms of memory window, program and erase (P/E) characteristics data retention and endurance. Next is to validate in the context of the memory performance trend between the experimental work and the proposed work. The memory window for flash memory cell for silicon dioxide (SiO_2) is 15.4 V while for the memory window using variable oxide thickness (VARIOT) of 1/7 nm of SiO_2/high-k material of four high-k materials for SiO_2/Si_3N_4, SiO_2/Al_2O_3, SiO_2/HfO_2 and SiO_2/ZrO_2 tunnel barrier are 23.0 V, 20.0 V, 25.4 V and 26.0 V, respectively at the same P/E voltage of ±20 V programming and erasing voltage. Conventional SiO_2 has good data retention but P/E characteristic is better with the introduction of VARIOT. The data retention capability of the four high-k materials is better than that of conventional SiO_2, and the data can be retained by 75% (11.6 V) after 10 years of extrapolation with -1/1 V gate stress. For high-k material of SiO_2/Si_3N_4, SiO_2/HfO_2 and SiO_2/ZrO_2 tunnel barrier, data are retained by 56% (12.9 V), 47% (11.9 V) and 33% (8.6 V) while SiO_2/Al_2O_3 tunnel barrier with thickness 1/7 nm shows an excellent result among others with 83% (16.6 V) data retained. The endurance performance of the best high-k materials SiO_2/Al_2O_3 and SiO_2/HfO_2 was tested, which showed that the endurance retained 82% and 75% of the charge during 10^4 P/E cycles, respectively.

ABSTRAK

Sejak kebelakangan ini, graphene telah menjadi bahan dengan permintaan tinggi pada masa sekarang dan masa hadapan kerana ciri-ciri yang luar biasa seperti bahan tahan lasak, prestasi terpantas bahan elektronik dan juga bahan yang sangat sensitif untuk penderia. Untuk transistor, pengskalaan saiz komponen telah mencapai titik maksima bagi bahan berdasarkan silikon. Kajian ini bertujuan untuk menyiasat prestasi memori mengunakan graphene sebagai lapisan simpanan cas di dalam get apungan dengan pembezaan jenis bahan tinggi-k seperti silikon nitrida (Si_3N_4), aluminium oksida (Al_2O_3), hafnium oksida (HfO_2) dan zikronium oksida (ZrO_2) dengan mengunakan alat simulasi Silvaco ATLAS TCAD. Kajian dimulakan dengan kerja simulasi untuk mengesahkan kerja eksperimen terdahulu dan kemudian mengenalpasti prestasi sel memori imbas dengan perbezaan jenis bahan tinggi-k untuk tingkap memori, ciri-ciri data program dan padam (P/E), data pengekalan dan juga data ketahanan. Pengesahan didalam konteks ini merujuk kepada pengesahan gaya prestasi memori diantara kerja eksperimen dan kerja cadangan. Tingkap memori untuk memori imbas yang menggunakan silikon dioksida (SiO_2) ialah 15.4 V sementara tingkap memori dengan kewujudan pemboleh ubah ketebalan oksida (VARIOT) untuk 1/7 nm silikon dioksida SiO_2/bahan tinggi-k untuk empat bahan tinggi-k seperti SiO_2/Si_3N_4, SiO_2/Al_2O_3, SiO_2/HfO_2 dan SiO_2/ZrO_2 di terowong penghalang ialah masing-masing 23.0 V, 20.0 V, 25.4 V dan 26.0 V bagi P/E voltan yang sama iaitu ±20 V voltan program dan padam. SiO_2 konvensional ialah bagus untuk data pengekalan namun kajian terhadap ciri-ciri P/E menunjukkan prestasi yang lebih baik dengan kehadiran VARIOT. Kemampuan data pengekalan untuk empat bahan tinggi-k menunjukkan prestasi yang lebih baik berbanding dengan konvensional SiO_2 dimana data kekal sebanyak 75% (11.6 V) selepas 10 tahun ekstrapolasi dengan -1/1 V tekanan get. Untuk bahan tinggi-k SiO_2/Si_3N_4, SiO_2/HfO_2 dan SiO_2/ZrO_2 terowong penghalang, masing-masing menunjukkan data kekal sebanyak 56% (12.9 V), 47% (11.9 V) dan 33% (8.6 V) dimana SiO_2/Al_2O_3 terowong penghalang dengan ketebalan 1/7 nm menunjukkan keputusan yang cemerlang iaitu data kekal sebanyak 83% (16.6 V). Kemudian, bahan tinggi-k SiO_2/Al_2O_3 dan SiO_2/HfO_2 dipilih untuk menguji data ketahanan yang menunjukkan ketahanan data masing-masing kekal 82% dan 75% cas sehingga 10^4 kitaran P/E.

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LIST OF ABBREVIATIONS

BIOS	-	Basic input/output System
CG	-	Control Gate
CNT	-	Carbon Nanotube
DRAM	-	Dynamic Random-access Memory
EEPROM	-	Electrically Erasable and Programmable Read-only Memory
EOT	-	Effective oxide thickness
EPROM	-	Erasable and Programmable Read-only Memory
FET	-	Field Effect Transistor
FG	-	Floating Gate
FN	-	Fowler Nordheim
GO	-	Graphene Oxide
HEI	-	Hot Electron Injection
ITRS	-	International Technology Roadmap for Semiconductor
MLG	-	Multi-layer Graphene
MOSFET	-	Metal-oxide-semiconductor Field Effect Transistor
NVM	-	Non-volatile Memory
P/E	-	Program and Erase
RAM	-	Random-access Memory
rMLG	-	Reduced Multi-layer Graphene
ROM	-	Read-only Memory
SILC	-	Stress Induced Leakage Current
SiNW	-	Silicon Nanowire
SLG	-	Single-layer Graphene
SRAM	-	Static Random-access Memory
TaN	-	Talanum Nitride
VARIOT	-	Variable Oxide Thickness

LIST OF SYMBOLS

Φ_B	-	Barrier height
ε_0	-	Permittivity free space
ε_{hk}	-	Dielectric constant
χ	-	Electron affinity
μ_n	-	Electron mobility
μ_p	-	Hole mobility
ΔV_T	-	Difference in threshold voltage
$\Delta V_{T,final}$	-	Difference in threshold voltage for final
$\Delta V_{T,initial}$	-	Difference in threshold voltage for initial
A_{FN}	-	FN coefficient
Al_2O_3	-	Aluminium Oxide
B_{FN}	-	FN coefficient
E	-	Electric field
E_g	-	Band gap
h	-	Planck's constant
HfO_2	-	Hafnium Dioxide
J_{FN}	-	Tunnel current density
m	-	Mass
m*	-	Effective mass
N_e	-	Number of electrons
q	-	Electronic charge
Q_{FG}	-	Floating gate charge
Si_3N_4	-	Silicon Nitride
t_{hk}	-	Thickness of high-k material
t_{ox}	-	Oxide thickness
V_T	-	Threshold voltage
W_F	-	Work function
ZrO_2	-	Zirconium Dioxide

CHAPTER 1

INTRODUCTION

1.1 Research Background

The nature of an innovation by contemporary product growth and opportunities facing next generation in electronics systems have become more complicated as the elements have become extremely integrated in both physical and functional characteristics. Placement of the number of transistors in a chip follows the traditional Moore's Law, invented by Gordon Moore, the founders of Intel, states that the numbers of transistors that can be placed on a chip will approximately double every 2 years, as can be seen in Figure 1.1 [1]. The law was invented in order to achieve low cost and able to accommodate more transistor in a chip while sustaining its high performance. As a result, since past few years, research has been working on shrinking down device dimension [2]. As a consequence, denser silicon integrated circuits can be realized which allows for integration of devices with many capabilities and added functionality. As a result, many high-technology electronics devices exist today [3].

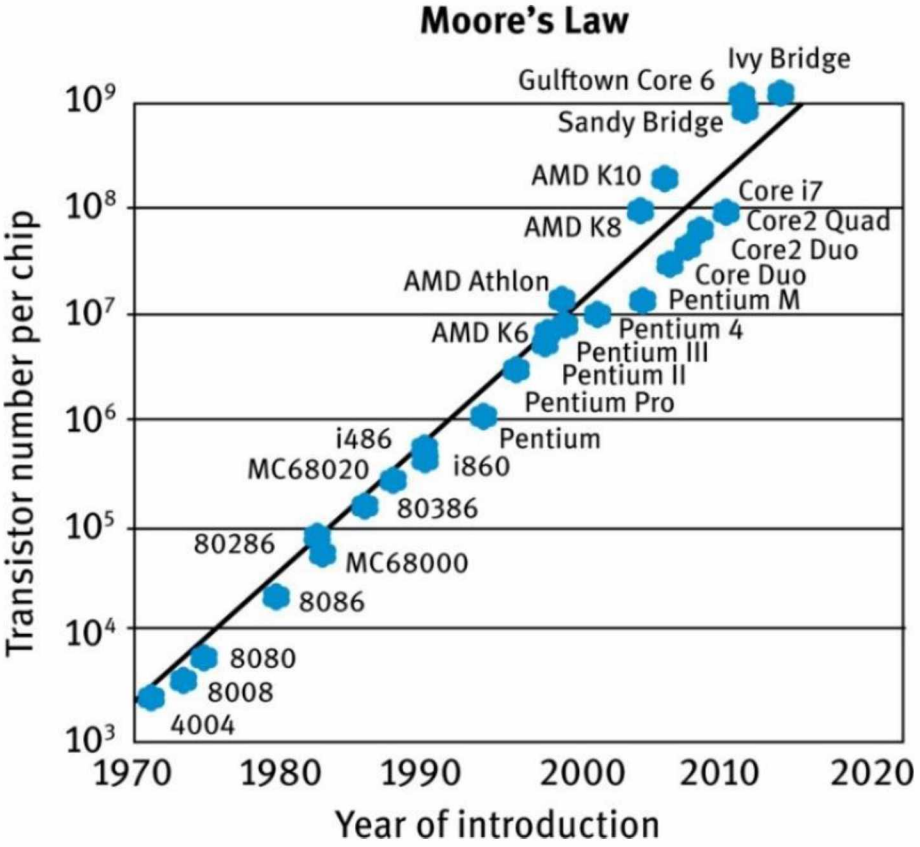

Figure 1.1 Semi-logarithmic plot of Moore's Law for number of transistors in microprocessors [1].

Memory technology is one of the highest demands to consumer and almost every electronic device utilizes the memory such as cell phones, computers, cameras and many more where the encoded data is stored and retained as digital information inside a memory device [4]. The trends of International Technology Roadmap for Semiconductor (ITRS) is illustrated in Figure 1.2 that showing the shrink of 0.7 times, in every 2 years and shows that the flash memory bit size is accelerated by one year compared to dynamic random-access memory (DRAM) [5]. Hard disk drives and flash memories are probably the most common form of non-volatile memory (NVM) due to their good reliability in term of its capability for smaller size footprint, high capacities and as well as relatively cheap production per byte (refer Figure 1.3) [6].

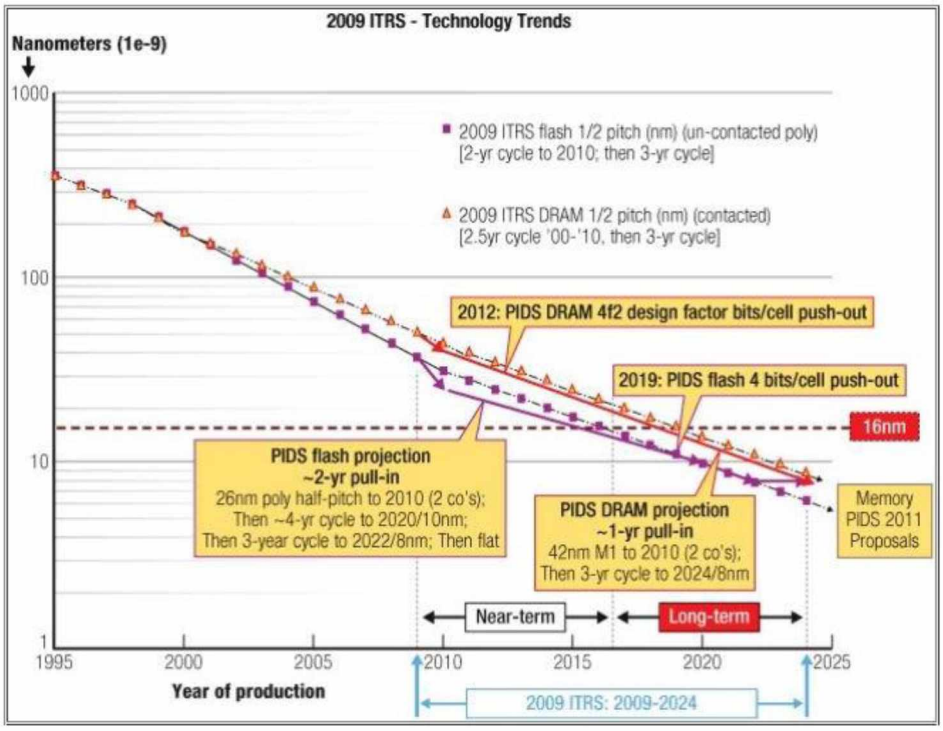

Figure 1.2 ITRS technology trends for memory technology [5].

The challenge of semiconductor industry is to produce absolutely small device while increase the performance to meets the consumer demands. Recently, introduction of non-silicon materials such as graphene and carbon nanotube (CNT) as field effect transistor (FET) channel seems to be the most promising solution [7].

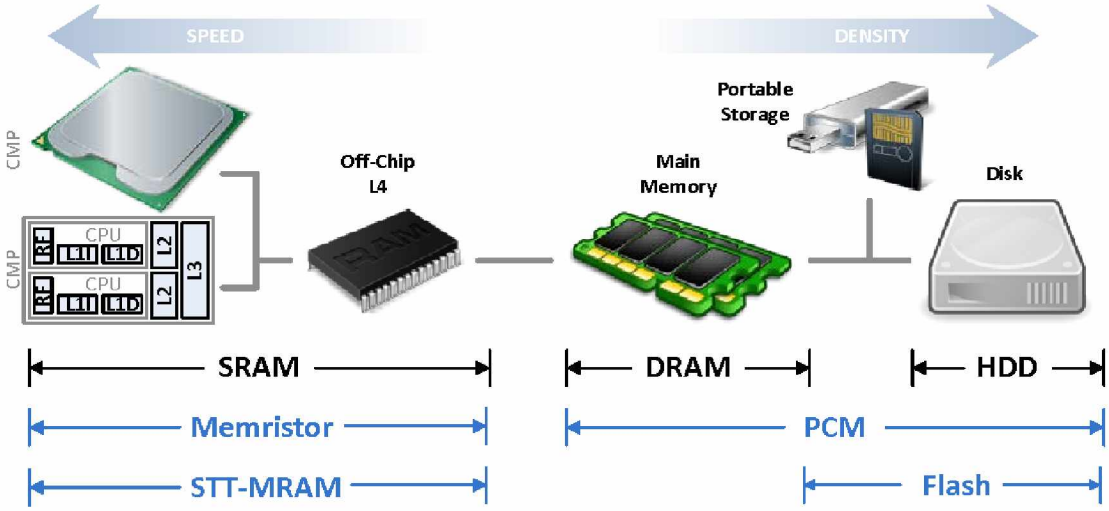

Figure 1.3 Memory technology [6].

In 2010, graphene resulted in a noble prize in physics and became a phenomenal growth in terms of published research. Graphene has potential to become one of the strongest candidates for post-silicon in the next generation of electronic and energy application because of its excellent in electronic, mechanical, chemical and optoelectronic properties [8]. Graphene could be ideal for utilize in future electronics applications because of the electrons can transport through the material at extremely in high speed and behave like relativistic particles with no rest mass [9]. These remarkable properties of graphene, such as high carrier mobility, thermal conductivity, mechanical flexibility and optical transparency, make it a highly promising material for future electronics and would be acceptable for production for solar cells, touch screens and light panel [10, 11].

Recently, high speed logic computing through device scaling, increasing number of electronic consumer and information technology have demanded for higher data storage capability. Flash memory technology has recently gained much attention with the growing demand of non-volatile memories for mobile electronic devices [12]. Researchers at Seoul National University and the Gwangju Institute of Science and Technology, South Korea, have fabricated organic memory devices that feature multilayer graphene film sandwiched between insulating polyimide layers with the embedded multilayer graphene film acting as a charge-trapping layer which having a fascinating result [9].

1.2 Problem Statement

The scaling of the semiconductor component sizes is crucial due to the growing needed for smaller sizes, faster computing capabilities, and lower power consumption [13]. Scaling is referring to the continued reducing the horizontal or vertical physical component sizes of the on-chip logic to overcome the reliability issues including increase the density and performance speed, reduce power and reduce cost [14]. However, the scaling of silicon-based technology is leading to an unfavourable bottleneck in the coming nano-technology era [15].

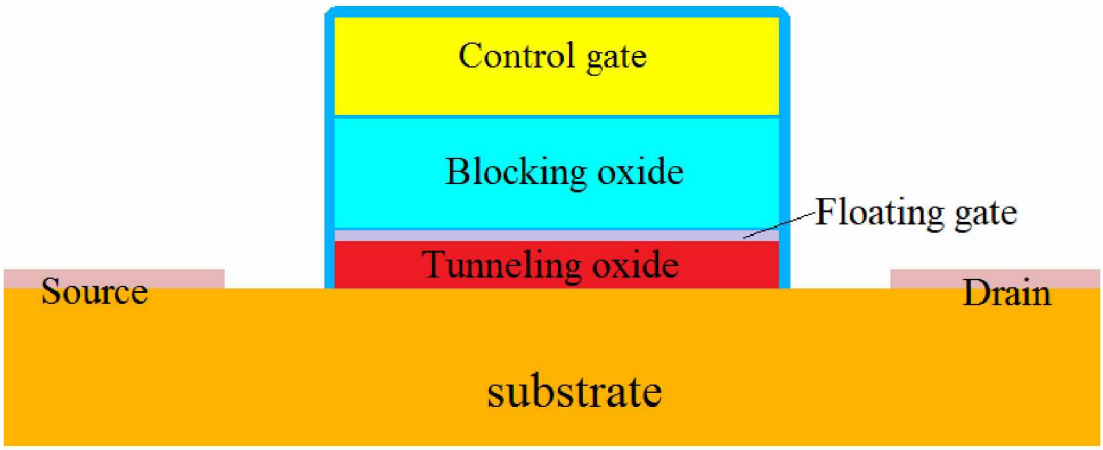

Figure 1.4 Basic concept of floating gate (FG) memory cell device structure.

The limitation of scaling in silicon-based technology has faced many challenges in the FG memory cell (Figure 1.4). Continuous decreasing the thickness may lead to defect in the dielectric layer which may generate device failure and reliability concerns and most crucial factor is that high operating voltages and high leakage currents [16].

Conventionally, SiO_2 (silicon dioxide) has been operated as a tunnel barrier layer for flash. Nevertheless, the major limitation of scaling the SiO_2 below the conventional thickness are issues in programming and erasing, memory window (MW) and retention trade-off due to stress induced leakage current (SILC) [17]. Further scaling of SiO_2 beyond 10nm brings problems as the gate oxide gets thinner because of quantum mechanical tunnelling of carriers through such a thin SiO_2 layer. The leakage current not only reduces the reliability of the device, but also creates oxide defects after repeated cycles of operation [18]. However, there are some major issues regarding to fabrication process which formed a mixture of metal and semiconductor and behaves in metallic manner. Further studies still undergoing to replace acceptability and suitability of material as FET channel. Fabrication process may involve a higher cost and time consuming. Therefore, simulation studies are one of a suitable choice as an alternative to investigate the characteristics of a new material especially graphene before actual fabricated and produced to the industries [7].

1.2.1 Tunnel barrier scaling issues

Flash memory requires approximately 15V to 20V biases for device operation. Scaling tunnel dielectrics generates higher electrical stress resulting defects in the gate stack. However, probability of electrons tunnelling in or out will increase exponentially and stored charges can easily leak into the channel resulting the flash cell may reduce both endurance and retention performance [18]. Figure 1.5 shows the scaling thin tunnel oxide below 4 nm resulting higher charges leakage due to direct tunnelling dominates to the tunnel dielectric compared to when thick tunnel oxide of 6-7 nm is used, tunnelling of electrons happens mostly by Fowler-Nordheim (FN) tunnelling. In conclusion, tunnel dielectric scaling creates better program and erase (P/E) and MW for the same P/E voltage, however, the retention is affected poor [19].

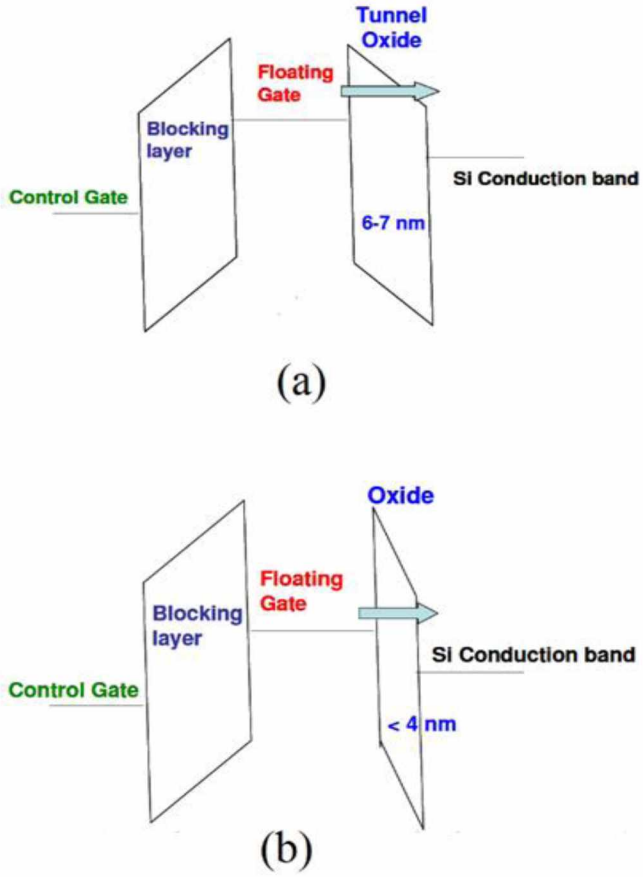

Figure 1.5 (a) Tunnel oxide of 6-7 nm and (b) tunnel oxide of less than 4 nm flash memory cell [19].

1.2.2 Graphene as floating gate issues

Graphene also have the remarkable properties such as high carrier mobility, mechanical flexibility as well as thermal conductivity which make it an optimistic material for hereafter electronics [9]. There has been interested in utilising graphene for faster and lesser energy-consuming in NVM in industries [20]. The MW and data retention analysis are important in determining the memory cell performance. However, there is lack of analysis on the memory characteristics for graphene-based FG memory cell due to graphene application is still new in memory cell. To discover more the unique behaviour of graphene in a memory cell, simulation and deep analysis will be performed to investigate the reliability of a single graphene-based memory cell on MW and data retention. The hypothesis on different number of layer and memory performance is still inconclusive. There are few variabilities works that have been done by previous researchers on different number of a graphene layer FG memory cell, however, the optimum number of graphene layer in FG memory cell is still questionable.

Table 1.1 Previous works on the graphene-based FG memory [12, 21-24].

Researcher	**Number of layers**	**MW (V)**	**Electron density, n_e (cm^{-2})**	**Data retention after 10 years**
A. J. Hong (2011) [12]	SLG: single-layer MLG: unmentioned	SLG: 2 MLG: 6	unmentioned	MLG: Only 8% data loss
A. Mishra, (2012) [21]	MLG of 6-7 layers	MLG: 6.8	9.1×10^{12}	unmentioned
S. Bertolazzi, (2013) [22]	MLG of 4-5 layers with additional SLG at channel	8	2.8×10^{13}	Only 30% data retains
A. Mishra, (2014) [23]	MLG: unmentioned	9.4	1×10^{13}	74% data retains
W. J. Liu, (2015) [24]	single-layer	5.6	unmentioned	unmentioned

Table 1.1 summarizes the previous work in graphene-based flash memory cell in past 10 years. The introduction to multi-layer graphene (MLG) as FG in flash memory structure may cause to increase the electron density compared to single-layer graphene (SLG) which is capable for storing number of charge accumulation in FG and also can lead to achieve large MW [16]. However, there are limited study on memory reliability on graphene flash memory and also the architecture for graphene layer as the FG is still undergoing research. Therefore, the variability simulation of memory reliability on graphene is choose to overcome some issues regarding the limitation graphene sources and equipment and also, the simulation can reduce time consuming and cost. Using this idea, the variabilities can occur on simulation for variability oxide thickness (VARIOT), P/E volage, data retention and endurance.

The introduction of VARIOT which referred to high-k material as tunnel layer becomes one of outstanding solution. A lot of research studies regarding VARIOT stack is found to have a high field sensitivity compared to single SiO_2 layer resulted in shorter P/E time, lower P/E voltage as well as less leakage in long-term retention time. However, due to high-k optimization of high-k dielectric materials based on their characteristics, the physical thickness of VARIOT considered thicker tunnel oxide compared with SiO_2 layer which expected degrading the P/E performance for memory devices.

1.3 Research Objective

The significant contributions in this research can be highlighted as follow:

1. To simulate and analyses the memory performance characteristics of graphene-based FG flash memory cell in terms of data retention and data endurance by using Silvaco TCAD Tools.

2. To analyse the reliability of graphene-based FG memory cell by using Variable Oxide Thickness (VARIOT) combination with different high-k materials in terms of data retention and data endurance.

1.4 Scopes of study

The scopes of this research involve the simulation of the graphene FG flash memory; from virtually fabricate the FG flash memory to analyzation of their memory performances. The simulation will be done by using Silvaco TCAD Tools. The structure parameters of a graphene FG flash memory cell which includes thickness, doping, band gap and others are determined by referring to the published data from [23-25]. The dimensions of device are shown in Table 1.2 and the voltage biases is from -14V to -20V for erasing and 14V to 20V for programming.

Table 1.2 Device dimension for graphene FG flash memory cell [23].

Gate length, L_G (nm)	600
Tunnel oxide thickness, t_{ox} (nm)	8 (SiO_2)
Blocking oxide thickness, t_{IPD} (nm)	22 (Al_2O_3)
FG thickness, t_{FG} (nm)	5
Control gate thickness, t_{CG} (nm)	15 (TiN)

The analysation of P/E operation, MW, data retention and also data endurance are validated with the previous work of [23]. The literature review was performed to understand the physical mechanism and electrical characteristics of graphene including graphene properties, current-voltage (I-V) characteristics, P/E operation with both models of hot electron injection (HEI) and Fowler-Nordheim (FN) tunnelling model. Introduction of high-k materials into tunnel barrier using VARIOT will be more interesting to the performance of flash memory. The tunnel barrier engineering (TBE) in flash memory using asymmetric structure (low-k/high-k) using SiO_2 as low-k and Aluminium Oxide (Al_2O_3), Silicon Nitride (Si_3N_4), Hafnium Oxide (HfO_2) and Zirconium Oxide (ZrO_2) as high-k for tunnel barrier oxide in flash memory cell to study the data retention and data endurance.

1.5 Research Contribution

The research contributions in this study can be highlighted as follow:

1. *VARIOT Optimization*: The optimization of VARIOT tunnel layer for multiple high-k dielectric materials where asymmetric combination of low-k/high-k stack is performed to determine the best asymmetric combination with optimum effective oxide thickness (EOT) and oxide thickness (T_{ox}).

2. *Graphene floating gate with high-k tunnel barrier*: Introduction of graphene-based material with high-k tunnel oxide show the best combination in flash memory cell to improve the P/E characteristics, its data retention as well as its data endurance.

1.6 Thesis Organization

This research study is conducted through simulation method and divided into 5 chapters. Chapter 1 is where to memory device background and development are discussed starting with types of memory, their importance in industry and demand to technology. Then, flash memory issues and challenges are highlighted in which the research's problem statements are determined. Based on the problem statements, the objectives of the research are proposed and the scope of the work has been identified. Finally, the research contributions have been highlighted and summarized in this chapter.

Chapter 2 is discussed on literature review of research on flash memory technology which discussed the graphene-based memory cell of flash memory structures are identified and its characteristics are being highlighted. The fundamentals of graphene material are discussed including the graphene properties and its demand to future technology. Furthermore, the concept of tunnel barrier engineering is discussed including introduction on high-k material that applied on the memory cell are explained.

Chapter 3 explained to the methodology of research including flow chart, equation, parameter and validated work from previous review. This chapter covers the research method of this work on simulation for validation from previous research. The research simulation work in this chapter are presented such as dielectric material, device dimension and other parameters. Lastly, the flow to characterize the memory device's reliability is summarized in the flowchart and discussed analytically.

Chapter 4 which result and discussion are demonstrated. The simulation results are presented and discussed in detail which includes the P/E characteristics, data retention and data endurance with aided of figures and tables. The introduction of graphene-based floating gate with VARIOT in flash memory cell are explained with presence of high-k materials.

Finally, Chapter 5 conclude all the findings in this research and the research contributions are highlighted again. Future works of this work are proposed to make sure the continuation of the research and contributions to the society.

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LIST OF PUBLICATIONS

List of presented conference:

1. M. Hilman Ahmad, N Ezaila Alias, Afiq Hamzah, Zaharah Johari, M. S. Z. Abidin, Norlina Paraman, M. L. Peng Tan, Razali Ismail, (8 October 2019). Reliability of graphene as charge storage layer in floating gate flash memory. National Symposium on Micro-Nano Technology (NaSMiNT) 2019 organized by Ministry of Science, Technology and Innovation (MOSTI) at Malaysia Global Innovation & Creativity Center (MaGIC), Cyberjaya, Selangor.

2. M. Hilman Ahmad, N Ezaila Alias, Afiq Hamzah, Zaharah Johari, M. S. Z. Abidin, Norlina Paraman, M. L. Peng Tan, Razali Ismail, (28-29 November 2019). Reliability of graphene as charge storage layer in floating gate flash memory. 3rd International Conference on Electrical, Electronic, Communication and Control Engineering (ICEECC) 2018 organized by School of Electrical Engineering, Faculty of Engineering, Universiti Teknologi Malaysia (UTM) at KSL Hotel, Johor Bahru, Johor.

3. M. Hilman Ahmad, N Ezaila Alias, Afiq Hamzah, Zaharah Johari, MSZ Abidin, Razali Ismail, (26-28 November 2018). Graphene as Charge Storage Layer in Floating Gate Flash Memory with High-*k* Tunnel Barrier Engineering. IEEE Student Conference on Research and Development (SCOReD) 2018 organized by Multimedia University Malaysia (MMU) at Bangi Golf Resort, Bangi, Selangor.

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2. M. Hilman Ahmad, N Ezaila Alias, Afiq Hamzah, Zaharah Johari, MSZ Abidin, Razali Ismail, (2018). Graphene as Charge Storage Layer in Floating Gate Flash Memory with Highk Tunnel Barrier Engineering. 2018 IEEE Student Conference on Research and Development (SCOReD).