SCALABLE DIVERSIFIED ANTIRANDOM TEST PATTERN GENERATION WITH IMPROVED FAULT COVERAGE FOR BLACK-BOX CIRCUIT TESTING

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A thesis submitted in fulfilment of the
requirements for the award of the degree of
Doctor of Philosophy

School of Electrical Engineering
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SEPTEMBER 2022

DEDICATION

Dedicated to my beloved grandfather Manzoor Ahmed, father Mohammad Anwar Alamgir, mother Sajida Tabassum, wife Farheen Nisar and son Aahil Arbab and Mikaeel Arbab. Thank you for your love, support, and understanding.

ACKNOWLEDGEMENT

I would like to thank Allah for giving me the opportunity to undertake my studies far from home. Moreover, I thank **Prof. Dr. Abu Khari Bin A'ain** for his continuous guidance, tireless efforts, encouragement, and patience regarding this study. I am indebted for his support until the completion of my thesis.

My special gratitude is due to my supervisors **Dr. Norlina Paraman** and **Dr. Usman Ullah Sheikh** for their valuable advice and friendly help. Their critical reviews on my work and interesting suggestions have been constructive throughout this study.

I would like to thank Virginia Polytechnic Institute and State University for allowing us to have access to ATALANTA fault simulator which made this research work possible.

My special gratitude is due to my parents and my wife for their loving support. Without their encouragement and understanding, it would have been hard for me to achieve my research objectives.

I appreciate all my friends, especially Mohammad Idrees Masud, Umair Hassan, Usama Mansoor, Saddam Ansari, Najeeb-ur-Rehman, Zeeshan Anjum, Dr. Syed Hamid Husain Madni and Dr. Touqeer Jumani, who advised and encouraged me whenever it was difficult for me.

ABSTRACT

Pseudorandom testing is incapable of utilizing the success rate of preceding test patterns while generating subsequent test patterns. Many redundant test patterns have been generated that increase the test length without any significant increase in the fault coverage. An extension to pseudorandom testing is Antirandom that induces divergent patterns by maximizing the Total Hamming Distance (THD) and Total Cartesian Distance (TCD) of every subsequent test pattern. However, the Antirandom test sequence generation algorithm is prone to unsystematic selection when more than one patterns possess maximum THD and TCD. As a result, diversity among test sequences is compromised, lowering the fault coverage. Therefore, this thesis analyses the effect of Hamming distance in vertical as well as horizontal dimension to enhance diversity among test patterns. First contribution of this thesis is the proposal of a Diverse Antirandom (DAR) test pattern generation algorithm. DAR employs Horizontal Total Hamming Distance (HTHD) along with THD and TCD for diversity enhancement among test patterns as maximum distance test pattern generation. The HTHD and TCD are used as distance metrics that increase computational complexity in divergent test sequence generation. Therefore, the second contribution of this thesis is the proposal of tree traversal search method to maximize diversity among test patterns. The proposed method uses bits mutation of a temporary test pattern following a path leading towards maximization of TCD. Results of fault simulations on benchmark circuits have shown that DAR significantly improves the fault coverage up to 18.3% as compared to Antirandom. Moreover, the computational complexity of Antirandom is reduced from exponential $O(2^n)$ to linear O(n). Next, the DAR algorithm is modified to ease hardware implementation for on-chip test generation. Therefore, the third contribution of this thesis is the design of a hardware-oriented DAR (HODA) test pattern generator architecture as an alternative to linear feedback shift register (LFSR) that consists of large number of memory elements. Parallel concatenation of the HODA architecture is designed to reduce the number of memory elements by implementing bit slicing architecture. It has been proven through simulation that the proposed architecture has increased fault coverage up to 66% and a reduction of 46.59% gate count compared to the LFSR. Consequently, this thesis presents uniform and scalable test pattern generator architecture for built-in self-test (BIST) applications and solution to maximum distance test pattern generation for high fault coverage in black-box environment.

ABSTRAK

Pseudorawak tidak berupaya memanfaatkan kadar kejayaan corak ujian sebelumnya sambil menghasilkan corak ujian yang seterusnya. Banyak corak ujian berlebihan terhasil yang meningkatkan panjang ujian tanpa peningkatan yang ketara dalam liputan kesalahan. Sambungan untuk ujian pseudorawak adalah Antirandom yang mendorong corak berbeza dengan memaksimumkan *Total Hamming Distance* (THD) dan *Total Cartesian Distance* (TCD) bagi setiap corak ujian seterusnya. Walau bagaimanapun, algoritma penjanaan urutan ujian Antirandom cenderung kepada pemilihan yang tidak sistematik apabila lebih daripada satu corak mempunyai maksimum THD dan TCD. Akibatnya, kepelbagaian antara urutan ujian terjejas, menurunkan liputan kesalahan. Oleh itu, tesis ini menganalisa pengaruh jarak Hamming pada dimensi menegak dan mendatar untuk meningkatkan kepelbagaian antara corak ujian. Sumbangan pertama tesis ini adalah cadangan penghasilan algoritma corak ujian *Diverse Antirandom* (DAR). DAR menggunakan *Horizontal Total Hamming Distance* (HTHD) bersama dengan THD dan TCD untuk meningkatkan kepelbagaian di antara corak ujian sebagai penghasilan corak ujian yang maksimum. HTHD dan TCD digunakan sebagai metrik jarak untuk meningkatkan kerumitan pengiraan dalam penjanaan urutan ujian yang berbeza. Oleh itu, sumbangan kedua dalam tesis ini adalah cadangan kaedah carian penyusuran pepohon untuk memaksimumkan kepelbagaian antara corak ujian. Kaedah yang dicadangkan menggunakan bit corak ujian sementara mengikuti laluan yang menuju ke arah memaksimumkan THD. Hasil simulasi kesalahan pada litar penanda aras telah menunjukkan bahawa DAR meningkatkan liputan kesalahan sehingga 18.3% dengan ketara berbanding dengan Antirandom. Tambahan pula, kerumitan pengiraan Antirandom dikurangkan daripada eksponen O(2^n) kepada linear O(n). Seterusnya, algoritma DAR diubah untuk memudahkan pelaksanaan perkakasan untuk penjanaan ujian cip. Oleh itu, sumbangan ketiga penyelidikan ini adalah reka bentuk seni bina penjana corak ujian DAR (HODA) yang berorientasikan perkakasan sebagai alternatif kepada *linear feedback shift register* (LFSR) yang mempunyai elemen memori yang besar. Gabungan senibina HODA selari direka bentuk untuk mengurangkan bilangan elemen memori dengan menerapkan seni bina penghirisan bit. Ia telah dibuktikan melalui simulasi bahawa seni bina yang dicadangkan telah meningkatkan liputan kesalahan sehingga 66% dengan pengurangan bilangan get sebanyak 46.59% berbanding LFSR. Oleh itu, tesis ini memberikan seni bina penjana corak ujian yang seragam dan berskala untuk aplikasi *built-in self-test (BIST)* dan penyelesaian untuk penghasilan corak ujian jarak yang maksimum bagi liputan kesalahan tinggi di persekitaran kotak-hitam.

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LIST OF ABBREVIATIONS

AR	-	Antirandom
ART	-	Adaptive Random Testing
BIST	-	Built-In Self-Test
CD	-	Cartesian Distance
CUT	-	Circuit Under Test
DAR	-	Diverse Antirandom
FAR	-	Fast Antirandom
FC	-	Fault Coverage
FSCS	-	Fixed Sized Candidate Set
HAC	-	Horizontal Absolute Criteria
HD	-	Hamming Distance
HDL	-	Hardware Description Language
HODA	-	Hardware-Oriented Diverse Antirandom
HTHD	-	Horizontal Total Hamming Distance
IAR	-	Iterative Antirandom
LFSR	-	Linear Feedback Shift Register
MISR	-	Multiple Input Signature Register
OCRT	-	Optimal Controlled Random Testing
PRTG	-	Pseudo-Random Test Generation
RLTS	-	Random Like Testing Sequence
SAR	-	Scalable Antirandom
STPG	-	Scalable Test Pattern Generation
STUMPS	-	Self-test Using MISR and Parallel Shift
TCD	-	Total Cartesian Distance
THD	-	Total Hamming Distance
TL	-	Test Length
VAC	-	Vertical Absolute Criteria
VHD	-	Vertical Hamming Distance

VTHD - Vertical Total Hamming Distance

LIST OF SYMBOLS

$t_{i,j}$	-	j^{th}bit of i^{th} test pattern in the test sequence
N	-	Number of inputs to CUT
N1	-	Order of Stage 1 Parallel HODA architecture
N2	-	Order of Stage 2 Parallel HODA architecture
T	-	Test Sequence

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The race of innovation and technology development has shifted the trends from system on board to system-on-chip and system-in-package [1, 2]. According to International Technology Roadmap for Semiconductors (ITRS), the current technology is approaching less than 7nm with the ever-increasing density on a single integrated circuit ranging up to billions of transistors [3, 4]. Embedding billions of logical operations on a single platform with efficient utilization of resources and high-speed processing results in extremely complex integrated circuits. However, testing and verification is an essential step in the formulation of the very large scale integration (VLSI) realization process that increases production costs by up to 40% [5]. Furthermore, it is impractical to synthesize and propagate faults on each node of embedded circuits. Thus, efficient testing to optimize yield loss and defect levels may cause delayed delivery to the market. Over the past 30 years, various facets of fault modeling, detection and diagnosis, fault simulation, and design-for-test have been presented to optimize reliability and minimize testing time. However, the challenges in testing have been ever-increasing with the complexities of integrated circuits.

Electronic testing can be broadly classified into white-box and black-box testing [6-8]. White-box testing refers to the testing technique where test patterns are developed using the structural information of the circuit under test (CUT) [9-11]. Spurring from D-algorithm [12, 13], FAN [14], and PODEM [15, 16], test generation has evolved over the past 50 years, hitting the boundaries of quantum search algorithms and utilizing probabilistic correlations [11, 17]. Test development time may be high for a complex circuits but white-box testing successfully optimizes the test length (TL). Contrarily, black-box testing is identified as a testing technique where test

generation is carried out irrespective of the structural implementation of the CUT. Black-box testing successfully reduces the development time and preserves the intellectual property. Black-box testing reduces development time by generating test patterns without going into the structural details of the CUT. As a result, a number of test patterns may target the faults that have already been discovered. Therefore, the test lengths may lead to exhaustive limits in black-box environment [4, 5, 7]. This research explores the possibilities to minimize test pattern redundancy for highly effective test pattern generation in a black-box environment.

Speedy testing even throughout the production cycle is not sufficient to maintain modern reliability standards. Therefore, high performance embedded systems are equipped with highly reliable built-in-self-test (BIST) for on-chip test operations [18]. BIST is an economical approach to do on-chip test operations providing technical opportunities with hierarchical testing using an inherent test pattern generator and response analyzer. Moreover, BIST applications also include detection of mismatch and bit error rate measurements in wireless transmissions and communications [9].

Figure 1.1 shows a popular Self-Test using a multiple input signature register (MISR) and parallel shift register (STUMPS) architecture of BIST. Comprising of a linear feedback shift register (LFSR) and MISR, this architecture automatically generates test patterns and performs signature analysis, respectively. The test pattern generator loads the patterns in the scan chains, and responses are collected using a MISR. Consequently, the circuit is evaluated based on a comparison between MISR output and golden signature. Instigating the testing process, the quality of on-chip BIST test pattern generation has a considerable influence on the fault coverage (FC). Lower FC leads to elongated TL that increase test time. Moreover, read-only memory (ROM) storage of non-accessible test patterns may increase the test costs [9, 19-22]. Thus, major contribution of this research is to improve quality of on-chip test patterns generation by diversifying the test sequence using different distance metrics. As a result, this research presents a self-scalable distance-based test pattern generator for high FC in the black-box circuits.

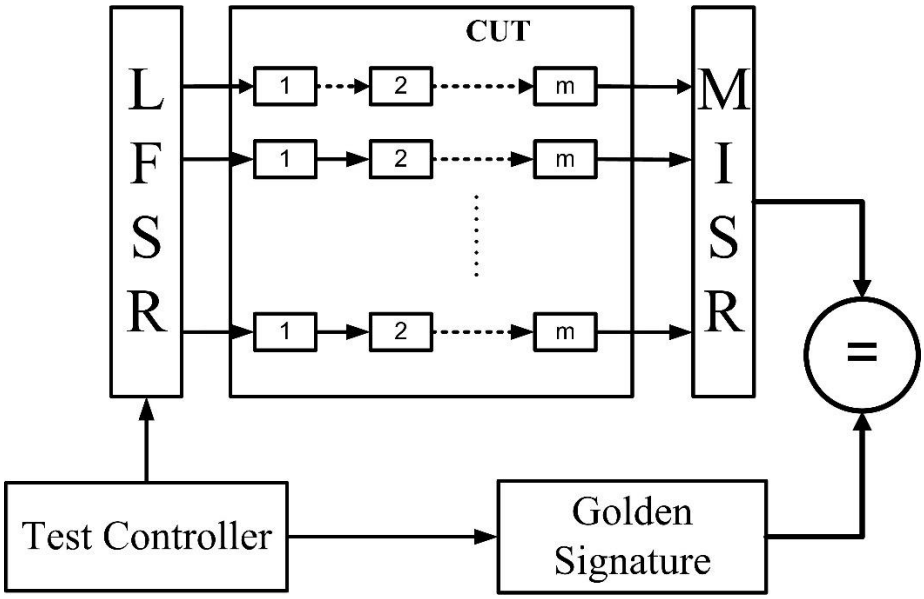

Figure 1.1 STUMPS architecture for BIST [9]

This thesis is an extension of the previous research work completed in the Master's thesis [23]. Previous research analyzes the improvements in the FC with the minimization of the horizontal distance metrics. Whereas, computational intensity due to total Cartesian distance (TCD) calculations increases exponentially with a linear increase in number of inputs to CUT. Moreover, the previous work reduces the computational intensity in the total Hamming distance (THD) calculations only. However, major part of computational overhead is experienced with the TCD calculations. This thesis extends the previous research to minimize computational overhead caused by TCD calculations for efficient test sequence generation. Moreover, hardware realization is taken into consideration for on-chip test sequence generation.

1.2 Problem Statement

Among the test pattern generation approaches to BIST, pseudo-random test generation (PRTG) is popular due to its ease of on-chip implementation using an LFSR [24-27]. PRTG generates test patterns using an equal probability for each pattern in the input space without replacement. PRTG significantly reduces the need to explore structural information of the CUT. Moreover, small memory requirement with low computational and hardware overhead makes PRTG an attractive choice for a test

pattern generator in the BIST architecture. PRTG outperforms other black-box test pattern generation approaches with its ability to automatically generate a large number of random patterns irrespective of the structural implementation of CUT [28, 29]. However, PRTG is unable to exploit all the information available in a black-box environment [22]. PRTG ignores the success or failure rate of the previously executed set of test patterns while generating subsequent test patterns. Lack of this ability may generate a number of subsequent test patterns targeting the faults that have already been detected [9, 19, 22, 23, 30, 31]. Thus, redundancy in test pattern generation increases the TL without any significant increase in the FC. Consequently, FC saturates at an early stage of testing with deterministic testing taking over to achieve satisfactory levels of FC.

Researchers have proposed several methods to overcome the inefficiency of PRTG. Weighted random testing uses a various set of weights to increase the probability of specific inputs [24, 32, 33]. Combinational logic is inserted between the test pattern generator and CUT to increase the probability of required inputs. However, the combinational logic overhead of weighted random testing is high for larger CUTs. Mixed-mode BIST uses the seeding of deterministic test patterns to increase the performance of PRTG [34, 35]. On the fly, reseeding inverts the logic values at the output of LFSR to modify next states targeting deterministic patterns [36]. The circular self-test scheme connects the primary input and output through a response analyzer forming circular feedback [37, 38]. Despite dense research around weighted random and mixed-mode BIST techniques, these methods are inefficient in the reduction of LFSR sizes and control logic overhead [24, 28, 39]. As a result, LFSR is loaded with additional hardware to facilitate high FC. Besides, LFSR itself is a significant contributor to the hardware overhead in a test pattern generator. The LFSR characteristic polynomial degree reflects the utilization of flip flops in the test pattern generator. This degree increases with the increase in the number of specified inputs required for the CUT [40]. Thus, an increasing number of primary inputs of CUT overloads BIST architecture with a proportional amount of hardware overhead. This research recognizes that Weighted random and Mixed-mode techniques seek to leverage the elegant simplicity of PRTG using LFSRs as a sequence generating device. However, LFSR is not necessarily the best sequence generating device if the goal is to generate high quality test patterns with low hardware overhead.

An extension to PRTG is Antirandom (AR), which tends to overcome test pattern redundancy by regular induction of divergent test patterns [19, 41-43]. Test sequence divergence exploits the contagious nature of faults in CUT and tends to increase fault detection by generating divergent test patterns. AR uses an analytical approach with distance metrics of THD and TCD to diversify test sequence generation. Consequently, subsequent test patterns are selected that maximize THD and TCD with all the previously generated test patterns. However, distance computation of every potential test pattern in the input space to maximize THD and TCD is a computationally intensive process, restricting the scalability of AR.

Random like testing sequence (RLTS) is an alternate approach to divergent test sequence generation that selects a random test pattern and maximizes the THD for subsequent test patterns [44]. This type of test pattern generation leads to the maximization of THD only and a random selection is carried out instead of TCD maximization [45]. Fast Antirandom (FAR) suggests a test pattern generation techniques based on centralizing method and orthogonal selection [46]. FAR centralizes the previously chosen test patterns by taking the average of each input and finds an orthogonal test pattern to the centralized pattern. FAR is best applicable in generating a test sequence for an existing random set of seed test patterns. However, the quality and quantity of the random seed patterns highly effects the FC.

Adaptive random testing (ART) overcomes the computational complexity by randomly selecting a number of test pattern candidates from the input space and computes only those for maximum TCD and maximum THD [47, 48]. As a result, the issue of scalability by introduction of a fixed distance approach. STPG avoids TCD calculations by using an adding factor to generate subsequent test patterns [49]. However, no guidelines are provided for the selection of the adding factor to increase fault detection. Shiyi Xu proposes a quasi-best distance approach that uses a predetermined distance to generate subsequent test patterns instead of maximizing the TCD [50]. However, according to the sphere-packing bound or hamming bound, a small number of test patterns are available if the predetermined distance is high and vice versa. Scalable Antirandom (SAT) proposes a bit swapping technique after every 2^n cycles of each input [31]. Iterative Antirandom (IAR) amplifies the fault detection

by proposing localized distance metric maximal minimal HD [51]. IAR suggests maximization of maximal minimal HD for a given length of testing sequence. Following this method controlled random testing generates short test sequences using predetermined lengths of $q = 2, 3$ and 4 test patterns [52]. Recently, Optimal controlled random tests with short lengths of $q = (\log_2 N + 1)$ are proposed for an N-input CUT [19]. Optimal controlled random tests (OCRT) are repeatedly generated for random test patterns to form a complete test set.

All the above approaches show an effort in minimizing the exponentially increasing computational overhead caused by the TCD computations. However, the effort to circumvent TCD computations results in compromised diversity in test sequence leading to lower FC. Furthermore, none of the distance-based algorithms present hardware architecture for on-chip BIST test pattern generation. This research firstly focuses on increasing the diversity among test patterns by introducing an additional distance criteria. Secondly, this research focuses on linearizing the computational complexity and increasing the FC at the same time. All the above issues point to a glaring research gap which needs to be answered from these questions:

1) As distance-based test sequences tend to increase fault detection. Is it possible, to introduce a new distance metric to further enhance FC?
2) Is it possible to linearize the TCD computations without compromising on the diversity among the test patterns.
3) Would the hardware realization of the divergent test generation incur less silicon area compared to traditional LFSR?

1.3 Objectives

The following are the objectives of this research work.

1) To analyze AR test sequence generation with an additional distance metric of horizontal total hamming distance (HTHD) for an average at least 3% higher FC in black-box circuits as compared to AR.
2) To propose a Diverse Antirandom (DAR) algorithm based on HTHD, THD and TCD for divergent test sequence generation with the linear O(n) computational complexity.
3) To propose a modular and structured hardware design approach for on-chip DAR using the bit-slice method for an average of at least 20% higher FC compared to conventional LFSR and an average of at least 40% reduction in gate count.

1.4 Scope of Work

Reliability analysis of integrated systems elongates throughout the backend system development equipped with failure analysis, fault tree analysis, and test development using structural implementations. However, this thesis is confined to the study of test pattern generation in the black-box environment where the test sequence is independent of structural implementation. This thesis is focused on developing a test pattern generation algorithm to generate a divergent test sequence for high fault in a black-box CUT. Verification of the proposed test pattern generation algorithm is carried out for all types of single stuck-at faults: stuck-at-0 and stuck-at-1 on the combinational profiles of ISCAS'85, ISCAS'89, and ITC'99 benchmark circuit to eliminate any biases. Afterward, the hardware realization of the proposed algorithm is carried out with a comparison of FC with an LFSR test sequence. The scope of this thesis is summarized as follows:

1) Single stuck-at-faults: stuck-at-0 and stuck-at-1 were considered in combinational profiles of benchmark circuits to evaluate the effectiveness in terms of fault detection.
2) AR is used as a basis for divergent test sequence generation as it is proved effective for high FC. The proposed technique extends the ideology of diversity among test patterns keeping AR distance metrics intact.
3) The effectiveness of the developed test suits is analyzed on combinational profiles of ISCAS'85, ISCAS'89, and ITC'99 benchmark circuits. This list of benchmark circuits provides an extreme challenge to the test pattern generator's scalability and eliminates all seed pattern biases.
4) Gate level fault simulation is carried out using ATALANTA 2.0 that uses all single stuck-at-faults to analyze the effectiveness of the input test sequence.
5) High-level MATLAB programming is utilized as a tool for algorithm implementation, distance calculations, and corresponding test file generation.
6) Quartus tools are used for the hardware realization and testing of the proposed test pattern generation algorithm.
7) A seed value of all ones test pattern is chosen to analyze the efficiency of test sequences.

1.5 Research Contributions

This thesis has significant contributions to the improvement of test pattern generation as follows:

1) The first contribution of this research is the proposal of the an additional distance metric of HTHD to enhance diversity among test patterns for higher FC in black-box.
2) The second contribution of this research is the proposal of a linearly complex O(n) DAR test pattern generation algorithm that employs HTHD along with TCD and THD without compromising on FC achieved by AR.
3) The third contribution of this research work is a hardware-oriented diverse Antirandom (HODA) test pattern generator architecture as an alternative to

LFSR. Consequently, this research presents a modular, structured, bit-slice approach for test pattern generation architecture for BIST applications.

1.6 Thesis Overview

This thesis is organized into six chapters. Chapter 1 provides the background and basics of testing leading to the problem statements and objectives of this research work. Moreover, this chapter defines the scope of the study and highlights the contributions of this research.

Chapter 2 of this thesis provides a summary of the critical literature review. This chapter discusses the different test pattern generation techniques for diversity enhancement. Moreover, this chapter explores the deterministic test pattern generation techniques for higher FC. Thus a platform is set for the proposed enhancements in test generation.

Chapter 3 of this thesis discusses the flow of this research. This chapter presents the development process of the proposed algorithm and test pattern generator architecture for high FC. Moreover, this chapter discusses the fault simulation set up to analyze the effectiveness of the proposed algorithm.

Chapter 4 is a detailed discussion on the proposed test pattern generation algorithm, along with its computational intensity. Moreover, this chapter extends the research with the hardware realization of the proposed test pattern generation algorithm.

Chapter 5 presents a detailed discussion of the fault simulation result for the proposed test pattern generation algorithm. A comparative analysis is carried out to prove the effectiveness of the proposed approaches. Lastly, a summary of this research and future recommendations are presented in Chapter 6.

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LIST OF PUBLICATIONS

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2. **Arbab Alamgir**, Abu Khari Bin A'ain, Norlina Paraman, Usman Ullah Sheikh, Mousa Mokji, Ian Grout. "*Multiple Controlled Antirandom Testing (MCAT) for high fault coverage in a black-box environment*." "IEEE Access," 7 (2019): 117246-117257.
3. **Arbab Alamgir**, Abu Khari Bin A'ain, Norlina Paraman, Usman Ullah Sheikh. "*Adaptive random testing with total cartesian distance for the black-box circuit under test*." "Indonesian Journal of Electrical Engineering and Computer Science." 20 (6) (2020)
4. **Arbab Alamgir**, Abu Khari Bin A'ain, Norlina Paraman, Usman Ullah Sheikh, Ian Grout. "*A comparative analysis of LFSR cascading for hardware efficiency and high fault coverage in BIST applications*." "Asian Test Symposium" November (2020).