

INTERFACIAL REACTIONS DURING SOLDERING OF Sn-Ag-Cu LEAD FREE
SOLDERS ON IMMERSION SILVER AND ELECTROLESS NICKEL/
IMMERSION GOLD SURFACE FINISHES

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To my beloved parents, sisters and brothers,
for their endless love, support and tolerance.

ABSTRACT

In the on-going trend towards miniaturization in the electronics packaging industry, the increasing popularity of ultra fine line technologies has brought into question the physical aspects of pad topography and metallization. As the solder joints shrink in size, the thickness of the pad metallization available can be very small, thus rendering close control of the soldering process and development of intermetallic compounds at the solder joint is essential. Interfacial reactions and the structure of intermetallics at the solder/substrate interface play an important role in solder joint reliability and the present study was undertaken to investigate these interfacial reactions in order to have a better understanding on the formation of reactions and their growth. In this study, interfacial reactions between Sn-4Ag-0.5Cu and Sn-3Ag-0.5Cu solders and immersion silver (ImAg) and electroless nickel/immersion gold (ENIG) surface finishes were investigated. Emphasis is made on the effect of solder size, subsequent ageing of solder joints on the interfacial microstructures. Several techniques of materials characterization including optical, image analysis, scanning electron microscopy and energy dispersive X-ray analysis were used to examine and quantify the intermetallics in terms of composition, thickness and morphology. It was found that after soldering on ImAg only scallop-type Cu_6Sn_5 layer was formed and that its thickness increases with decreasing solder size. Subsequent ageing produced a second layer of Cu_3Sn that forms between the Cu substrate and Cu_6Sn_5 layer. Growth kinetics showed that the Cu_3Sn layer grew at a faster rate than the Cu_6Sn_5 and that *Kirkendall voids* were also observed within this Cu_3Sn indicating that Cu diffuses much faster in the Cu_3Sn than Sn in the Cu_6Sn_5 . When soldering on ENIG finish, the reaction layer was found to consist of only one layer of $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ in the larger solders, while in the smallest solder (200 μm) both $(\text{Ni}, \text{Cu})_3\text{Sn}$ and $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ were formed. These results reconciled well with the current theory of a critical Cu concentration determining the type of intermetallic layer that would form. The Ag content in the solder also affected the nucleation and growth of Ag_3Sn plates as well as Cu-Sn intermetallic. Higher Ag containing Sn-Ag-Cu solder promoted growth of Cu_6Sn_5 rods and large Ag_3Sn plates. Subjecting the solder joint to isothermal ageing induced thickening and coarsening of the intermetallics as well as changed in their morphologies. The results showed that the thickness of intermetallics increases with increasing the duration of ageing for both solders investigated and for all solder sphere sizes.

ABSTRAK

Dalam menuju ke arah pengecilan dalam industri pembungkusan elektronik, peningkatan kepopularan teknologi ultra halus telah menimbulkan tanda tanya terhadap aspek fizikal topografi pad dan perlogaman. Sebaik sahaja saiz sambungan pateri mengecut, ketebalan perlogaman pad yang ada boleh menjadi kecil, maka ini menjadikan pengawalan tertutup proses pematerian dan perkembangan sebatian antara logam pada sambungan pateri adalah penting. Tindakbalas antara muka dan struktur sebatian antara logam pada pateri/ antara muka substrat memainkan peranan penting dalam keboleharapan sambungan pateri dan dengan itu, kajian ini dijalankan untuk menyelidik tindakbalas antara muka ini untuk mendapatkan pemahaman yang lebih baik terhadap pembentukan tindakbalas dan penumbuhannya. Dalam kajian ini, tindakbalas antara muka antara pateri Sn-4Ag-0.5Cu dan Sn-3Ag-0.5Cu dan kemasan permukaan *immersion silver* (ImAg) dan *electroless nickel/ immersion gold* (ENIG) telah diselidik. Penekanan diberikan kepada kesan saiz pateri, diikuti dengan penuaan sambungan pateri ke atas mikrostruktur antara muka. Beberapa teknik pencirian bahan telah digunakan untuk memeriksa dan menjumlahkan sebatian antara logam yang berkaitan dengan komposisi, ketebalan dan morfologi iaitu kaedah optik, analisis imej, *scanning electron microscopy* dan *energy dispersive X-ray analysis*. Didapati bahawa selepas pematerian ke atas ImAg, hanya lapisan Cu_6Sn_5 jenis *scallop* dijumpai dan ketebalannya meningkat dengan peningkatan saiz pateri. Proses penuaan menghasilkan lapisan kedua iaitu Cu_3Sn yang terbentuk di antara Cu di dalam substrat dan lapisan Cu_6Sn_5 . Kinetik pertumbuhan menunjukkan lapisan Cu_3Sn tumbuh dengan kadar yang lebih cepat berbanding Cu_6Sn_5 dan *Kirkendall voids* juga didapati terbentuk di dalam Cu_3Sn menunjukkan Cu meresap lebih cepat di dalam Cu_3Sn berbanding Sn di dalam Cu_6Sn_5 . Apabila pematerian ke atas ENIG dilakukan lapisan tindakbalas didapati terdiri daripada hanya satu lapisan $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ di dalam pateri yang besar manakala di dalam pateri yang kecil ($\text{Ø}200 \mu\text{m}$) kedua-dua $(\text{Ni}, \text{Cu})_3\text{Sn}_4$ dan $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ terbentuk. Keputusan ini bersesuaian dengan teori yang digunakan iaitu kepekatan Cu kritikal menentukan jenis lapisan sebatian antara logam yang akan terbentuk. Kandungan Ag di dalam pateri juga memberikan kesan ke atas penukleusan dan pertumbuhan kepingan Ag_3Sn dan juga sebatian antara logam Cu-Sn. Pateri Sn-Ag-Cu yang mengandungi Ag yang tinggi menggalakkan pertumbuhan rod Cu_6Sn_5 dan kepingan Ag_3Sn yang besar. Penuaan ke atas sambungan pateri menggalakkan peningkatan ketebalan dan pengasaran sebatian antara logam dan juga perubahan ke atas morfologinya. Keputusan menunjukkan ketebalan sebatian antara logam meningkat dengan peningkatan masa penuaan untuk kedua-dua jenis pateri dan kesemua saiz pateri logam yang dikaji.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Integrated circuit (IC) chips are the heart of electronic system controls, and since they are typically sensitive to electrical, mechanical, physical and chemical influences, they require special considerations by the packaging engineer. Today's circuit and system-level requirements of high performance, high reliability and low cost have placed greater demands on the packaging engineer to have a better understanding of the existing and emerging IC packaging technologies.

The number of input/output (I/O) pin count for high-end use is increasing all the time with decreasing package size. On these advanced high pin count chips, the electrode pads are arranged into an area array with narrow pad pitch and bumps are formed on each pad for flip chip interconnection. Assembly in flip chip interconnection is a direct electrical and mechanical connection face down of a bare die onto the printed circuit board (PWB) by means of solder bumps. As shown in Figure 1.1 the entire interconnection system consists of four parts: under bump metallurgy (UBM) on the die side, solder balls, and substrate metallization pad with top surface metallurgy (TSM). Both UBM and TSM provide adhesion, diffusion

barriers and protection layers. During assembly, and hence soldering, the solder melts and an intermetallic layer forms between the solder and metallurgy pads on both sides of the package.

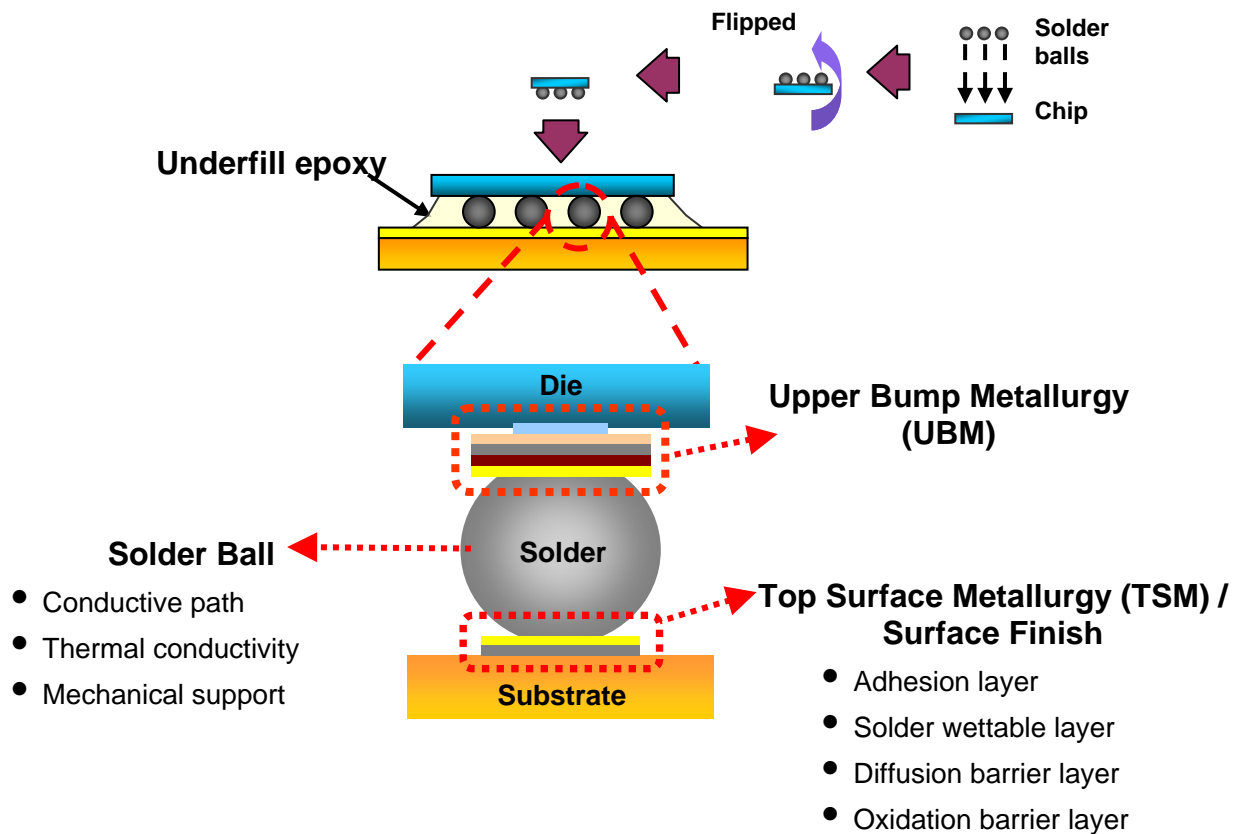


Figure 1.1: Schematic showing the main parts of an electronic package

The demand has recently increased for new bump formation technologies which enable the simultaneous formation of large numbers of bumps with a narrow bump pitch at low cost and short tact processing. However, some reliability issues may be arising from the utilization of smaller solder bump size.

Due to its excellent conductivity and surface for soldering, copper has been widely used as the substrate materials. However, several types of metal coating must also be deposited on copper surfaces as board finishes for the purpose of providing

wetting surfaces and protection against the environment. The selection of a metallurgical system (solder – top surface metallurgy) is very important because of its influence on the reliability of electronic assemblies. Typical surface finish metallurgy consists of two main layers: 1) a solderable layer in contact with the underlying copper and 2) a protective layer on top of the solderable layer. The purpose of the solderable layer is to provide the surface to which the liquid solder wets and then adheres upon solidification. This same solderable layer also acts as the diffusion barrier by preventing diffusion of the solder to the copper substrate. The protective layer serves to protect the solderability of the solderable layer from degradation due to exposure to ambient environment until reflow soldering occurs. During reflow the solder melts and the protective layer dissolves into the molten solder exposing in the process the solderable layer to the molten solder. The solderable layer now is also subjected to dissolution by the molten solder until solidification is complete. This results in the formation of an intermetallic layer between the solderable layer and solder. This intermetallic layer will grow in thickness during subsequent thermal ageing after assembly due to solid – solid reaction between the solderable layer and the solder by solid-state diffusion.

An important aspect of solder joint processing is a good understanding of the solder – substrate metallization reaction. The intermetallic layer, which develops from this reaction, is essential in order to achieve strong and reliable solder joints. However, excessive growth of this intermetallic layer may lead to degradation of solder joint reliability. Also the morphology of the intermetallic layer after soldering and subsequent solid-state thermal processes may also affect the reliability of the solder joint.

1.2 Field of Research

While the majority of surface finishes can be considered as multifunctional in nature, their primary function remains that of providing either solderability protection to the underlying copper basis material or to act as a solderable surface to which the solder joint will be formed. There are many factors that can influence the choice or rejection of a surface finish – cost, availability and even misinformation – but as a minimum a good surface finish should have or meet the following criteria: 1) It must have reasonable shelf-life; 2) It must be capable of withstanding multiple process steps; 3) It should be compatible with existing assembly equipment.

Among these board finishes, electroless nickel/ immersion gold (ENIG) has gained a significant level of interest in the last few years. This metal coating is deposited directly on copper to provide a diffusion barrier (to prevent copper dissolution in liquid solder), is very solderable, provides flat board finishes and protects against oxidation. Also, compared to other metals, growth of intermetallics between Ni and Sn is much slower. However, as the usage of ENIG increased, a problem of void formation which leads to brittle failure was found. These voids are also known as the Kirkendall voids. It is believed that these voids are formed because of the fast diffusion of Ni from the phosphorus rich nickel layer, which is a by-product layer of Ni-Sn interfacial reaction. This concern of voiding is further magnified with lead-free soldering. Thus, the search for a surface finish that produces high reliability of solder joints continues.

An ideal surface finish is still eluding most researchers and manufacturers especially with the imminent global usage of lead free solders. Thus, the need to find the most suitable and low cost surface finish has become necessary. Recently, silver coatings, including the new immersion silver coatings are used in numerous electronic components (Arra, M., *et al.*, 2003). This is due to its lower material cost, wire-bondable and silver coating itself does not melt, but instead, it dissolves into the molten solder, which may decrease the speed of wetting. Apart from that, immersion

silver can develop single element coating (which can reduce cost); result in relatively thin layers (typically less than $1\mu\text{m}$) because the deposition process halts when the substrate surface is completely covered with the coated material.

Based on the challenges discussed above, this research aims at understanding the interfacial reactions occurring during soldering and subsequent thermal ageing between different lead-free solders and different surface finishes metallurgies. Many research studies have been performed on the interfacial reactions between lead-free solders and various surface finish metallurgies, such as Cu, and ENIG but very little research has been done on immersion silver finish and thus knowledge on interfacial reactions during reflow and ageing is lacking. The current research addresses in particular the effect of solder bump sizes, solder composition, and thermal ageing on the type, size and morphologies of intermetallics formed on immersion silver (ImAg) and electroless nickel/immersion gold (ENIG) finishes. The solder alloys investigated are Sn-4Ag-0.5Cu and Sn-3Ag-0.5Cu with spheres having diameters of 700, 500, 300 and 200 μm . In order to quantify the effect of temperature on the growth of intermetallics the solder joints formed after reflow are subjected to thermal ageing at 150 °C for up to 2000 hours. To address the above issues and achieve the research aims reflow soldering experiments have been conducted and several characterization techniques were used in including, optical microcopy, image analysis, scanning electron microscopy (SEM) and energy dispersive X-ray analysis (EDX). Special focus will also be on the formation and growth of interfacial voids and their influence on the reliability of solder joints.

1.3 Objectives of the Research

The followings are the objectives of the project:

- To identify the types of intermetallic compounds formed during the interfacial reaction between lead-free solders and several surface finish metallurgies, mainly electroless nickel/immersion gold (ENIG) and immersion silver (ImAg).
- To quantify the effect of solid state ageing duration on the formation and growth of intermetallics both at the solder/ substrate interface and bulk solder.
- To establish the effect of solder bump size, Ag concentration of the solder alloy and reflow soldering time on the interfacial reactions.

1.4 Scope of the Research

The project consists of two main tasks:

1. Deposition of the surface finish, ENIG and ImAg. This task will involve the use of the electroless and immersion plating processes to deposit the desired thickness of the finish layers on a copper substrate.
2. The second task aims at conducting experimental work of soldering between liquid lead-free solder on the two surface finishes described above and evaluate the effect of factors such as, solid state aging, reflow soldering time and cooling rates on the formation and growth of intermetallics both at the solder/ substrate interface and bulk solder. Characterization will involve the type, morphology and thickness of intermetallics as well as the volume fraction of these intermetallics both at the interface and bulk solder.

1.5 Importance of the Research

In this research, we will try to obtain more knowledge on a new kind of surface finish, the immersion silver (ImAg) with lead free solders, i.e., Sn-4Ag-0.5Cu and Sn-3Ag-0.5Cu. Other parameters will also be taken into consideration like the sizes of the solder ball, i.e., 200 μ m, 300 μ m, 500 μ m and 700 μ m. ENIG also will be conducted in this research as a comparison to IAg. We would also study the effect of different ageing time on the solder joints such as 0 hour, 250 hours, 500 hours, 1000 hours and 2000 hours. We hope that the results from this research would provide a clearer view of what is happening in the solder joint and to what extent the intermetallics may become detrimental to the solder joint so that more consideration factors for future design and material selection could be provided.

1.6 Structure of the Thesis

This thesis comprises five chapters. Chapter one is an introduction in which problem statement, objective of the research and scope of work are presented. The literature review is divided into three parts. Part one is presented in chapter two which covers the basics on electronic packaging and methods of bonding such as flip chip bonding, wire bonding and tape automated bonding. The second part of literature review is in chapter three and covers the surface finish systems for TSM, coating technology and plating techniques. Whereas the third part of literature review (chapter four) discusses the soldering methods as well as the intermetallic compounds formation in the solder joint during soldering. In chapter five, the detailed experimental procedure and techniques employed in the current research are presented and discussed. In chapter six, results and discussion, the author presents all experimental results obtained and evidence to support them. Finally, in chapter seven, a set of conclusions and future work is presented.

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