LOW TEMPERATURE GROWTH OF ZINC OXIDE ON INSULATOR UTILIZING GRAPHENE BUFFER LAYER FOR TRANSFERABLE ELECTRONICS

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DEDICATION

To everyone

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ABSTRACT

Intelligent system-on-chip (SoC), which is the heterogeneous integration of devices on insulator/silicon (Si) platform and other arbitrary substrates, is considered as the most promising next-generation technology. Since the insulator and those arbitrary substrates are generally amorphous, the direct growth of crystalline semiconductor materials is extremely difficult. Hence, a breakthrough of clever growth technology is demanded. Zinc oxide (ZnO) is one of the promising metal-oxide materials for many device applications like sensors, optoelectronic devices, etc. Buffer or template layer has been widely utilized to reduce the large lattice mismatch between the grown materials and insulators or arbitrary substrates. In this study, graphene, which is flexible, transparent and possesses a similar hexagonal atomic arrangement structure to ZnO, was chosen as a buffer or template layer. Since most of the arbitrary substrates possess low- melting temperatures, the growth of ZnO had to be performed at low temperatures. Three low- temperature techniques were used; combination of thermal evaporation and oxidation, hydrothermal deposition and hot-water-beam chemical vapour deposition (CVD). For thermal evaporation, first, ZnO film with a thickness of ~350 nm was deposited, followed by oxidation treatment at 450°C in oxygen ambient. The oxidation times varied between 30 to 120 minutes. Oxidation of physically deposited ZnO was to minimize the oxygen vacancies or to increase the crystallinity of ZnO with the appearance of diffraction peaks corresponded to (0002), (10-10) and (10-11), and these peaks increased with the oxidation time up to 60 min. However, the peak intensity showed a decrease with broad FWHM of (0002) after 60 min of oxidation which was speculated to be caused by the intermixing of ZnO and graphene. For the hydrothermal process,which was carried at 90°C for 3 hours, a graphene/glass and a ZnO/ glass were used as the substrates. No growth of ZnO was obtained on graphene/glass. It was speculated that graphene with low defects might not promote the nucleation of ZnO. However, the growth of ZnO nanorods on ZnO-seeded was obtained with a considerable small FWHM of 0.2892° for the (0002) peak. However, the intensity ratios of the ultraviolet emission (I_{uv}) and visible emission (I_{vis}) for both ZnO grown by thermal evaporation combined with oxidation, and hydrothermal process were around 1.05. This suggested that defects or oxygen vacancies were still high. Finally, ZnO was grown on graphene/SiO_2/Si by hot water beam CVD with a growth time ranging from 20-60 min at a fixed substrate temperature of 500°C. As expected, a ZnO layer with high crystallinity (small FWHM of 0.0743°- 0.1955° for the (0002)) was obtained. Since the location of the 2θ of ZnO (0002) was close to the bulk value, this seemed to suggest less residual tensile stress compared to the other two methods. Extremely low defect of CVD-grown ZnO layer was also confirmed from I_{uv}/I_{vis} measurement, suggesting the potential for the device fabrication. The use of graphene as the buffer or template layer provides the potential for transferable electronics since the adhesion of graphene and substrate is extremely weak.

ABSTRAK

Sistem-pada-cip (SoC) pintar, yang merupakan peranti penyepaduan heterogen pada pelantar penebat/silikon (Si) dan substrat sebarangan yang lain, telah dianggap sebagai teknologi generasi-masa-depan yang memberangsangkan. Pertumbuhan langsung bahan semikonduktor kristal amat sukar disebabkan oleh penebat dan substrat sebarangan yang secara umumnya amorfus. Jadi, suatu kejayaan teknologi pertumbuhan yang bijak adalah dituntut. Zink oksida (ZnO) merupakan salah satu bahan logam-oksida yang menggalakkan untuk diaplikasikan pada banyak peranti seperti penderia, peranti optoelektronik, dan lain – lain. Lapisan penampan atau templat telah digunakan secara meluas bagi mengurangkan ketakpadanan kekisi yang ketara di antara bahan yang ditanam dan penebat atau substrat sebarangan. Dalam kajian ini, grafin, yang fleksibel, telus dan mempunyai struktur susunan atom heksagon yang sama dengan ZnO, telah dipilih sebagai lapisan penampan atau templat. Disebabkan kebanyakan substrat sebarangan mempunyai suhu lebur yang rendah, pertumbuhan ZnO perlu dilakukan pada suhu rendah. Tiga teknik suhu rendah telah digunakan; gabungan penyejatan terma dan pengoksidaan, pemendapan hidroterma dan alur air panas pemendapan wap kimia (CVD). Untuk penyejatan terma, pertama, filem ZnO dengan ketebalan ~ 350 nm diendapkan, diikuti dengan rawatan pengoksidaan pada 450°C dalam ambien oksigen. Masa pengoksidaan diubah, antara 30 hingga 120 minit. Pengoksidaan ke atas endapan fizikal ZnO adalah bagi meminimumkan kekosongan oksigen atau untuk meningkatkan kehabluran ZnO dengan mempamerkan puncak pembelauan yang sepadan dengan (0002), (10-10) dan (10-11), dan puncak-puncak ini telah meningkat dengan masa pengoksidaan sehingga 60 minit. Namun, keamatan puncak menunjukkan penurunan dengan FWHM (0002) yang lebar selepas 60 minit pengoksidaan yang dijangka disebabkan oleh percampuran diantara ZnO dan grafin. Bagi proses hidroterma, yang telah dilakukan pada suhu 90°C selama 3 jam, grafin/kaca dan ZnO/kaca telah digunakan sebagai substrat. Tiada pertumbuhan ZnO diperoleh pada grafin/kaca. Ini berkemungkinan disebabkan oleh kecacatan yang rendah pada grafin yang mungkin tidak merangsang nukleasi ZnO. Namun, FWHM yang kecil terhasil daripada pertumbuhan nanorod ZnO pada ZnO-biji iaitu 0.2892° bagi puncak (0002). Walau bagaimanapun, nisbah keamatan pancaran ultraviolet (I_{uv}) dan pancaran nampak (I_{vis}) bagi kedua-dua ZnO yang ditanam melalui gabungan penyejatan terma dan pengoksidaan, dan proses hidroterma adalah sekitar 1.05. Ini menunjukkan bahawa kecacatan atau kekosongan oksigen masih tinggi. Akhirnya, ZnO ditanam pada grafin/SiO_2/Si oleh alur air panas CVD dengan masa pertumbuhan diantara 20-60 min pada suhu substrat yang tetap, 500°C. Seperti yang dijangkakan, lapisan ZnO dengan kehabluran tinggi (FWHM kecil 0.0743°- 0.1955° bagi (0002)) telah diperoleh. Memandangkan lokasi 2θ ZnO (0002) berhampiran dengan nilai pukal, ini menunjukkan tegasan tegangan sisa yang kurang berbanding dengan dua kaedah lain. Kecacatan yang sangat rendah pada lapisan ZnO yang ditanam CVD juga telah disahkan daripada pengukuran I_{uv}/I_{vis}, menunjukkan potensi bagi fabrikasi suatu peranti. Penggunaan grafin sebagai lapisan penampan atau templat adalah berpotensi untuk elektronik terpindah kerana lekatan grafin dan substrat adalah sangat lemah.

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LIST OF ABBREVIATIONS

0D	-	Zero dimensional
1D	-	One dimensional
2D	-	Two dimensional
3D	-	Three dimensional
AFM	-	Atomic force microscopy
AI	-	Artificial intelligent
Ar	-	Argon
a-Si:H	-	Hydrogenated amorphous silicon
CdO	-	Cadmium oxide
CH_2O	-	Formaldehyde
CMOS	-	complementary metal-oxide-semiconductor
Cu	-	Copper
CuO	-	Copper oxide
CVD	-	Chemical vapor deposition
DI	-	Deionized
DLE	-	Deep level emission
DMZn	-	dimethyl zinc
EDX	-	Energy dispersive x-ray
FESEM	-	Field emission scanning electron
FET	-	Field effect transistor
FWHM	-	full width half maximum
GaAs	-	Gallium arsenide
GaN	-	Gallium nitride
Ge	-	Germanium
H_2	-	Hydrogen
H_2O	-	Water
hBN	-	Hexagonal boron nitride
HMTA	-	Hexamethylenetetramine
IoT	-	Internet of thing
IR	-	Infrared

ITO	-	Indium tin oxide
LP-MOCVD	-	Low-pressure metal-organic chemical vapor deposition
MBE	-	Molecular beam epitaxy
MgO	-	Magnesium oxide
MLG	-	Multilayer graphene
MOCVD	-	Metal-oxide chemical vapor deposition
MoS_2	-	Molybdenum disulphide
N_2	-	Nitrogen
N_2O	-	Nitrous oxide
NBE	-	Near band edge
NH_3	-	Ammonia
NH^{4+}	-	Ammonium
O	-	Oxygen (atom)
O_2	-	Oxygen (molecule)
O^{2-}	-	Oxygen ion
OH^-	-	Hydroxyl
PL	-	Photoluminescene
Pt	-	Platinum
PVD	-	Physical vapor deposition
rGO	-	Reduced graphene oxide
RF	-	Radiofrequency
RMS	-	Root mean square
RT	-	Room temperature
Si	-	Silicon
Si-ULSi	-	Silicon-ultra-large-scale
SiC	-	Silicon carbide
Si_3N_4	-	Silicon nitrate
SiO_2	-	Silicon dioxide
SLG	-	Single-layer graphene
TEM	-	Transmission electron microscope
ULSi	-	Ultra-large-scale integrated circuit
UV	-	Ultraviolet
UV-Vis	-	Ultraviolet-visible

vdW	-	Van der Waals
XRD	-	X-ray diffraction
Zn	-	Zinc
Zn^{2+}	-	Zinc ion
$Zn(CH_3)_2$	-	Dialkyl Zinc
$Zn(NO_3)_2.6H_2O$	-	Zinc nitrate hydroxide
ZnO	-	Zinc oxide
ZrO_2	-	Zirconia
ZnS	-	Zinc sulphide

LIST OF SYMBOLS

λ	-	Lambda
μm	-	Micrometre
°	-	Degree
°C	-	Degree Celsius
Å	-	Angstroms
a. u.	-	Arbitrary unit
cm	-	Centimetre
cm^2/Vs	-	Centimetres squared per volt-second
cm^{-1}	-	Per centimetre
cm^{-3}	-	Per centimetre cube
d	-	Interplanar spacing
eV	-	Electron volt
Hz	-	Hertz
I_{uv}/I_{vis}	-	Intensity of UV emission to intensity of green emission
meV	-	Milli-electron volt
min	-	Minute(s)
ml	-	Millilitre
mM	-	Millimolar
ms	-	Millisecond
n	-	Integer
nm	-	Nanometer
Pa	-	Pascal
sccm	-	Standard cubic centimetre per minute
W/mK	-	Watt per metre Kelvin
O_i	-	Oxygen interstitial
V_o	-	Oxygen vacancy
V_{Zn}	-	Zinc vacancy
Zn_i	-	Zinc interstitial
%	-	Percentage
θ	-	Angle

CHAPTER 1

INTRODUCTION

1.1 Research Background

People nowadays live in a modern era where the use of nano-sized silicon-based transistors has brought the realization of the Internet of Things (IoT) and artificial intelligence (AI) technology. The revolution of Silicon (Si) based transistor that kept growing over the years, together with the size reduction of the transistor, allowed the miniaturization of the transistor, which enables numbers of transistors to be crammed onto a single Si platform, thereby boosting computer capabilities. This obeyed Moore’s law, where the performance of silicon-ultra-large-scale integrated circuits (Si-ULSIs) has been improved over the last 30 years by doubling the number of transistors every two years on a single platform [1]. Today, a single processor can hold more than a trillion transistors [2]. However, the never-ending miniaturization of transistors makes winning more difficult due to limitations such as the short channel effect and gate leakage current.

The concept of advanced heterogeneous integration on a single platform has attracted much attention toward realizing a ‘More than Moore' technology [3]. In realizing such technology, the growth of various high-quality semiconductors such as germanium (Ge) [4], gallium arsenide (GaAs) [5], gallium nitride (GaN) [6], silicon carbide (SiC) [7], zinc oxide (ZnO) [8] on the platform is a must. The co-integration of materials enables the present ULSIs to be facilitated not only with ultra-high-speed complementary metal-oxide-semiconductor (CMOS) transistors and novel transistors [9] but also with various kinds of functional devices, such as optical devices [10], photodetectors [11], solar batteries [12], and sensors [13, 14]. Such intelligent system-on-chip (i-SoC) on Si is considered a promising and practical direction. To fabricate multi-functional devices on a single Si substrate, it is necessary to electronically isolate the semiconductor materials using insulators such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4) or arbitrary substrates. Figure 1.1 illustrates the evolution of Si in the 'More than Moore' [15]. However, the hybridization of high performance of semiconductors and insulators is impossible due to the amorphous structures of the insulators. Therefore, it needs some significant development in growth technology.

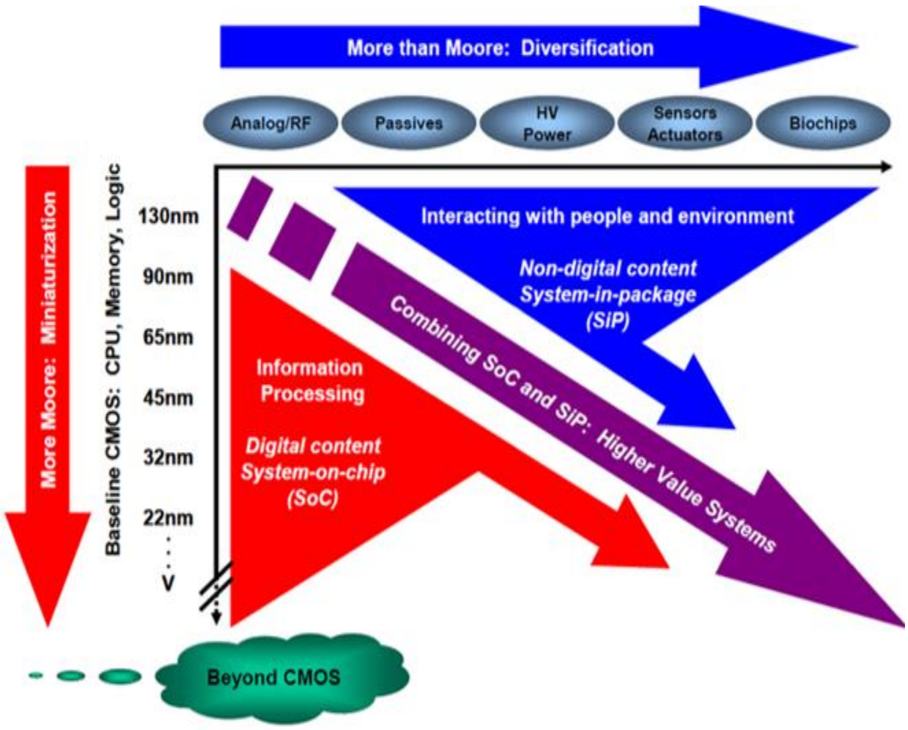

Figure 1.1 Evolution of Si in 'More than Moore' [15]

In the meantime, the use of insulators or arbitrary substrates such as polymers, rubber, and glass to fabricate the devices has become phenomenal today. Some of the devices are widely used in optoelectronics [16-18], sensors [19-21], and photovoltaic [22, 23] industries. Several advantages include simple, environmentally friendly, yet cheap materials suitable for the fabrication of commercial devices. Besides, other physically unique and eye-catching features like flexibility, transparency, and colourful are added values for device production on these arbitrary platforms. However, it still needs technology to breakthrough in fabricating semiconductor devices on these platforms due to the substrate's non-crystalline or amorphous structure, which makes the fabrication of high-quality semiconductor devices challenging.

Graphene is remarkably known for its flexibility and has superior characteristics. Besides, it has a similar hexagonal orientation to the ZnO, making a combination of ZnO and graphene feasible. Hence, in this study, we will utilize graphene as the buffer layer for ZnO on the insulator, and we speculate that the grown ZnO structures on the insulator by using graphene as the template or buffer layer will be high-quality.

1.2 Research Motivation

Since decades ago, semiconductor materials such as ZnO, SiC, GaN and GaAs have been widely used in device fabrication, such as in sensors [24-26], transistors [27], optoelectronics [28, 29] and photovoltaic [30]. Generally, the materials' morphology, compositions, and physical and chemical properties can be controlled during the growth process, which can be exploited for specific device fabrication. However, in fabricating a semiconductor device system on a Si substrate, it is crucial to electronically isolate the grown material and Si platform with any isolator, such as SiO_2, Si_3N_4, or any arbitrary substrate, to avoid any current leakage or short circuit, especially in the production of CMOS or field-effect transistor (FET) as in Figure 1.2 [31]. On the other hand, a recent commercial-value semiconductor device was fabricated on a cheap and flexible platform like polymers and glass.

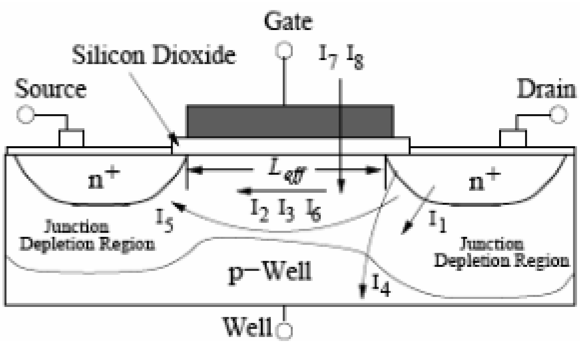

Figure 1.2 Different types of leakage current present in transistor [31]

The concept of flexible electronics device fabrication was introduced in the 1960s [32]. It begins with thinned-Si platforms, which have been used in solar cell fabrication for extra-terrestrial satellites. Over the years, researchers have added some exciting features in fabricating flexible yet lightweight devices, such as increasing their robustness and stretchability. This device must be robust in order to avoid any deformation or malfunction during the integration process. These unique characteristics will eventually increase semiconductor electronic devices' quality, sensitivity, and performance. Aside from thinned-Si, some other inexpensive arbitrary substrates were used as the platform, such as polymers [33, 34], hydrogenated amorphous Si (a-Si:H) [35], and glass [36], which brought out visually appealing features like transparent, bendable and flexible [37]. The semiconductor-based flexible electronics have grasped attention throughout these years due to their wide-ranging applications, such as flexible displays [33] and skin electronics [38].

Recently, some novel technology for fabricating semiconductor-based flexible electronics device systems with an ability to be transferred from one platform to another has arisen. This process usually uses an atomically thin layer of two-dimensional (2D) materials or novel van der Waals (vdW) heterostructures as the transferred tool or template layer [39]. These thin layers of 2D materials such as graphene [40], molybdenum disulfide (MoS_2) [41], or hexagonal boron nitride (hBN) [39, 41], which act as the template will allow the metal-oxide to be directly grown on that template, where it will be part of the device. This innovative technology trend enhanced i-SoC on the semiconductor or arbitrary platform's performance to the full extent with the versatility of device fabrication technique.

In realizing a good performance of flexible and transferable semiconductor-based electronic devices on the insulator-character arbitrary substrate, it is essential to do a fundamental study, beginning with the growth process of semiconductor materials. A breakthrough in growth technology is strongly required to fabricate a high-quality semiconductor-on-insulator with excellent crystallinity and other properties. Since an insulator has amorphous or polycrystalline lattice structures, growing the high crystallinity of semiconductor structures on an insulator is almost impossible. It is because of the large lattice mismatch between a crystalline semiconductor and an amorphous insulator [42]. This significant lattice difference will make the grown semiconductor material in the polycrystalline structure; thus, making a high-quality semiconductor structure is challenging. In reducing the lattice mismatch, a buffer or template layer is exploited during fabrication [43]. Similar to the fabrication of transferable devices, this template layer for the growth of high-quality semiconductor structures on the insulator was placed between semiconductor materials and the insulator. In addition, some growth methods also need a buffer layer of semiconductor materials for the nucleation site of the subsequent material growth, such as in the hydrothermal growth technique [44].

Several intensive researchers have focused on fabricating one and two-dimensional ZnO semiconducting nanostructures throughout the years because of their uniqueness in morphology, compositional and other main properties such as chemical, physical, optical and electrical. This white and non-toxic ZnO is a promising candidate for the fabrication of several devices due to its unique electronic and optical properties, such as a wide bandgap at 3.37 eV and enormous exciton binding energy of 60 meV at room temperature (RT) [45, 46]. These properties allow the ZnO-based devices to be used at RT without any hindering from thermal instability. In addition, the high transparency of ZnO makes it the best choice for making transparent-like devices such as photovoltaics. Thus, ZnO is the best material for the device's system in various astonishing applications such as photovoltaics, optoelectronics, and sensor sensing elements [47].

As mentioned, a template layer is needed during the growth process of ZnO on an insulator, the type of material used for the template layer is also critical, starting with lattice orientation. The lattice orientation of both the template layer and semiconductor is preferably similar. Here, the lattice of both template and insulator will bond together using vdW forces by mechanically-assembled stacks or physical epitaxy or chemical vapor deposition (CVD) [39]. One of the simplest ways to grow ZnO structures on the template is by using the same material, ZnO-seed, as the buffer layer. The exact similar lattice structure will eventually make a least lattice mismatch. This ZnO layer, known as the ZnO seed layer, is commonly used as the nucleation site to enable the subsequent growth of ZnO nanostructures on the insulators [44]. Still, using the ZnO thin layer as a template layer is challenging for fabricating flexible and transferable devices [48]. Those very fragile materials give some minus points for the fabrication of a transferable device as it may be deformed during transferring process of the device. Here, atomically thinned 2D material with a similar lattice orientation to the ZnO, such as graphene, is the best candidate to act as the buffer layer.

Graphene is a 2D hexagonal network of carbon atoms formed by making strong triangular σ-bonds of the sp^2-hybridized orbitals. This bonding structure is similar to the (111) plane of zinc-blende and the c-plane of a hexagonal crystalline structure [49]. Thus, making the growth of semiconductor nanostructures and thin films on graphene feasible. In addition, graphene has excellent potential for novel electronic devices because of its extraordinary optical, electrical, thermal, and mechanical properties, including carrier mobility exceeding 10^4 cm^2/Vs and thermal conductivity of 10^3 W/mK [49].

This zero bandgap and high mobility of graphene can also act as the metal contact or junction, allowing electrons or ions to move freely from one place to another. Therefore, with such excellent characteristics of graphene layers, growing semiconductor nanostructures on graphene layers would enable their novel physical properties to be exploited in diverse, sophisticated device applications. Since graphene is an excellent heat conductor thus, a significant issue of thermal management in heterogeneous integration can also be solved. In addition, the weakly bonded layers of graphene allow transferring the grown semiconductor nanostructures or films onto other arbitrary substrates such as glass, metal, and plastics [37]. Hence, we speculated that using this atom-thick material with high flexibility, transparency, and mobility as the buffer layer would likely increase the quality of grown ZnO.

Diverse group morphologies of ZnO structures such as nanorods [50], nanowires [51], nano-porous [52] and thin films [44] were synthesized using a variety of vapor and liquid phase fabrication techniques. In addition, the vapor phase deposition techniques can be separated into two; physical vapor deposition (PVD) and CVD. These deposition methods include metal-oxide chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), and thermal evaporation, while the liquid phase techniques include hydrothermal, sol-gel deposition and electrodeposition [53]. Each method has its benefits in growing the ZnO structures on a substrate.

PVD methods can be either sputtering, thermal evaporators or others. In some cases, the PVD technique is preferable over CVD due to its advantages, such as fast growth and simplicity. Besides, this technique only uses a single solid target. Again, some methods like electron beam and thermal evaporation have no direct temperature applied on the substrates, making it possible to be carried on the substrates with low-melting temperatures, such as plastic or rubber. In addition, the process is considered less toxic, so there will be no toxic waste, such as toxic gas or liquid, throughout the experiment. Therefore, this study will use thermal evaporation as the only PVD-based method for depositing the ZnO on the insulator at low temperatures.

On the other hand, implementing the liquid phase of the chemical approach as the growth technique is still impossible for industrial-scale production. However, this technique fits for studying the grown semiconductor on an insulator utilizing a buffer layer. Simple, low operating temperatures, yet a wide range of chemicals can be used as the aqueous solutions and electrolytes throughout the process. Thus, it allows the study on the effect of the buffer layer on the grown structures.

Meanwhile, MOCVD has a higher commercial value than other methods because it can grow high-quality nanostructures compared to liquid phase deposition techniques and has cheaper production than the MBE technique. The ability of these methods to coat the unreachable area and evenly coated irregular surfaces is preferable in the coating industry. Besides, it can grow at a large scale with a wide range of elements and compounds with a high-purity end product, making the technique suitable for the industrial scale. However, MOCVD tends to have high energy consumption and higher toxicity due to precursors in metal oxides and waste products. These pros and cons of techniques have initiated researchers to upgrade and invent an innovative approach that can increase production quality and commercial value at a low cost.

One of the innovative technologies is a high-temperature water CVD known as hot water beam CVD. Yasui et al. invented this technique for overcoming the high energy consumption problem using conventional CVD. The hot water CVD used high energy of water molecules originated from the exothermic reaction of H_2 and O_2. Then, the hot H_2O will react with the Zn source to produce ZnO molecules, which then been directly grown on the substrate. Although the research study of grown material in film and nanostructures using this technique is still at the surface, continuous results show that the technique can overcome past problems in using conventional CVD, such as high power consumption and toxic gas [54]. Besides, this technique uses a low working temperature and pressure, suitable for pressure and temperature-sensitive materials such as a polymer.

In this study, the deposition of ZnO structures on an insulator with graphene as a buffer layer is carried out by a combination of thermal evaporation and oxidation. The deposition process was carried out using the thermal evaporation technique under vacuum conditions, with ZnO powder as the main target. Next, the deposited ZnO layer was annealed under an oxygen (O_2) ambient. Only one parameter was used to optimize the oxidation condition, which is the oxidation time, that acted on ZnO with and without buffer layers. Besides, the physically deposited ZnO will be utilized as the buffer layer to study the growth of ZnO structures using the liquid phase of the chemical approach; the hydrothermal method. The outcomes are compared with the hydrothermally grown ZnO structures on an insulator utilizing single-layer graphene (SLG) and multi-layer graphene (MLG). These buffer layer differences are expected to play a role in the growth of ZnO structures. The recent vapor phase CVD technique, hot water beam CVD, grows ZnO structures on SLG and MLG insulators. Here, the number of graphene layers and the growth time were differentiated. Finally, grown ZnO structures' morphological, crystallinity and optical properties are systematically characterized.

1.3 Problem Statement

The use of high crystalline semiconductor material in fabricating optoelectronics and photovoltaic applications has been started for years. Over the last decades, heterogeneous integration technology has been promising in realising the next-generation technology, the so-called i-SOC. However, in realizing such technology, it is crucial to isolate the active semiconductor and the Si platform to avoid any current leakage or short circuit. It has brought the introduction of the insulator to many multifunctional devices such as power devices, electronic displays and so forth. In the meantime, arbitrary substrates, such as polymer, glass and paper, were introduced to replace the conventional Si in fabricating electronic devices, where these substrates had some unique features such as flexibility and transparency. And recently, the emergence of transferable electronics that can be transferred between the arbitrary substrate, such as LED, utilised template or buffer layers during device fabrication.

ZnO, an II-VI element, is given high interest to be studied for its wide bandgap and large exciton energy. These behaviours allow the ZnO-based device to work well at room temperature and have a higher breakdown voltage. Moreover, ZnO has high transparency, can be implemented for the element in a transparent device and is environmentally friendly. However, a significant lattice mismatch has made a direct growth of crystalline ZnO on the insulator almost impossible. Here, a buffer layer such as graphene and hBN with a similar hexagonal lattice structure with the ZnO was introduced to reduce the lattice difference. However, graphene consists of a single element, robust, flexible and transparent, and has zero bandgap that can be exploited as the active element, is the best choice as the buffer or template layer. Thus, in this case, the use of graphene is favourable due to the similar hexagonal lattice structure with the ZnO and the graphene's superior characteristics, such as good conductivity, which are expected to enhance the performance of the semiconductor ZnO on the insulator. However, some arbitrary substrates, such as polymer or paper, have low thermal resistance, which becomes a critical issue in the growth process. Therefore, the low-temperature technique is needed.

Thus, we need a breakthrough in the growth technique, where the growth processes are focused on low-temperature growth at less than 600°C. Several techniques for the growth process are covered in physical and chemical approaches. PVD and CVD are common techniques used on a commercial scale, and one of the simple yet well-known liquid phases using a chemical approach is hydrothermal. In this study, the thermal evaporation PVD with a combination of oxidation at low temperatures will be used as one of the growth techniques. One of the CVD techniques, hot water beam, is one of the latest techniques which focuses on low-temperature growth with simple H_2 and O_2 gases as the H_2O source, and dimethyl zinc (DMZn) as the Zn source also will be carried out to grow the ZnO on graphene/insulator. One chemical approach acknowledged for its simple and low operation temperature, hydrothermal, is used to grow ZnO on the insulator in this study. The growth process will use low growth temperature at atmospheric pressure as the constant parameter.

1.5 Research Objective and Scopes

In this study, the main objective is to investigate the low-temperature growth of ZnO on an insulator by utilizing graphene as the buffer layer. The study will use physical and chemical techniques for the growth process of the insulator. In addition, the quality of ZnO structures will be thoroughly analyzed from their morphology, crystallinity and optical properties. There are three sub-objectives for achieving the goal.

a) To synthesize and optimize the ZnO growth on an insulator utilizing a buffer layer using a combination of thermal evaporation PVD, hydrothermal, and a recent technique, hot water beam CVD.
b) To compare the performances of the grown ZnO on graphene/insulator by its morphology, crystallinity, and optical properties.
c) To analyze the best method for the ZnO on the insulator, utilizing a buffer layer.

This study concentrates on the growth of ZnO on an insulator using graphene as the buffer layer. The deposition and growth process will focus on low-temperature techniques using vapor and liquid phases; thermal evaporator PVD, hydrothermal, and hot water beam CVD. The effect of graphene on the grown ZnO has also been comprehensively studied. This study can be divided into four scopes, where three scopes are related to the growth techniques, and one scope for the second and third objective :

i. The thermal evaporator PVD and oxidation process were combined in the deposition of ZnO on graphene on the insulator. ZnO's oxidation study was done with different oxidation times, 30 – 120 minutes, with a fixed temperature of 450°C. The as-deposited and oxidized deposited ZnO structures on buffered graphene were compared with non-buffered ZnO on the insulator. All finding was studied based on their morphology, crystallinity and optical properties.

ii. The liquid phase technique, hydrothermal, was used in growing ZnO structures on the insulator. This study used three types of buffer layers for the grown ZnO: SLG, MLG, and ZnO seed layer. An equimolar solution of Zinc nitrate hexahydrate and HMTA was used to grow ZnO on all different buffer layers on the insulator. The grown ZnO was compared based on its morphology, crystallinity, and optical properties.

iii. A relatively new method called hot water beam CVD was used to grow ZnO structures on graphene on an insulator. Here, SLG and MLG were used as the buffer layer. The high purity of O_2 and H_2 gases play a crucial part in forming hot water molecules with Pt catalyst. DMZn is used as the zinc source at fixed substrate temperature. A study on ZnO on an insulator utilizing a buffer layer by varying time and gas flow rates was evaluated. Effect on the quality of morphology, crystallinity, and optical properties of grown ZnO on different buffer layer graphene on insulators were analysed.

iv. All the results are analyzed and compared by their performance on crystallinity and optical properties of the grown ZnO structures on the insulator, with and without a graphene buffer layer. The analyses were done to get the best technique to grow ZnO on an insulator utilizing graphene as the buffer.

1.6 Overview of Thesis Organization

This thesis consists of seven chapters and three chapters for results and discussions. Chapter 1 overviews the research background and its motivation for the growth of semiconductor material, ZnO, on insulator utilizing graphene as a template layer. The problem of the study has also been discussed in this section. Moreover, the research objective and its scope are also presented.

Chapter 2 gives an overview of the fundamental properties of ZnO and graphene. Discussion of previous studies of ZnO and buffer layer hybridisation on the insulator and their possible applications will be explained. In addition, growth techniques of ZnO structures on the insulator, especially in the thermal evaporator, hydrothermal, and catalyzed hot water beam and its previous study, are described in this chapter. The potential applications of oriented non-buffered ZnO nanostructures and ZnO nanostructures on graphene are also discussed.

Chapter 3 focuses on the research methodology. The substrate's properties and preparation prior to the experiment are presented. Three different methods used to grow ZnO structures are explained, and the parameters used during the study are also discussed. Preparation and techniques used to grow ZnO structures are presented. The characterization techniques used to study the grown ZnO are also listed.

Chapter 4 discussed the graphene factor to the grown ZnO on the insulator. A combination of thermal evaporator PVD and the oxidation process of the grown ZnO on graphene on an insulator will be discussed thoroughly. Besides, the comparison between grown ZnO on the insulator and grown ZnO on graphene on the insulator will be explained. The discussions will thoroughly examine the morphology, crystallinity and optical properties of the deposited ZnO on the insulator.

Chapter 5 studies the effect of buffer layers used to the grown ZnO on the insulator using the liquid-phase hydrothermal technique. Morphology, crystallinity and optical properties of the deposited ZnO on the insulator will be thoroughly discussed.

Chapter 6 introduces the new CVD method to grow high-quality ZnO. The method of the new CVD, hot water beam CVD, and the grown ZnO on graphene on the insulator will be explained. Morphology, crystallinity, and optical properties of grown ZnO on an insulator will be thoroughly discussed. Comparison between grown ZnO using thermal evaporator PVD, the hydrothermal technique and the new hot water beam CVD will also be explained here.

Finally, Chapter 7 concludes the contributions of the present works and discusses future research directions.

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